Received 8 June 2021; revised 9 July 2021; accepted 12 July 2021. Date of publication 19 July 2021; date of current version 13 December 2021.
The review of this paper was arranged by Editor Q. Shao.

Digital Object Identifier 10.1109/JEDS.2021.3097995

Two-Dimensional Inverters Based on MoS_2-hBN-Graphene Heterostructures Enabled by a Layer-by-Layer Dry-Transfer Method

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This work was supported in part by the Ministry of Science and Technology under Grant 2018YFE0115500 and Grant 2019YFE0120300; in part by the National Natural Science Foundation of China under Grant 62004026, Grant 62004032, and Grant 61774029; and in part by the Sichuan Provincial Science and Technology Department under Grant 2021YJ0517, Grant 21CXTD0088, Grant 21YYJC3079, Grant 2019JDTD0006, and Grant 2019YFSY0007.

ABSTRACT Two-dimensional (2D) layered materials offer unique opportunities for building novel nanoscale electronics devices. As the family of 2D materials and their heterostructure continue to grow, it is desirable to have a technique capable of quickly prototyping 2D devices for efficient exploration of new materials and devices. Here, we demonstrate a facile all-dry transfer technique that can very efficiently build 2D devices, and show that a digital inverter can be realized using such technique. Our results can be leveraged for building and testing new types of 2D nanodevices with high throughput.

INDEX TERMS 2D materials, nanodevice, 2D semiconductor, device fabrication.

I. INTRODUCTION

Two-dimensional (2D) layered materials hold great promises for enabling new atomically-thin nanodevices that can lead to new paradigms in information processing and computation [1], [2]. In particular, the ultimate thinness of these devices can enable logic gates with very short channel length [3], [4], low-power electronics, flexible circuits [5], [6], and are compatible with transparent substrates [7], [8], offering new opportunities for smart wireless components.

While transistors based on 2D materials have been broadly explored [9], [10], the first step towards building logical circuits is to construct logical gates using multiple transistors. Among them, inverter is one of the most basic digital circuit components, and are often used as the building block of the logical "NOT" gate. While a number of 2D inverters have been demonstrated [11], [12], most of them are constructed using conventional techniques such as photolithography or e-beam lithography.

While these techniques are scalable and can be used towards large scale production, it is still desirable to have an alternative technique that's capable of very fast prototyping new devices, so that inverters based on different types of 2D materials can be efficiently realized and explored. Further, to construct novel 2D circuits it may require different type of devices structures to be fabricated on the same substrate, and certain 2D device structures (such as nanoelectromechanical systems, which are based on suspended 2D structures) may not be compatible with the wet processes involved in the lithography techniques.

We have demonstrated a facile all-dry transfer technique that can quickly fabricate 2D devices, and show that 2D inverters can be efficiently prototyped [13]. Here, we presented additional experiment details and extended analysis about MoS_2 transistors performance, including top-gated/back-gated devices, and inverter performance.

II. MATERIAL CHARACTERIZATION

Molybdenum disulfide (MoS_2) is the prototypical 2D semiconductor, and has been widely explored to construct novel electronic devices [14], [15]. To demonstrate the fast-prototyping capability of the dry transfer technique, we use mechanically exfoliated MoS_2 in this work. We characterize the exfoliated 2D flakes using Raman spectroscopy.

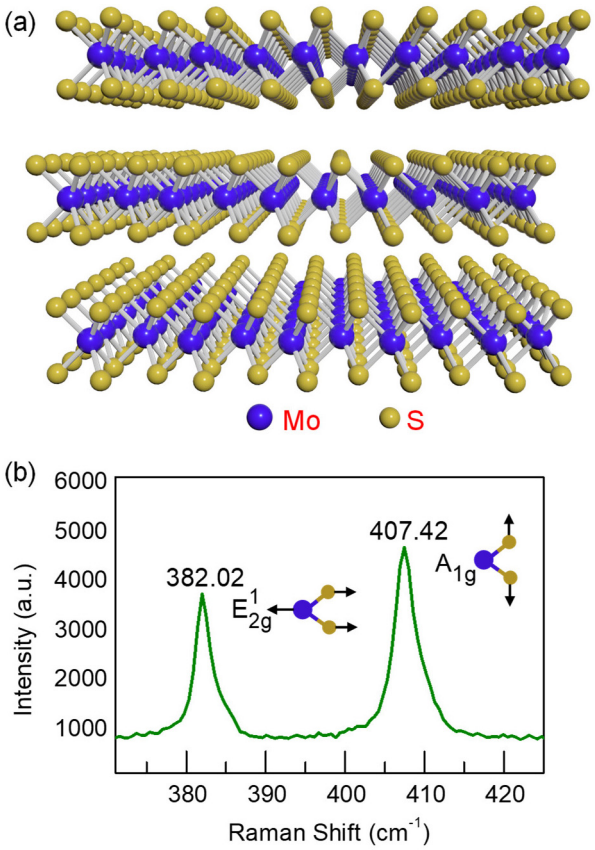

FIGURE 1. **MoS_2 material characterization. (a) Crystal structure of MoS_2. (b) Raman spectrum and illustration of the vibrational modes.**

Through analyzing the Raman spectrum (Fig. 1), we can characterize the quality and thickness of the MoS_2 flake. First, the sharp profile and strong intensity of the two featured Raman peaks (E^1_{2g} and A_{1g} vibrations) confirm the high quality of our sample. Besides, the two featured Raman peaks are found at 382.02 cm^{-1} (E^1_{2g}) and 407.42 cm^{-1} (A_{1g}), referring to the multilayer feature (~10 layers) of the MoS_2 flake [16].

III. DEVICE FABRICATION

We fabricate the MoS_2 nanoelectronic devices using a dry transfer method [17]. First, MoS_2 flakes are exfoliated using the scotch tape method onto a Polydimethylsiloxane (PDMS) piece residing on a glass slide. The glass slide is then flipped upside down and mounted onto an x-y-z translational stage, and a target MoS_2 flake is identified under the microscope for making the device (Fig. 2b').

The device substrate is made of a silicon wafer with 290 nm SiO_2 on top. Metal electrodes (40 nm Cr/Au) are prepatterned using photolithography onto the substrate, forming the source and drain contacts for the MoS_2 devices (Fig. 2a').

During the dry transfer process, the PDMS is gradually lowered onto the substrate under a microscope, with the indemnified MoS_2 flake aligned towards the devices area between the electrodes. Once the PDMS piece is in contact with the substrate, the glass slide is further lowered a bit in order to depress the MoS_2 flake onto the substrate for better adhesion, and then very slowly raised

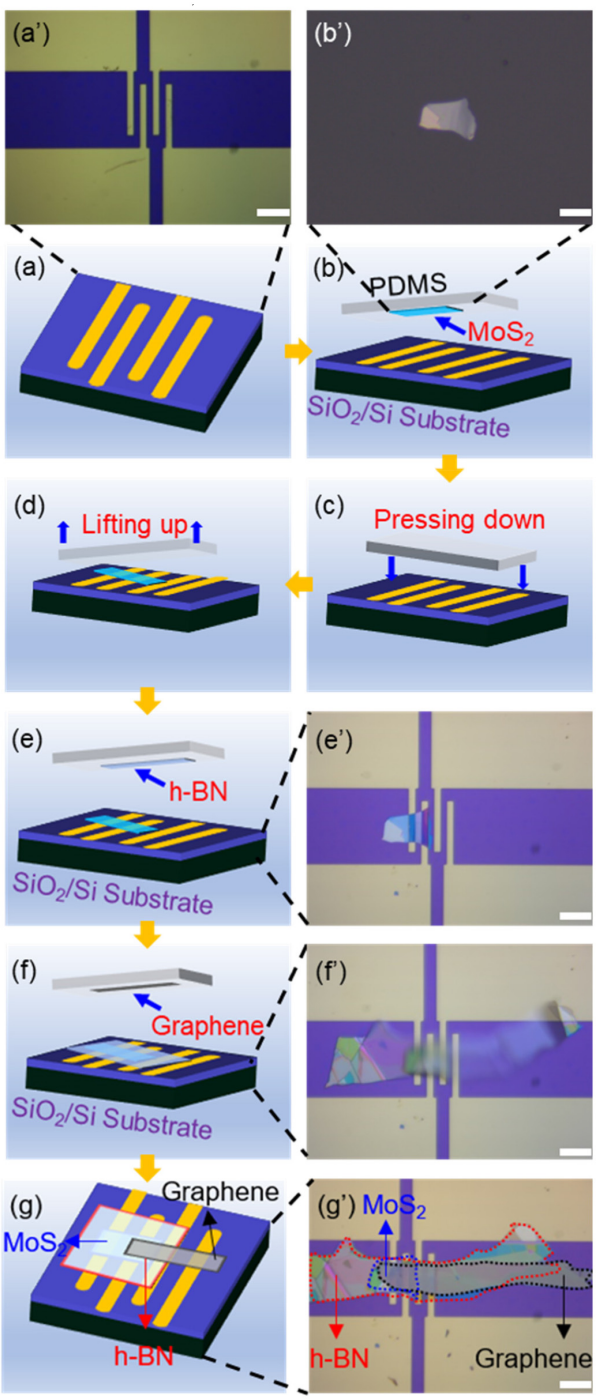

FIGURE 2. **Device fabrication using the facile dry-transfer method. (a-g) The transfer process. (a'-g') Optical images of the starting substrate, the MoS_2 flake, and device structure during each fabrication step. An additional transfer step was performed after the stage shown in Fig. 2g', with another graphene flake connecting the top-gate graphene piece to the metal electrode. For clarity the optical image after completing that step is now shown here, but is available upon request by contacting the authors. Scale bar: 25 μm. All optical images are roughly 215 μm by 160 μm in size.**

to detach the PDMS from the substrate. Due to van der Waals interaction, the MoS_2 flake can stay on the substrate, contacted by the electrodes. We repeat such process multiple times, and deposit a hexagonal boron nitride (h-BN) flake as a top dielectric layer, followed by another graphene flake on top serving as the top gate electrode. The complete dry-transfer process and the device image during each step are shown in Fig. 2.

The resulting device has a MoS_2/h-BN/graphene heterostructure, with source, drain, and two gate electrodes: the top electrode is the graphene piece in contact with one metal bond pad, and the bottom electrode is the highly-doped Si substrate. The device is then annealed in 250°C for 30 min with N_2 flow of 6 cc/min for better electrical contact [18].

IV. TRANSISTOR MEASUREMENTS

We first characterize the electronic properties of individual transistor devices using a probe station. Fig. 3a shows the measurement configuration. Here, the source electrode of the device is connected to the ground, and the drain electrode is connected to the output of a parameter analyzer, which supplies the drain voltage $V_{\rm ds}$ and measures the drain current $I_{\rm ds}$. Two other parameter analyzers are connected to the top gate and back gate electrodes, and supply the gate voltages $V_{\rm tgs}$ and $V_{\rm bgs}$, respectively. During the measurements, as the voltage on one gate electrode is swept, the other gate electrode is grounded to avoid coupling between the two gates [19].

We first measure the back-gated transistor behavior (Fig. 3c). When $V_{\rm bgs}$ is 3V and $V_{\rm ds}$ is swept from -0.1 V to 0.1V, the range of drain current $I_{\rm ds}$ is $\pm$80 nA. Figure 3d shows the transfer curve of the same transistor. The device exhibit N-type transfer behavior, as $I_{\rm ds}$ increases with the $V_{\rm bgs}$, reaching 50 nA at $V_{\rm bgs} = 3$ V.

We also explore the device performance under different drain biases and gate voltage ranges. Figure 3e shows that as the back gate voltage is swept from -5 V to 3 V, $I_{\rm ds}$ does not change significantly when $V_{\rm ds}$ is 0.1 V. Meanwhile, if $V_{\rm ds}$ is increased to 0.3V, $I_{\rm ds}$ will also increase (Fig. 3f).

With the top gate dielectric layer (h-BN) being much thinner than that of the bottom gate (SiO_2), the top gate is expected to be much more efficient in controlling the carrier density and thus conductance in the transistor channel. Accordingly, we examine the top-gated transistor behavior (Fig. 3g).

We first measure the transport curve of the top-gated device. When $V_{\rm tgs}$ is 1 V and $V_{\rm ds}$ is swept from -0.1 V to 0.1V, the range of drain current $I_{\rm ds}$ is $\pm$300 nA, which is much larger drain current range compared with that of the back-gated device. Figure 3h shows the transfer curve of the same transistor. When we sweep the top gate voltage -3 V to 0.5 V ($V_{\rm ds} = 0.1$ V), it shows a more pronounced N-type transfer curve, with a clear on and off region, and on-state current reaches up to 250 nA. With the same $V_{\rm ds}$ (0.1 V), the drain current for the top-gated device is almost 10 times that of the back-gated device, all while using the same channel. As we continue to increase the top gate voltage, the drain current $I_{\rm ds}$ also continue to increase, reaching 500 nA with $V_{\rm tgs} = 2.5$ V, as shown in Fig. 3i and 3j.

From the above measurements, we confirm clear N-type transfer behavior of the devices. The top gate is much more efficient in switching the device on and off, i.e., requiring a much lower switching voltage, consistent with the top gate dielectric being much thinner than the bottom one.

We further measure the MoS_2 transistor electrical performance by sweeping both back gate and top gate voltages, while setting the $V_{\rm ds}$ is 0.5V, with the results shown in Fig. 3k and 3l. The collective gate tuning behavior, from both top gate and back gate, allows us to extract more information about the device by comparing the gate tuning effects from the two gates.

In the linear regime, the dependence of drain current I_{ds} on the two gates can be written as $I_{ds} = \frac{w\mu C_{ox}}{L}(V_{bgs} - V_{th})$ and $I_{ds} = \frac{w\mu C_{bn}}{L}(V_{tgs} - V_{th})$ [19], where μ, L and W are the mobility, channel length and width of transistor, C_{ox} and C_{bn} are the capacitance per unit area to the channel for the back gate (with silicon dioxide as the gate dielectric) and top gate (with h-BN as the gate dielectric), and $V_{\rm th}$ is the threshold voltage.

When both gates are used, the carrier density and thus the conductance of the channel is controlled collectively by both gates, through the two gate capacitors. Both gates can induce/remove charge from the channel through its gate voltage and gate capacitor. Therefore, when one gate voltage is increased to induce charge in the channel while the other gate voltage is decreased to remove charge in the channel, there is a condition where the effects from the two gates cancel each other, resulting in zero net charge in the carrier density and thus the current. Such conditions are manifested by the constant-current contour lines in Fig. 3l, from which we can derive the ratio of the two gate capacitors using the slope of the contour (the voltage ratio).

From the argument presented above and the equations, one can derive the ratio of the two gate capacitances as $\frac{C_{ox}}{C_{bn}} = \frac{V_{tgs}-V_{th}}{V_{bgs}-V_{th}}$. In the linear regime, one can use $\frac{C_{ox}}{C_{bn}} = \frac{dV_{tgs}}{dV_{bgs}}$ by examining the slope of constant-$I_{\rm ds}$ contour line in Fig. 3l (dashed line); we find that the slope of the line ($\frac{dV_{bgs}}{dV_{tgs}}$) is -42.42, which gives the ratio of the two capacitances.

Using the thickness of SiO_2 ($d_{ox} = 290$ nm) and relative permittivity of SiO_2 ($\varepsilon_{rox} = 3.9$), we calculate $C_{ox} = \frac{\varepsilon_0\varepsilon_{rox}}{d_{ox}} = 1.19 \times 10^{-4}$ F/m^2, which further gives on $C_{bn} = 50.48 \times 10^{-4}$ F/m^2. We then use $C_{bn} = \frac{\varepsilon_0\varepsilon_{rbn}}{d_{bn}}$ to calculate the h-BN thickness, with relative permittivity of h-BN $\varepsilon_{rbn} = 3.76$ [20]. From the equation we obtain thickness of the h-BN $d_{bn} = 6.6$ nm, which appears to be a reasonable value given the contrast and color of the h-BN flake in the optical image.

V. INVERTER MEASUREMENTS

We then construct digital inverters by connecting multiple transistors, and test their digital operation. Figure 4a shows

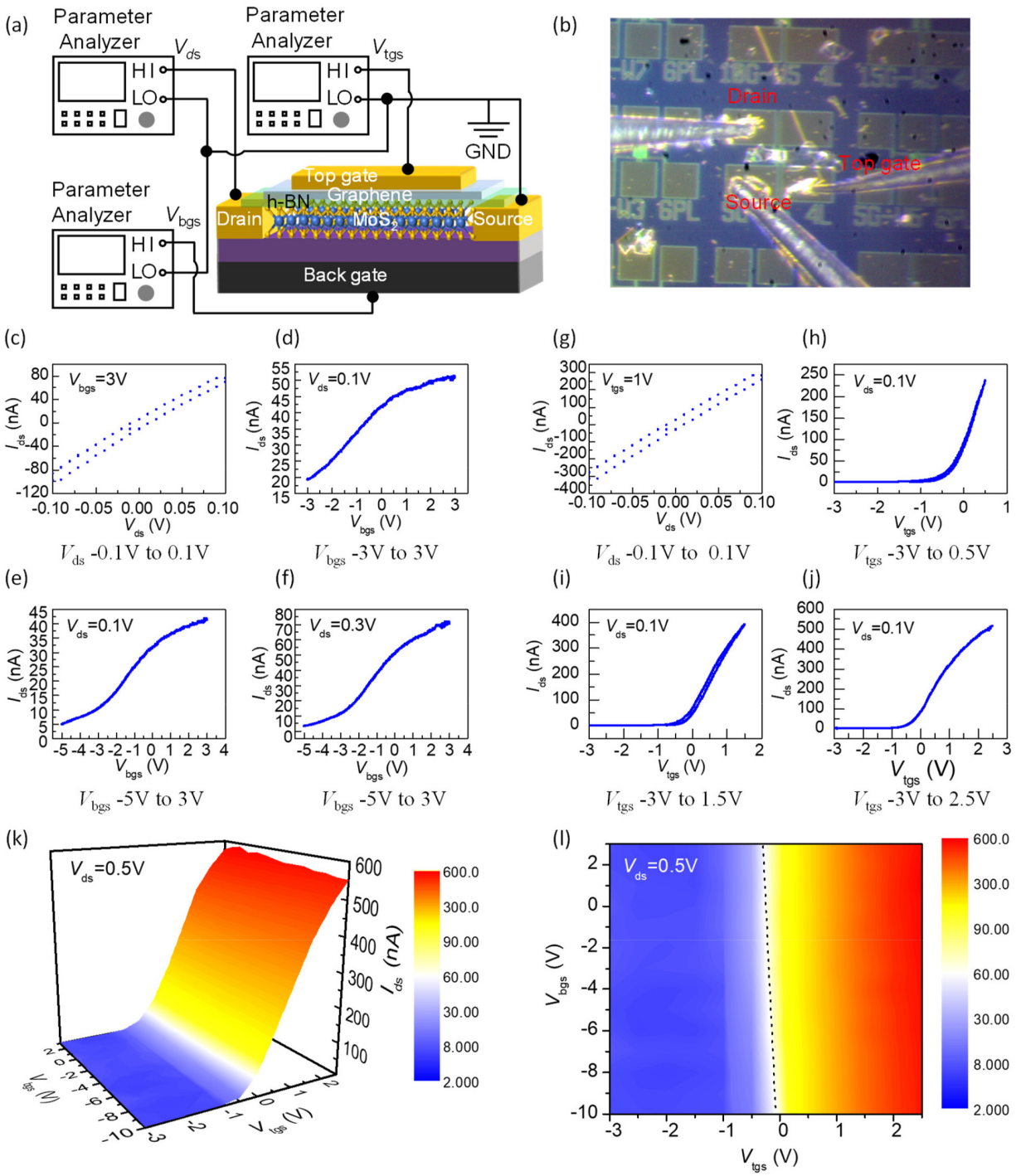

FIGURE 3. **MoS_2 transistor. (a) Measurement circuit. (b) Optical image of a device being measured, with bond pads leading to electrodes contacted by electrical probes under microscope. (c) Output curve of back-gated transistor, with V_{ds} from −0.1 V to 0.1 V, and V_{bgs} = 3 V. (d) Output curve of back-gated transistor, with V_{bgs} from −3 V to 3 V, and V_{ds} = 0.1 V. (e) Output curve of back-gated transistor, with V_{bgs} from −5 V to 3 V, and V_{ds} = 0.1 V. (f) Output curve of back-gated transistor, with V_{bgs} from −5 V to 3 V, and V_{ds} = 0.3 V. (g) Output curve of top-gated transistor, with V_{ds} from −0.1 V to 0.1 V, and V_{tgs} = 1 V. (h) Output curve of top-gated transistor, with V_{tgs} from −3 V to 0.5 V, and V_{ds} = 0.1 V. (i) Output curve of top-gated transistor, with V_{tgs} from −3 V to 1.5 V, and V_{ds} = 0.1 V. (j) Output curve of top-gated transistor, with V_{tgs} from −3 V to 2.5 V, and V_{ds} = 0.1 V. (k) and (l) 3D color plot and 2D color map of I_{ds} as a function of both V_{tgs} and V_{bgs}, measured by sweeping both gate voltages simultaneously.**

the schematic of a digital inverter composed of two N-type transistors, together with its truth table and output curve when used in digital circuits. Figure 4b shows the configuration of an inverter composed of two transistors, together with the measurement circuit diagram, with three parameter analyzers used for V_{dd}, V_{out} and V_{in}, respectively.

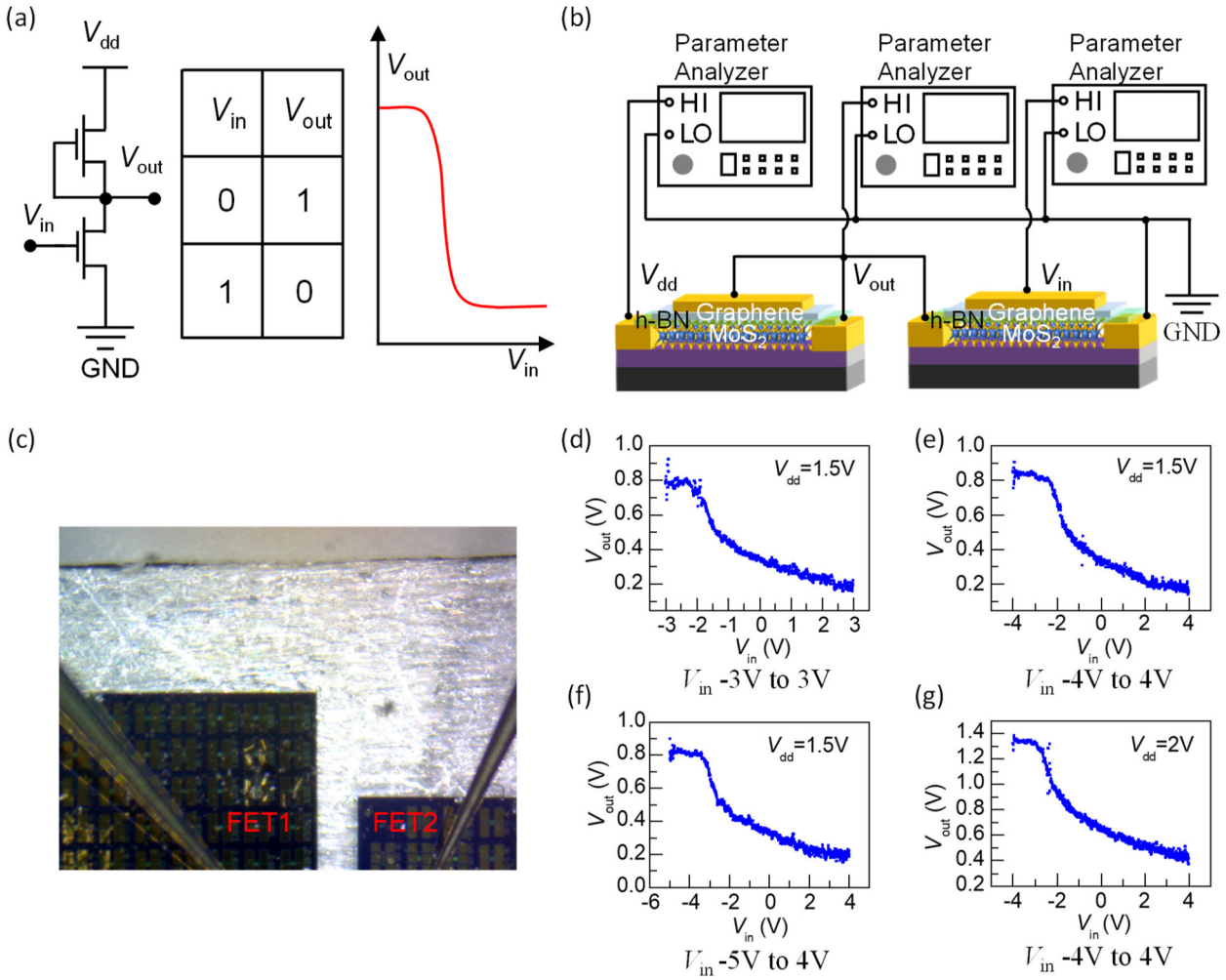

FIGURE 4. **MoS_2 inverter. (a) Circuit schematic of an inverter based on two transistors, its truth table and output curve. (b) Measurement circuit. (c) Optical image of a device connected to the probes. (d) Measured output curve of the MoS_2 inverter, with V_{in} from −3 V to 3 V, and V_{dd} = 1.5 V. (e) Measured output curve of the MoS_2 inverter, with V_{in} from −4 V to 4 V, and V_{dd} = 1.5 V. (f) Measured output curve of the MoS_2 inverter, with V_{in} from −5 V to 4 V, and V_{dd} = 1.5 V. (g) Measured output curve of the MoS_2 inverter, with V_{in} from −4 V to 4 V, and V_{dd} = 2 V.**

Figure 4c shows an optical image of an inverter made of two MoS_2 transistors on two different substrates.

The measured inverter performance is shown in Figs. 4d-g, showing the inverter input *vs.* output. We find that the dry-transferred MoS_2 devices exhibit clear inverter behavior, with output voltage being negatively correlated with the input voltage, *i.e.,* when input is high, the output is low; and vice versa. We also measure the device with different input voltage ranges, and confirm the functionality of the MoS_2 inverter.

Specifically, in the first measurement (Fig. 4d), we use V_{in}: from −3 V to 3 V, and set V_{dd} = 1.5 V. We observe clear inverter behavior with V_{out} going from 0.8 V to 0.2 V. We then vary both the range of input voltage (Figs. 4e-f) and V_{dd} (Fig. 4g), and find that the output window can be increased as V_{dd} increases, as expected for a two-transistor inverter.

VI. CONCLUSION

A dry-transfer method has been successfully demonstrated in building inverters based on MoS_2/h-BN/graphene heterostructures, and the resulting devices are tested and exhibit clear inverter behavior. The result shows that the dry transfer method can be used for efficient prototyping of new types of 2D devices and testing their performances, such as quickly surveying the device properties of nanoelectronics devices and circuit components based on different combination of 2D materials and heterostructures. Such technique is compatible with the processing requirement for certain type of 2D nanostructures, such as nanoelectromechanical devices [21], [22], and offers unique opportunities for building new types of mixed-type circuits components [23] that can combine multiple functionalities, such as sensing, signal processing, and logical operation.

REFERENCES

[1] H. Tang *et al.*, "Recent progress in devices and circuits based on wafer-scale transition metal dichalcogenides," *Sci. China Inf. Sci.*, vol. 62, no. 12, Dec. 2019, Art. no. 220401.

[2] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nat. Nanotechnol.*, vol. 7, no. 11, pp. 699–712, Nov. 2012.

[3] S. B. Desai *et al.*, "MoS_2 transistors with 1-nanometer gate lengths," *Science*, vol. 354, no. 6308, pp. 99–102, Oct. 2016.

[4] K. Xu *et al.*, "Sub-10 nm nanopattern architecture for 2D material field-effect transistors," *Nano Lett.*, vol. 17, no. 2, pp. 1065–1070, Jan. 2017.

[5] G.-H. Lee *et al.*, "Flexible and transparent MoS_2 field-effect transistors on hexagonal boron nitride-graphene heterostructures," *ACS Nano*, vol. 7, no. 9, pp. 7931–7936, Aug. 2013.

[6] H.-Y. Chang *et al.*, "High-performance, highly bendable MoS_2 transistors with high-k dielectrics for flexible low-power systems," *ACS Nano*, vol. 7, no. 6, pp. 5446–5452, May 2013.

[7] S. Das, R. Gulotty, A. V. Sumant, and A. Roelofs, "All two-dimensional, flexible, transparent, and thinnest thin film transistor," *Nano Lett.*, vol. 14, no. 5, pp. 2861–2866, Apr. 2014.

[8] J. Yoon *et al.*, "Highly flexible and transparent multilayer MoS_2 transistors with graphene electrodes," *Small*, vol. 9, no. 19, pp. 3295–3300, Oct. 2013.

[9] Y. Xu, W. Li, D. Fan, Y. Shi, H. Qiu, and X. Wang, "A compact model for transition metal dichalcogenide field effect transistors with effects of interface traps," *Sci. China Inf. Sci.*, vol. 64, no. 4, Apr. 2021, Art. no. 140408.

[10] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 147–150, Jan. 2011.

[11] B. Radisavljevic, M. B. Whitwick, and A. Kis, "Integrated circuits and logic operations based on single-layer MoS_2," *ACS Nano*, vol. 5, no. 12, pp. 9934–9938, Nov. 2011.

[12] H. Wang *et al.*, "Integrated circuits based on bilayer MoS_2 transistors," *Nano Lett.*, vol. 12, no. 9, pp. 4674–4680, Aug. 2012.

[13] Y. Liang *et al.*, "Nanoscale inverters enabled by a facile dry-transfer technique capable of fast prototyping of emerging two-dimensional electronic devices," presented at 5th IEEE Electron Devices Technol. Manuf. Conf. (EDTM), Chengdu, China, 2021, pp. 1–3. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9421003

[14] S. Wu *et al.*, "Interface engineering of ferroelectric-gated MoS_2 phototransistor," *Sci. China Inf. Sci.*, vol. 64, no. 4, Mar. 2021, Art. no. 140407.

[15] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically thin MoS_2: A new direct-gap semiconductor," *Phys. Rev. Lett*. vol. 105, no. 13, Sep. 2010, Art. no. 136805.

[16] L. Liang and V. Meunier, "First-principles Raman spectra of MoS_2, WS_2 and their heterostructures," *Nanoscale*, vol. 6, no. 10, pp. 5394–5401, Feb. 2014.

[17] R. Yang, X. Zheng, Z. Wang, C. J. Miller, and P. X.-L. Feng, "Multilayer MoS_2 transistors enabled by a facile dry-transfer technique and thermal annealing," *J. Vac. Sci. Technol. B*, vol. 32, no. 6, Oct. 2014, Art. no. 061203.

[18] R. Yang, Z. Wang, and P. X.-L. Feng, "Electrical breakdown of multilayer MoS_2 field-effect transistors with thickness-dependent mobility," *Nanoscale*, vol. 6, no. 21, pp. 12383–12390, Aug. 2014.

[19] M. S. Fuhrer and J. Hone, "Measurement of mobility in dual-gated MoS_2 transistors," *Nat. Nanotechnol.*, vol. 8, no. 3, pp. 146–147, Mar. 2013.

[20] A. Laturia, M. L. Van de Put, and W. G. Vandenberghe, "Dielectric properties of hexagonal boron nitride and transition metal dichalcogenides: From monolayer to bulk," *NPJ 2D Mater. Appl.*, vol. 2, no. 1, pp. 1–7, Mar. 2018.

[21] Z. Wang *et al.*, "Black phosphorus nanoelectromechanical resonators vibrating at very high frequencies," *Nanoscale*, vol. 7, no. 3, pp. 877–884, Oct. 2015.

[22] Z. Wang *et al.*, "Resolving and tuning mechanical anisotropy in black phosphorus via nanomechanical multimode resonance spectromicroscopy," *Nano Lett.*, vol. 16, no. 9, pp. 5394–5400, Aug. 2016.

[23] Y. Hao *et al.*, "Recent progress of integrated circuits and optoelectronic chips," *Sci. China Inf. Sci.*, vol. 64, no. 10, Oct. 2021, Art. no. 201401.