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Junction Design and Complementary Capacitance Matching for NCFET CMOS Logic

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ABSTRACT Negative capacitance field effect transistors (NCFETs) are modeled in this study, with an emphasis on junction design, implications of complementary logic, and device V_t menu enablement. Contrary to conventional MOSFET design, increased junction overlap is beneficial to NCFETs, provided the remnant polarization (P_r) is high enough. Combining broad junctions with complementary capacitance matching (CCM) in MFMIS (metal/ferroelectric/metal/insulator/semiconductor) NCFETs, it is shown that super-steep and non-hysteretic switching are not mutually exclusive, and that it is theoretically possible to achieve non-hysteretic sub-5 mV/dec *SS* over > 6 decades. In a CMOS circuit, due to CCM, low-V_t pairs provide steeper subthreshold swing (*SS*) than high-V_t pairs. Transient power/performance is also modeled, and it is shown that a DC-optimal NCFET design, employing broad junctions, CCM, and a low-V_t NFET/PFET pair, does not translate to improved AC power/performance in unloaded circuits compared to a conventional FET reference. It is also shown that the same non-hysteretic DC design point is hysteretic in AC and may also lead to full polarization switching at higher voltages. Thus, a usable voltage window for AC NCFET operation forces a retreat from the DC-optimal design point.

INDEX TERMS Ferroelectric, negative capacitance, modeling, TCAD, capacitance matching, junction design, Miller Effect, AC performance.

I. INTRODUCTION

Negative capacitance field effect transistors (NCFETs) have received attention [1]–[6] for their potential to extend CMOS scaling by improving electrostatic integrity and, in some cases [6]–[8], achieving sub-*kT* subthreshold swing (*SS*). The expectation for NCFETs is to achieve enhanced, high speed switching capability with zero or near-zero hysteresis (*i.e.*, for logic applications), unlike FEFETs which specifically target hysteretic switching (*i.e.,* for memory applications). However, the boundary condition to achieve enhanced, non-hysteretic switching is a problem for NCFETs, due to a lack of adequate capacitance matching over the full gate voltage (V_g) sweep range [1], or a lack of adequate polarization switching speed [4], [9]. Achieving non-hysteretic switching requires the absolute value of the negative capacitance component of the ferroelectric capacitance (C_{NC}) to be greater than the maximum dielectric capacitance (C_{DE}) with which C_{NC} is placed in series (Fig. 1). In a transistor, this means $C_{NC} > C_{inv}$, which in-turn requires C_{NC} to be poorly matched to the off-state capacitance, otherwise known as overlap capacitance (C_{ov}), which is much lower than C_{inv}. This results in enhanced switching characteristics only near inversion and less so in the off-state. Reducing *SS* requires C_{NC} to be matched to C_{ov}, but this results in hysteretic switching and the prevalence of thought that super-steep and non-hysteretic switching are mutually exclusive.

1-dimensional channel materials have been proposed [10] to reduce the difference between C_{inv} and C_{ov}, thereby improving capacitance matching across the full V_g sweep range, essentially by forcing C_{inv} to be limited by the density of states (DOS) of inversion carriers. However, drive current is also DOS-limited. Reference [11] proposed a multi-layer ferroelectric/dielectric (FE/DE) stack, with each FE layer possessing a different negative capacitance (NC) slope, in order to achieve said matching; however, *SS* reduction in the

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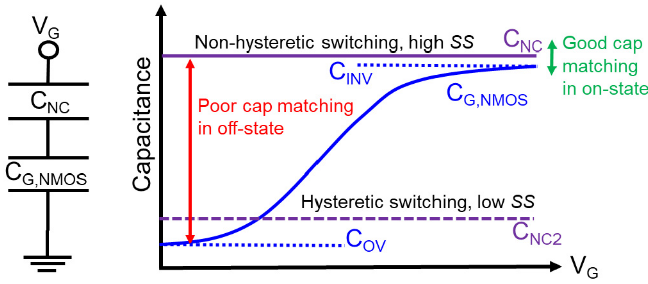


FIGURE 1. Equivalent capacitance network and illustrative C-V curve showing NMOS and NC curves. C_{NC} > C_{INV} results in non-hysteretic switching, but low voltage gain in the off-state due to C_{NC} >> C_{OV}. Setting C_{NC} to C_{NC2}, which is matched more closely to C_{OV}, results in very low *SS*, but also hysteretic switching as C_{NC2} < C_{INV}.

deep off-state is modest. Reference [7] demonstrated non-hysteretic sub-*kT* switching in hardware; however, remnant polarization (P_r) is small and so only part of the off-state is in the NC regime. The work presented herein will describe the importance of treating NCFETs as a complementary pair and how this can be leveraged to break the perceived mutual exclusivity between super-steep and non-hysteretic switching when both the on- and off-states are in the NC regime, through an effect described as complementary capacitance matching (CCM).

Furthermore, what has been missing to-date is an accurate analysis of the transient performance potential of NCFETs. Although efforts have been made on this topic [4], [12]–[20], they generally fall into two categories: 1.) assessment of polarization switching speed (*dP/dt*); 2.) AC circuit analysis enabled by either spice model fitting to DC NCFET TCAD or hardware data or self-consistent solving of the Landau-Khalatnikov (L-K) equation with a compact FET model [12], [21]–[23]. Regarding 1.), work to-date on this topic [4], [14]–[20] has been mostly based on full polarization switching of MFM (metal/ferroelectric/metal) capacitors and are thus contextually inaccurate for NCFETs, as the results describe the average switching speed over a full P-E loop rather than the average over some fraction of an S-curve defined by the voltage window used and the capacitance matching achieved for a particular sample. Other experimental work based on a contextually relevant FE/DE stack [4], [16] either does not adequately describe the extent of capacitance matching (*i.e.*, is the device operating non-hysteretically and therefore in the S-curve regime, or hysteretically and therefore in a minor- or full-P-E loop regime) or the dependence of *dQ/dt* on capacitance matching, voltage window, or material selection. Regarding 2.), compact modeling methodology is simply assumed to equally apply to NCFETs and conventional FETs [12], [21]–[23]; however, such an assumption is potentially risky. Instead, TCAD is used explicitly to simulate the transient behavior of NCFETs, and the results suggest a need for new types of compact models which can accurately capture transient changes in capacitance matching. If this is not captured, then existing compact modeling methods run the risk of over-estimating the power/performance characteristics of NCFET logic.

In Section II, the device structure and modeling assumptions are presented. In Section III, the effect of junction engineering on the trade-off between short channel effects and improved capacitance matching is evaluated using TCAD. In Section IV, a complementary pair of NCFETs are modeled and its impact on DC performance is evaluated using TCAD. In Section V, the AC behavior of DC-optimized NCFETs, applied to a simple inverter, is evaluated using TCAD. In Section VI, the AC behavior of NCFET ring oscillators (ROs), treated here as a delay chain, is evaluated using TCAD. Section VII concludes this study.

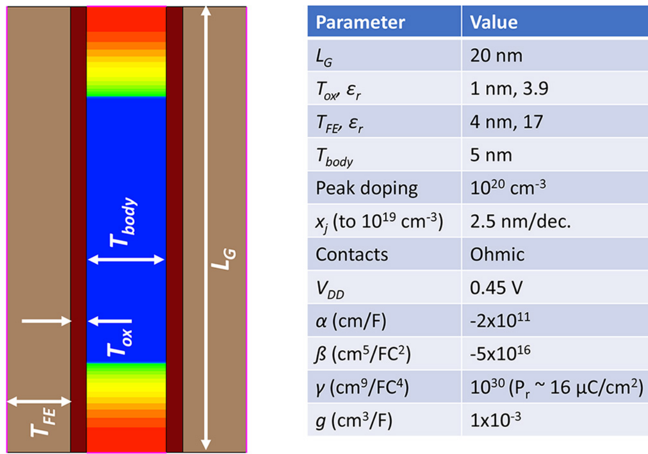
II. MODELING SETUP AND ASSUMPTIONS

A relatively simple yet insightful modeling approach is employed in this study. Sentaurus Device [24] is used to self-consistently solve the 1-D Landau-Khalatnikov (L-K) equation (Equation (1)) with Poisson's equation. Although this is treated as a DC study, the simulation setup is a transient simulation with a slow (5 ms) rising/falling edge.

$$E = 2 \propto P + 4\beta P^3 + 6\gamma P^5 - 2g\nabla^2 P + \rho\frac{dP}{dt} \qquad (1)$$

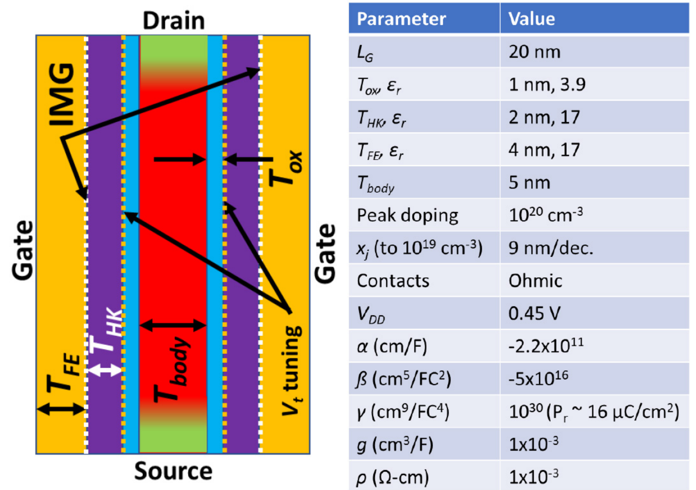
A "barebones" 2-dimensional double-gate MFIS (metal/ferroelectric/insulator/semiconductor) NCFET (Fig. 2) is modeled for the DC study, with structural and material parameters also defined in Fig. 2 (unless otherwise noted) for the DC component of this study. The point here is to extend every possible benefit of the doubt to NCFETs, no matter what the literature of the moment claims is possible or realistic, in order to determine whether and to what extent deeper design considerations persist even in the most ideal case with the most ideal materials and process engineering. There is no source/drain flaring, to remove any impact of 2-D fringing fields, which does not aid fundamental learning here. The L-K parameters are unbound to any particular material demonstrated in practice (although within range [2], [3], [5], [7]), in order to independently evaluate the impact of remnant polarization (P_r by varying γ, being higher as γ drops) and C_{NC} (by varying α, being higher as $|\alpha|$ drops) on NCFET design and performance. It is emphasized that FE $\varepsilon_r = 17$ and $T_{FE} = 4$ nm is electrostatically equivalent to $\varepsilon_r = 34$ and $T_{FE} = 8$ nm, which is more in line with FE layers having large P_r [2] but requires fewer TCAD mesh points. Ferroelectric parameters α and γ, respectively, are used to modulate C_{NC} and remnant polarization (P_r). Charge traps are ignored, again assuming a perfectly ideal ferroelectric. Junction profiles are defined analytically as Gaussian profiles with variable decay length x_j (defined from 10^{20} to 10^{19} cm^{-3} doping, with 10^{20} cm^{-3} peak doping at the contact interface) and ohmic contacts are assumed.

This work assumes single domain ferroelectrics but is arguably applicable to multi-domain as well. Much work



Parameter	Value
L_G	20 nm
T_{ox}, ε_r	1 nm, 3.9
T_{FE}, ε_r	4 nm, 17
T_{body}	5 nm
Peak doping	10^{20} cm^{-3}
x_j (to 10^{19} cm^{-3})	2.5 nm/dec.
Contacts	Ohmic
V_{DD}	0.45 V
α (cm/F)	-2×10^{11}
β (cm^5/FC^2)	-5×10^{16}
γ (cm^9/FC^4)	10^{30} (P_r ~ 16 μC/cm^2)
g (cm^3/F)	1×10^{-3}

FIGURE 2. **MFIS (metal/ferroelectric/insulator/semiconductor) example of simulated NCFET structure and corresponding structural and material parameter values.**



Parameter	Value
L_G	20 nm
T_{ox}, ε_r	1 nm, 3.9
T_{HK}, ε_r	2 nm, 17
T_{FE}, ε_r	4 nm, 17
T_{body}	5 nm
Peak doping	10^{20} cm^{-3}
x_j (to 10^{19} cm^{-3})	9 nm/dec.
Contacts	Ohmic
V_{DD}	0.45 V
α (cm/F)	-2.2×10^{11}
β (cm^5/FC^2)	-5×10^{16}
γ (cm^9/FC^4)	10^{30} (P_r ~ 16 μC/cm^2)
g (cm^3/F)	1×10^{-3}
ρ (Ω-cm)	1×10^{-3}

FIGURE 3. **MFMIS NCFET structural and material parameter details. The external gate electrode and floating IMG are set to the same workfunction between the NFET and PFET, while a floating V_t tuning electrode is used to independently modulate NFET and PFET V_t as a simple emulation of dipole tuning.**

has been published on the effect of multiple domains on NCFETs [25]–[29]. At a high level, though, both single- and multi-domain ferroelectrics will exhibit an S-curve relationship between polarization charge and electric field, when placed in series with a dielectric layer, in order to access the negative capacitance regime. Thus, to a first order, the use of single- or multi-domain ferroelectrics in a modeling study such as this will not impact the executive conclusions about junction design, capacitance matching, complementary operation, etc.

For MFMIS NCFETs and for the transient component of this study, the structure and material details shown in Fig. 3 (unless otherwise noted). Technically, the structure is actually MFMIMIS, with an additional floating internal gate inserted to provide a simple means of V_t tuning without adding modeling complexity associated with explicitly modeling fixed oxide charge or interface dipoles. This is treated as equivalent to MFMIS as it has no impact to FET behavior, since non-uniform field screening to the FE layer is agnostic to how many floating electrodes separate it from the channel. The assumption of $\rho = 10^{-3}$ Ω-cm is one decade lower than the recommendation from [15] for THz switching. This value is chosen to presumably decouple any ferroelectric switching speed limitation (which can distort the S-curve and therefore capacitance matching [19]) from other design criteria which may arise as a result of this study (although, as will be shown, even this low value is too large under certain conditions). Although [30] reported empirically that MFIS should produce superior AC performance to MFMIS for a discrete PFET, it was in a multi-domain context (*i.e.*, very large L_G) without CCM and furthermore does not imagine what is possible if ρ is not a bounding parameter, as that study is necessarily bound by the current state of hardware. Here, MFMIS is chosen explicitly due to the CCM-derived advantage to DC performance.

III. JUNCTION DESIGN IMPLICATIONS

Fig. 4 shows the minimum SS vs. x_j and P_r for a MFIS NCFET, assuming constant α and independently tunable γ. There are two regimes of junction design for NCFETs. The first regime is with relatively low P_r, wherein the voltage window for amplification due to the NC effect is small and in the off-state where capacitance matching is poor (Fig. 5, blue curve with solid red curve representing low C_{ov}). In the on-state (dashed red curve), the load line intercept is already in or near the positive capacitance (PC) regime, due to a low critical polarization field E_{crit}, where there is no amplification. This results in lower peak amplification, in turn favoring sharper/shallower junctions as with conventional MOSFETs, to minimize short channel effects (SCE). This is consistent with [31] and, in this regime, the NC entitlement is not fully realized. However, in the second regime (Fig. 5, black curve with solid red curve representing high C_{ov}), P_r (and, correspondingly, E_{crit}) is high enough such that the load line intercept for a FET with high junction overlap is still in the NC regime in the off-state. Here, the effect of broader junctions on capacitance matching in the off-state outweighs classical SCE for a net reduction in SS. This was also shown briefly in [32] with $P_r \sim 10$ μC/cm^2, but without any investigation into the P_r dependence.

There are some important implications to the preference for broader junctions here. First, NCFETs are not a simple "plug and play" into existing CMOS technologies, which are optimized with shallow/sharp junctions and at considerable development cost, to optimize the trade-off between SCE and external resistance (R_{ext}). This partially explains the sub-optimal DC parametric and AC NCFET performance reported in [5] and means NCFETs must either 1.) be a full replacement technology vs. conventional CMOS; 2.) impose additional cost to co-integrate conventional CMOS with

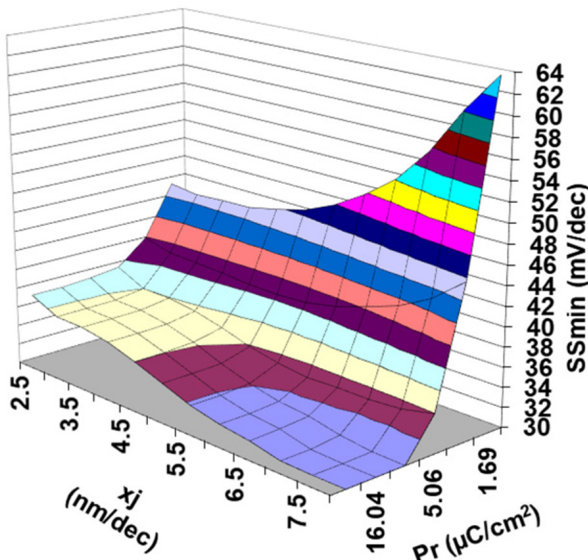


FIGURE 4. Surface plot of (non-hysteretic) minimum SS vs. P_r vs. x_j for a MFIS NCFET. At low P_r, small x_j is preferable. At high P_r, large x_j is preferable.

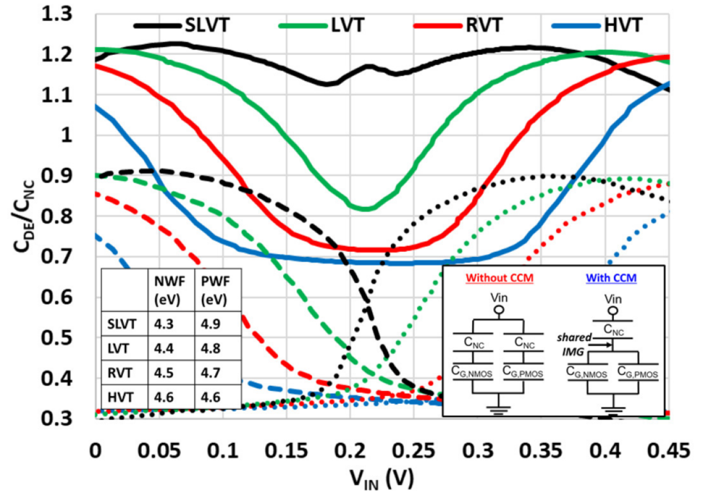


FIGURE 6. C_{DE}/C_{NC} vs. V_{IN} for a complementary MFMIS NCFET arrangement, with a FE(4nm)/HK(2nm)/IL(1nm) gate stack and $\alpha = -2.4x10^{11}$ cm/F. V_t is modulated by changing WF at a floating HK/IL interface (table on lower left inset) to emulate an interface dipole. Solid curves show C_{DE}/C_{NC} for a CCM pair. Dashed and dotted curves show the discrete PFET and NFET C_{DE}/C_{NC}, respectively (corresponding circuit diagrams in inset).

	NWF (eV)	PWF (eV)
SLVT	4.3	4.9
LVT	4.4	4.8
RVT	4.5	4.7
HVT	4.6	4.6

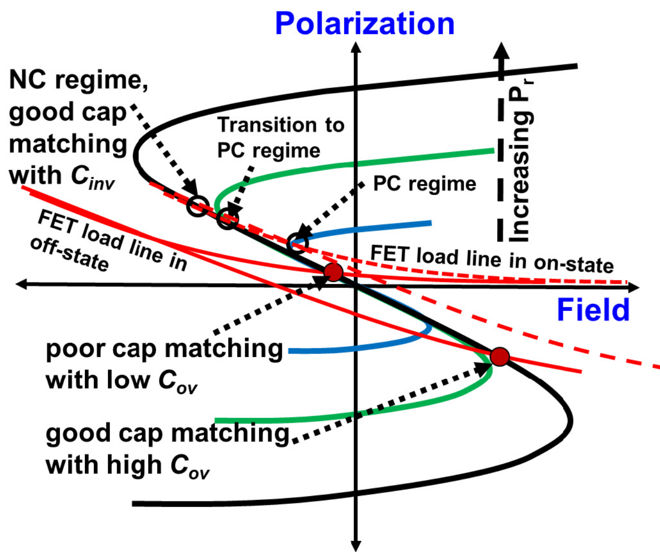


FIGURE 5. Illustrative ferroelectric-dielectric load lines for a NCFET with low and high C_{ov} (i.e., small x_j vs. large x_j, respectively).

optimally-designed NCFETs; 3.) employ some other design trick/innovation to achieve comparably low SS on NCFETs with shallow junctions as with broad junctions. In the optimistic case of the first scenario, NCFETs provide opportunity to trade technology development cycles between junction optimization and ferroelectric materials development, and/or to trade junction profile for gate stack reliability, by expanding the thermal budget (*i.e.*, a larger thermal budget can be used in the gate stack module to broaden the junctions appropriately while also increasing gate stack reliability). Precisely because the preferred junction profiles for NCFETs are broad, fewer learning cycles can be spent to define junctions more amenable to optimal NCFET performance, thus mitigating additional development cost associated with incorporating new materials into an advanced CMOS process.

A caveat to this preference for broader junctions is the apparent requirement for large P_r in order to realize the full NC entitlement. This is a problem if the series dielectric has maximum allowable charge $Q_{max} < P_r$, with Q_{max} defined as $\varepsilon_r\varepsilon_0$ E_{br}, where $\varepsilon_r\varepsilon_0$ is the dielectric permittivity and E_{br} is the dielectric breakdown field. Although SiO_2 has high $E_{br} \sim 10$ MV/cm, it has a low dielectric constant ($3.9*\varepsilon_0$) and so $Q_{max} \sim 3.45$ μC/cm^2. This would restrict NCFETs containing SiO_2 in the gate stack to the shallow junction regime (Fig. 4). Higher-k dielectrics have higher Q_{max}, but poorer interface quality to Si channels, so either alternate channel materials must be combined with high-k gate dielectrics (oxide-less) and/or some design trick must be realized in order to enable oxide dielectrics with high-P_r ferroelectrics without compromising reliability. This engineering challenge is henceforth ignored to gain deeper insight.

IV. COMPLEMENTARY NCFET LOGIC

A common approach toward modeling transistors is to treat them in isolation; however, this does not accurately represent MFMIS NCFET logic behavior, owing to the influence of complementary capacitance matching (CCM). In a logic gate, the NFET and PFET gate share the same gate finger, which also means a shared internal metal gate (IMG). This IMG is equipotential and therefore the capacitance as seen by the logic gate input $C_{IN} = C_{NC}*(C_{NFET} + C_{PFET})/(C_{NC}$

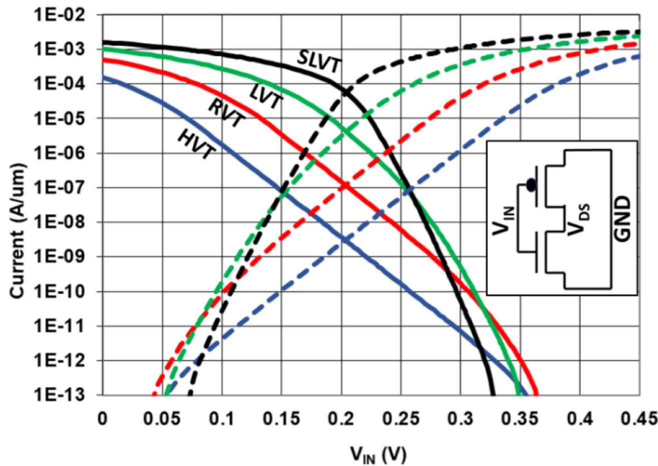


FIGURE 7. IDVG curves of the same complementary MFMIS NCFET arrangement from Fig. 6.

$+ C_{NFET} + C_{PFET}$). This is CCM (*i.e.,* C_{DE} is the parallel sum of C_{NFET} and C_{PFET} and is what matches to C_{NC}) and results in a C_{DE}/C_{NC} vs. V_{IN} curve that looks relatively flat, because the PFET is off while the NFET is on and vice versa (Fig. 6, solid curves). In a CMOS context, it can therefore be expected that PFET C_{inv} matching to C_{NC} will reduce NFET *SS* and vice versa, thus extending the usable capacitance matching for a given FET into both the on-state and off-state regimes. Furthermore, in CCM the maximum $C_{DE} = C_{inv,NFET} + C_{ov,PFET}$ or $C_{inv,PFET} + C_{ov,NFET}$, for high and low V_{IN}, respectively, as opposed to only $C_{inv,NFET}$ or $C_{inv,PFET}$ for the discrete (non-CCM) case. This enables C_{DE} to more closely approach C_{NC} for higher internal voltage gain. The extent of CCM on reducing *SS* depends on whether the NFET/PFET pair is a low-V_t pair or a high-V_t pair. A low-V_t pair has more NFET + PFET *C-V* curve overlap and therefore a flatter C_{IN} vs. V_{IN} curve (Fig. 6), leading to steeper *SS* for each of the NFET and PFET (Fig. 7). This is a benefit to high performance computing (HPC), which employs a larger balance of low-V_t FETs.

Combining CCM with broad junctions increases C_{DE}/C_{NC} in the PFET-to-NFET transition region of the V_{IN} sweep, to the point wherein a near-perfect switch with non-hysteretic $SS < 5$ mV/dec over 6+ decades is at least theoretically possible (Fig. 8a). Internal voltage gain follows C_{DE}/C_{NC} as in Fig. 8b, peaking at ~ 100 V/V at $x_j = 9$ nm/dec. $> 1{,}000$ V/V (technically infinite, but resolution-limited) is achieved with $x_j = 10$ nm/dec (Fig. 8b inset); however, this case is hysteretic as indicated in Fig. 8b where the forward and reverse sweeps separate by ~ 26 mV at the mid-point of the V_{IN} sweep (some separation also occurs at $x_j = 9$ nm/dec, but it is much smaller at ~ 4 mV). C_{DE}/C_{NC} (and voltage gain) actually drops in the on-state (*i.e.*, at $V_{IN} = 0$ V and V_{DD}) with larger x_j. This is because the FE/DE load line intercept is closer to the NC-to-PC transition (*i.e.*, E_{FE} approaches E_{crit}), where the P-E curvature increases C_{NC}, thereby reducing C_{DE}/C_{NC}.

This combination of low V_t and large x_j has limited compatibility across a full V_t menu (Fig. 9), though, owing to the effect of increased internal voltage gain on reducing V_t, and so for broad enough junctions combined with CCM, there is no distinction between the high-V_t and low-V_t devices. Thus, CCM is best suited for low-V_t pairs, while high-V_t pairs, which are more common in low power computing (LPC - mobile, SoC, IoT, etc.), benefit less. Nonetheless, it is shown clearly here that CCM with MFMIS CMOS breaks the existing perception of mutual exclusivity between super-steep and non-hysteretic switching. It is also noteworthy that $C_{DE}/C_{NC} > 1$ (Figs. 6 and 8) and yet hysteresis remains low, albeit non-zero. This is because peak C_{DE}/C_{NC} is only over a portion of the V_{IN} sweep. From Fig. 8(a) inset, C_{DE}/C_{NC} starts off as > 1, then drops to < 1, then returns to > 1, for $x_j = 2.5$ nm/dec, while the opposite is the case for $x_j = 9$ nm/dec. For the latter case, this confines the full DE load line to the NC regime despite some fraction of that load line exhibiting $C_{DE}/C_{NC} > 1$. For the former case, the DE load line does intercept the FE in the PC regime with $C_{DE}/C_{NC} \sim 1.2$, but as Fig. 8(b) inset suggests, significant hysteresis occurs beyond $C_{DE}/C_{NC} \sim 1.3$.

A requirement for CCM in MFMIS CMOS is that the IMG workfunctions (WF) of the NFET and PFET are matched (the external gate contact is assumed as having the same WF already). Otherwise, the NFET and PFET load lines intersect the shared ferroelectric S-curve at different polarization *P*, which sum together to define the total *P* at the shared IMG. This averages out any WF difference and distorts the apparent S-curve as seen by the input, in turn increasing the apparent C_{NC} and therefore degrading capacitance matching (Fig. 10). On the other hand, if the shared IMG has the same WF on the NFET and PFET, this results in a high-Vt pair and therefore reduced CCM. In order to fully leverage CCM with a shared WF IMG, there are two options for V_t modulation: 1.) interface dipole engineering [33], [34] and/or oxygen vacancy modulation [35] across the V_t menu; 2.) different junction profiles across the V_t menu (Fig. 8a, broader for low-V_t, shallower for high-V_t). In either case, *SS* would not be constant across the V_t menu, being higher for high-V_t and lower for low-V_t. This can be a problem if high-V_t is used to reduce standby power consumption, as the low-V_t device may actually exhibit lower leakage as in Fig. 7. In such a case, low-V_t would be more favorable, but at the expense of thermal management. If instead high-V_t is used to reduce dynamic power consumption, then to a first order, non-uniform *SS* across the V_t menu is not an issue.

Another caveat with MFMIS NCFETs is leakage-induced drift and instability [36], which is avoided with MFIS NCFETs. However, complementary MFIS NCFETs (Fig. 11) behave differently from MFMIS NCFETs, owing to the lack of an IMG. This isolates the internal gate potentials of the NFET and PFET. Any CCM is therefore limited by polarization gradient coupling coefficient (g) and

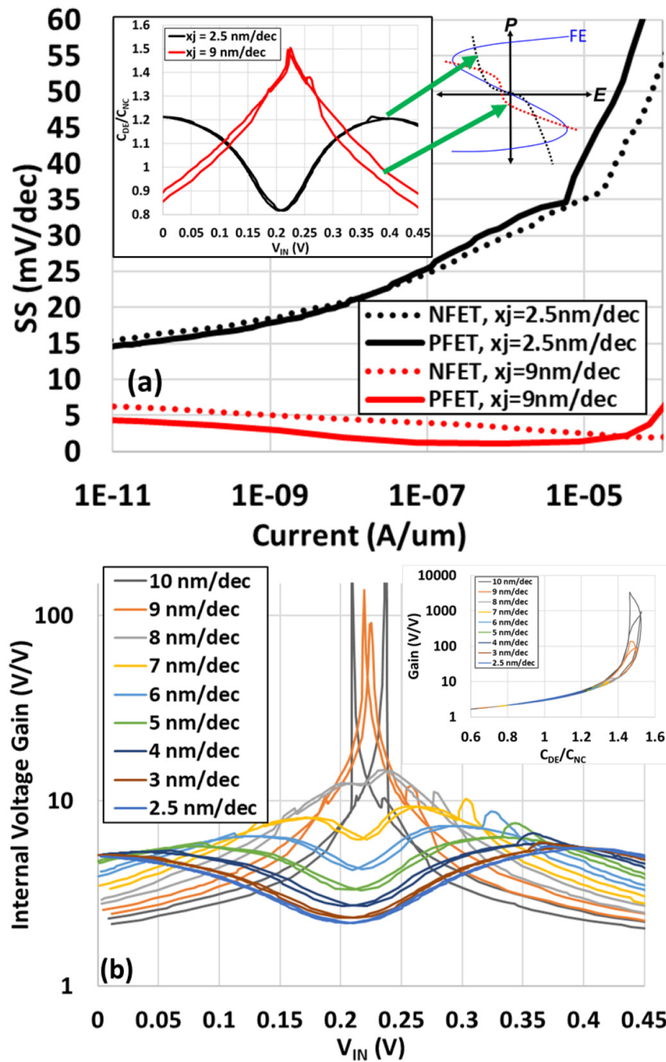


FIGURE 8. *SS* vs drain current of complementary LVT MFMIS NCFETs (as in Fig. 7) for shallow and broad junctions. (inset) Forward + backward sweeps of C_{DE}/C_{NC} vs. V_{IN} with illustrative DE/FE loadline. (b) Forward + backward sweeps for internal voltage gain vs. V_{IN} across varying x_j for complementary LVT MFMIS NCFETs (as in Fig. 7). (inset) Internal voltage gain vs. C_{DE}/C_{NC} across varying x_j.

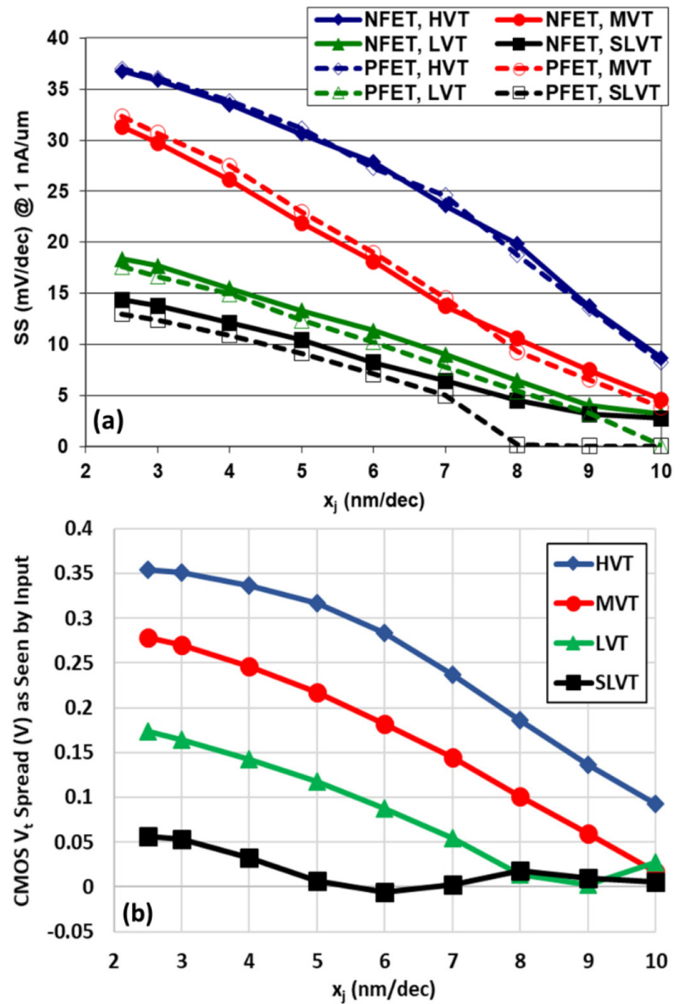


FIGURE 9. (a) *SS* vs. x_j for complementary MFMIS NCFETs with different V_t pairs, as in Fig. 7. Most cases are non-hysteretic (< 15 mV). Hysteresis exists where *SS* = 0. (b) V_t spread (difference between NFET and PFET V_t in Fig. 7) vs. x_j for complementary MFMIS NCFETs with different V_t pairs. V_t is extracted using the maximum transconductance method.

NFET/PFET spacing L_{iso} (Fig. 12, in order of green black red blue curves). High g and small L_{iso} are necessary for MFIS CMOS to leverage CCM. This allows the NFET and PFET internal potentials to "talk" through the shared FE but requires a degree of material engineering and layout patterning which may not be possible. Thus, MFIS CMOS is realistically limited to long-range coupling in layouts with shared gate fingers, owing to how the active regions are patterned (e.g., minimum single fin separation results in minimum L_{iso} = fin pitch). This, in turn, means less CCM compared to MFMIS CMOS, which is not limited by either of g or L_{iso} due to the equipotential IMG.

A more plausible approach to MFIS CMOS is to simply isolate the NFET and PFET from each other entirely, which includes cutting the shared gate finger such that the ferroelectric is not shared between them. The advantage here is that broader junctions may be employed than in MFMIS CMOS, in lieu of CCM, in order to achieve steeper *SS*. This is beneficial for thermal budget design space and gate stack reliability, as mentioned previously, while also removing CCM dependence on variation in g (e.g., grain orientation variation) and L_{iso} (e.g., logic cell height). However, disadvantages include: 1.) CCM is not possible (degraded lower *SS* limit); 2.) separate gate contacts (or a single, wider contact extending over an active gate cut region) are preferred for NFET and PFET in order to eliminate any parasitic FE cross-talk between NFET and PFET, resulting in a circuit density penalty unless the gate contact can be reliably placed over the active region.

V. AC BEHAVIOR OF SINGLE INVERTER

A key component to evaluating transient performance is to properly account for the Miller Effect (Fig. 13), which

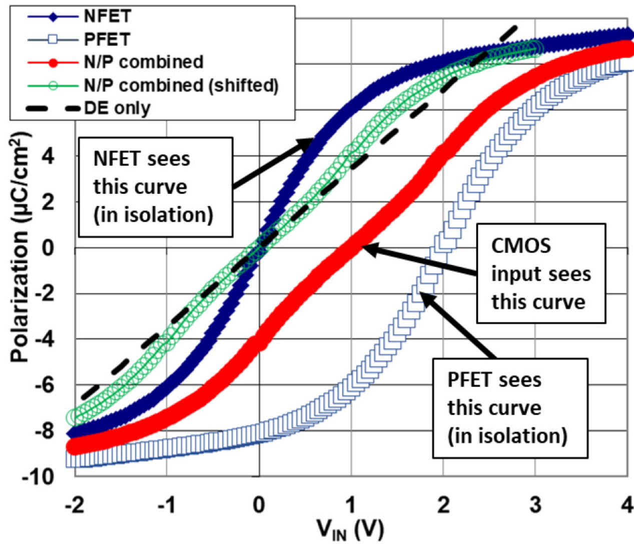


FIGURE 10. Polarization vs. V_{IN} as modeled with the 1-D L-K equation and parameters in Fig. 2. A load line shift of 2 V is applied between the NFET and PFET, to accentuate the distorted apparent S-curve as seen by the input when the NFET and PFET have different IMG WF. In this example, dP/dV_{IN} is comparable between the DE only case (black dashed line) and the FE/DE CMOS pair (green curve, which is the red curve shifted back to directly compare to the DE only case), implying little to zero voltage amplification.

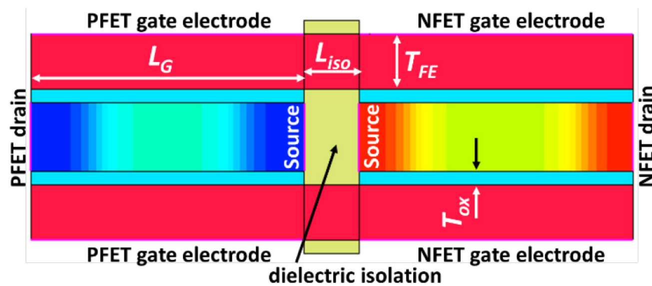


FIGURE 11. Complementary MFIS simulation structure. NFET and PFET are separated by dielectric isolation of length L_{iso} which is treated here as a proxy for vertical N-to-P spacing in the cell height direction (into the page if a 3D simulation). The ferroelectric layer is continuous across the NFET, isolation, and PFET. PFET parameters are the same as NFET as described in Fig. 2, albeit with opposite polarity doping. PFET and NFET drain are biased to $+V_{DS}$, with the source grounded and gate electrodes treated as a common node in simulation, but with independently tunable WF.

increases the capacitance between two circuit nodes when the voltage at each node is changing in the opposite direction at high speed (e.g., one increases while the other decreases, such as the input and output nodes of an inverter). For instance, one might start with either of measured MFIS NCFET I-V and C-V curves or TCAD-generated curves of the same kind, and then fit a compact model to these curves, and then simulate a RO or logic block using spice simulation. As these curves are all generated in a DC context, they cannot capture the dynamic change in capacitance matching as a function of switching speed, owing to the Miller Effect. This can result in erroneous predictions for NCFET AC performance, and furthermore an erroneous understanding of

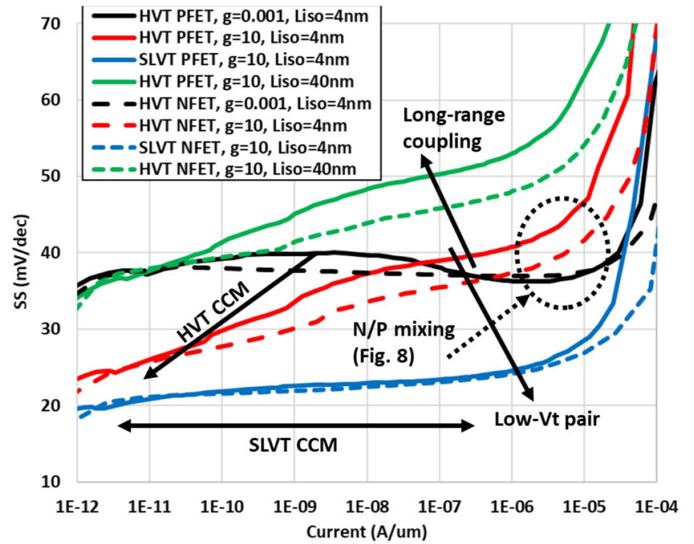


FIGURE 12. SS vs. current for complementary HVT and SLVT MFIS NCFET pairs. $\alpha = -1.8x10^{11}$ cm/F. Increasing g from 0.001 cm^3/F to 10 cm^3/F improves ferroelectric domain coupling, resulting in higher CCM; however, larger L_{iso} degrades CCM due to longer range coupling. This is problematic for HVT, which has degraded SS (due to less CCM) at higher current. Also, some degrade in SS at higher current arises from the apparent load line effect as in Fig. 8. Maximizing CCM in MFIS CMOS not only requires a low-V_t pair, but also high g and very small L_{iso}.

what design point is actually non-hysteretic in AC (notwithstanding the effect of switching speed on the P-E loop and S-curve [19]). Some studies [12], [21]–[23] have self-consistently solved the L-K equation with a separate compact FET model, connected through an equipotential internal circuit node. This should presumably produce an accurate result for MFMIS, which has an equipotential internal metal gate (IMG); however, compact FET models are typically poorly equipped to handle changes in junction profile, for instance lacking a perfect physical partitioning between inner fringe and direct overlap capacitances as well as their bias dependencies beyond a "good enough" model fitting. The TCAD simulation presented herein makes no such assumption, although in principle both approaches should produce an equivalent result.

Fig. 13a shows a simple case of a single, unloaded inverter with an input ramp rate varying between 5 ms and 5 ps. This clearly illustrates the Miller Effect, which increases C_{DE}/C_{NC} during high frequency AC operation, wherein C_{DE} is the dielectric capacitance (measured as dQ/dV between the shared IMG and the inverter output) and C_{NC} is the absolute value of the negative capacitance portion of the ferroelectric capacitance (measured as dQ/dV between the input and the shared IMG), which can also be expressed as abs(C_{FE}). The impact to switching current is the result of a trade-off between hysteresis and capacitance matching (Fig. 13b). At small abs(α), $C_{NC} >> C_{DE}$ and so capacitance matching is poor and hysteresis is very low. Even in this regime, though, the Miller Effect reduces the C_{NC}-to-C_{DE} offset and improves capacitance matching at high switching speeds.

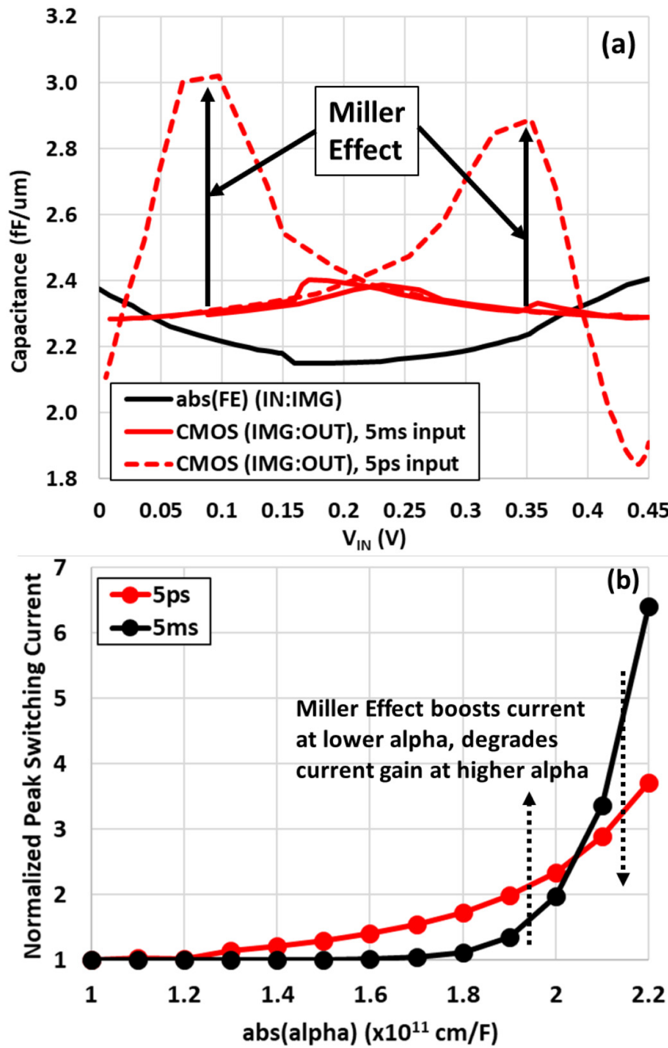


FIGURE 13. **(a) Capacitance vs. V_{IN} for a single, unloaded MFMIS NCFET inverter with CCM varying input ramp rates. (b) Normalized peak switching current vs. α with varying input ramp rates.**

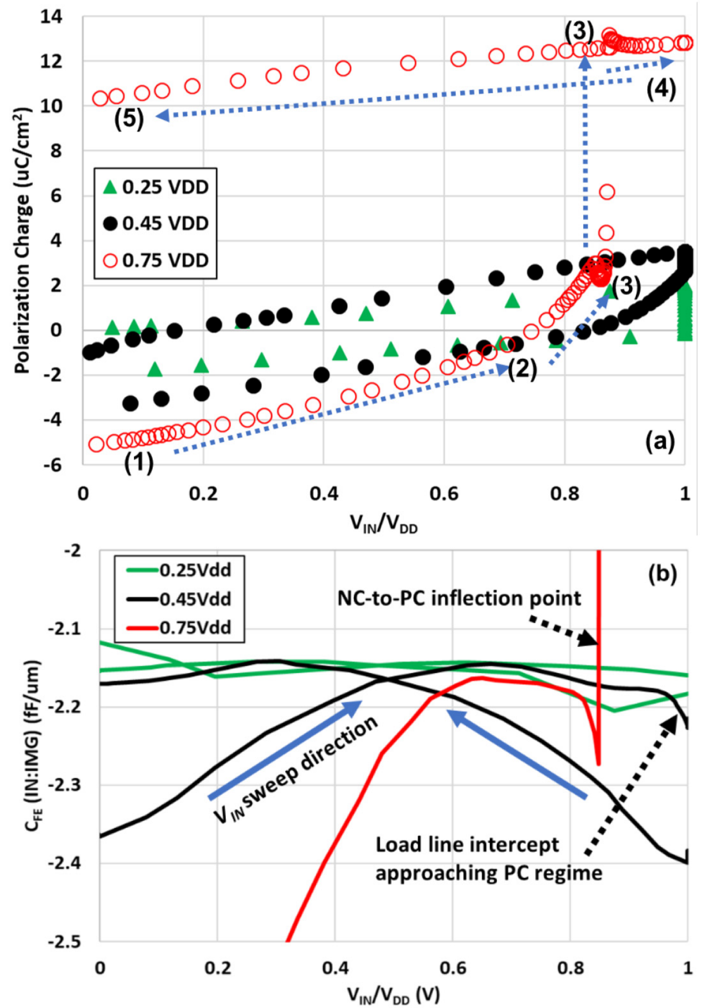


FIGURE 14. **(a) Polarization charge vs. V_{IN}/V_{DD} and (b) C_{FE} vs. V_{IN}/V_{DD} at varying V_{DD}, for a single, unloaded MFMIS NCFET inverter with CCM and a 5 ps input ramp rate.**

This simultaneously increases switching current while reducing the threshold for onset of hysteresis (*i.e.*, hysteresis will occur at smaller abs(α)). As abs(α) increases, switching current continues to rise as C_{NC} reduces and approaches C_{DE}; however, at some point the AC hysteresis is large enough such that the rate of increase in switching current with abs(α) is exceeded by that in the slow switching speed case. DC hysteresis is also present (*i.e.,* 5 ms sweep), although the abs(α) threshold for this is higher. This is because C_{DE}/C_{NC} is always lower in DC than AC, due to a lack of Miller Effect, and so hysteresis is lower for the same abs(α). Thus, the full DC entitlement of NCFETs is not realized in AC with what is otherwise a DC-optimal design which uses a higher abs(α).

Another implication of the Miller Effect is the transition to polarization switching at higher V_{DD} and higher abs(α) and how this limits the usable voltage window for NCFETs during fast switching. Fig. 14a shows the evolution of FE polarization charge throughout a high-speed switching event for a below-threshold condition (0.25 V_{DD}), near-threshold condition (0.45 V_{DD}), and above-threshold condition (0.75 V_{DD}). At 0.25 and 0.45 V_{DD}, the switching is hysteretic, but remains in the NC regime for both the forward and backward sweeps, as indicated by the ferroelectric capacitance (C_{FE}) in Fig. 14b being mostly flat and negative throughout the V_{IN} sweep. As V_{IN} increases, the FE/DE load line intercept approaches the positive capacitance (PC) regime. At the NC-to-PC inflection point, the NC slope increases toward $-\infty$ and then settles at a positive value in the PC regime. At 0.45 V_{DD}, the FE/DE load line approaches this transition point but does not cross it. However, at higher V_{DD}, (e.g., 0.75 V_{DD} in Fig. 14b), this transition occurs and drives an onset of polarization switching. This would not occur in DC, as C_{DE} is either greater than or less than C_{NC}, and under the right conditions can lead to non-hysteretic switching. However, in AC operation,

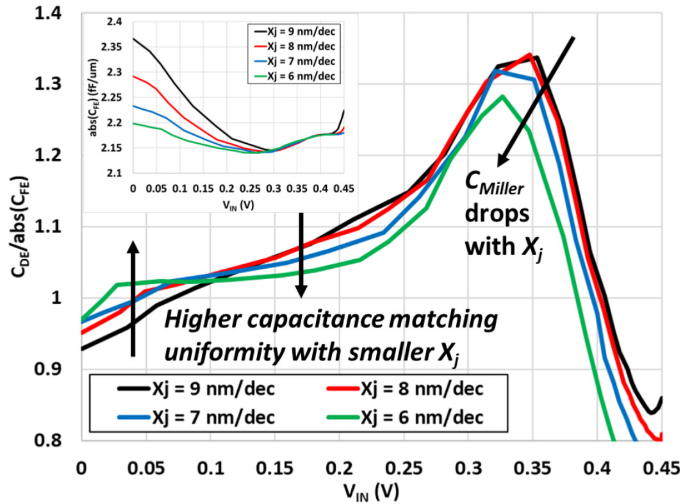


FIGURE 15. C_{DE}/abs(C_{FE}) vs. V_{IN} with varying x_j, for a single, unloaded MFMIS NCFET inverter with CCM and a 5 ps input ramp rate, for a rising edge input. (inset) abs(C_{FE}) vs. V_{IN} with varying x_j for the same MFMIS NCFET inverter.

the Miller Effect causes C_{DE} to sharply rise and then drop, driving a sharp increase in polarization current (*dP/dt*). As V_{IN} is ramped toward V_{DD}, C_{DE} starts off as $< C_{NC}$, representing point (1) in Fig. 14a. Since V_{IN} ramps quickly, the Miller Effect results in $C_{DE} > C_{NC}$ and peaks at point (2). As Fig. 14b shows, the device is still in the NC regime at this point. From point (2) to point (3), the Miller capacitance discharges, resulting in a rapid increase in polarization charge. Despite the small ρ of 10^{-3} Ω-cm, this increase in *dP/dt* exceeds the *dP/dt* limit of the ferroelectric, resulting in a compression of the S-curve and corresponding *P-E* loop [15]. As C_{DE} drops back below C_{NC}, the FE/DE load line intercept drives toward the NC-to-PC inflection point which, due to the high *dP/dt* coming from the Miller Effect, now occurs at a reduced electric field (*i.e.*, the critical field E_{crit} is reduced). At point (3), the load line intercept transitions into the PC regime, where it remains permanently as V_{IN} increases toward V_{DD} in point (4) and then is swept back to zero as in point (5).

It is noteworthy that, at 0.45 V_{DD}, C_{DE} also drops back below C_{NC} as V_{IN} approaches V_{DD} and yet only a minor hysteresis loop is realized rather than full polarization switching. This is because *dP/dt* remains below the *dP/dt* limit for the case modeled here. This is implied in Fig. 14a, where the slope of polarization charge vs. V_{IN}/V_{DD} in the forward sweep is lower than that for 0.75 V_{DD}. It is emphasized that what is observed here is specifically an AC effect, owing to the Miller Effect, and is why the AC simulations shown here have $\alpha = -2.2x10^{11}$ cm/F, whereas the DC cases for CCM with the exact same junctions and V_t pair have $\alpha = -2.4x10^{11}$ cm/F. Backing off of α (*i.e.*, increasing C_{NC}) achieves a usable V_{DD} window for high frequency AC operation without polarization switching (one can equivalently increase T_{ox} to achieve the same effect), for the ρ assumed here, because capacitance matching is degraded and so *dP/dt* from point (2) to point (3) in Fig. 14a is low enough to provide some window of operation. One might expect shallower junctions to achieve a similar effect, by reducing C_{ov} and therefore the Miller Effect; however, the net effect on performance is a trade-off between reduced capacitance matching to enable higher V_{DD} and the peak achievable I_{eff} at that higher V_{DD} but with degraded capacitance matching. Also, as Fig. 15 shows and as described earlier, smaller x_j still results in $C_{DE} > C_{FE}$ as V_{IN} approaches the rail voltage (either 0 V or V_{DD}, depending on the sweep direction), and over a larger portion of the V_{IN} sweep, because C_{NC} at the FE/DE load line intercept depends on x_j, being lower for smaller x_j (Fig. 15 inset). The reduction in Miller Effect with x_j is also small and so polarization switching for small x_j is perhaps an even higher risk than for larger x_j during AC operation, as the NC-to-PC transition occurs near the rail voltage and $C_{DE} > C_{FE}$ in this regime for small x_j. This will be revisited later.

VI. AC PERFORMANCE OF RING OSCILLATORS

ROs are simulated as a 6-stage delay chain with a single fanout (FO). DC-optimal NCFET performance does not directly translate to AC power/performance (Fig. 16). Although raw frequency (Fig. 5a) and AC I_{eff} (Fig. 16a inset) increase for both loaded and unloaded ROs relative to a conventional FET, power/performance is degraded in the unloaded case (Fig. 16b). The root cause is the very same capacitance matching that is a feature of NCFETs, which increases C_{eff}. A similar point was made in [23] regarding higher C_{eff} for NCFETs, although power/performance was not explicitly reported. There is also some enhancement of the Miller Effect (Fig. 16b inset) for NCFETs with CCM. Although [22] claimed a reduction in Miller Effect for NCFETs, here the opposite is demonstrated. This is rooted in CCM, wherein gate-to-drain capacitance C_{GD} as seen by the input is in parallel with C_{inv} of the opposing complementary FET, thus increasing the total capacitance which undergoes a Miller effect.

One might simply reduce the extent of capacitance matching, for instance by increasing C_{NC} (*i.e.*, lower abs(α) and/or larger FE-to-DE area ratio), to guardband against hysteresis and polarization switching while also reducing C_{eff} (Fig. 17a), but unloaded power/performance is always degraded (Fig. 17b) relative to a conventional FET reference with the same broad junctions. Shallow junctions further expand the NCFET power/performance deficit (Fig. 17). Loaded circuits exhibit the opposite relationship (Fig. 16), as C_{load} is a large fraction of the total C_{eff}, and so the stage delay depends more on I_{eff}. Loaded circuits also expand the operable V_{DD} window (Fig. 16a inset), as the reduced switching speed in a loaded circuit reduces *dP/dt*. One might also reduce the remnant polarization P_r (*i.e.*, increasing γ in the L-K equation), which restricts *dQ/dV* (and therefore C_{eff}) by forcing a transition to the PC regime in the on-state (and in the deep off-state); however, not only does this reduce I_{ON}

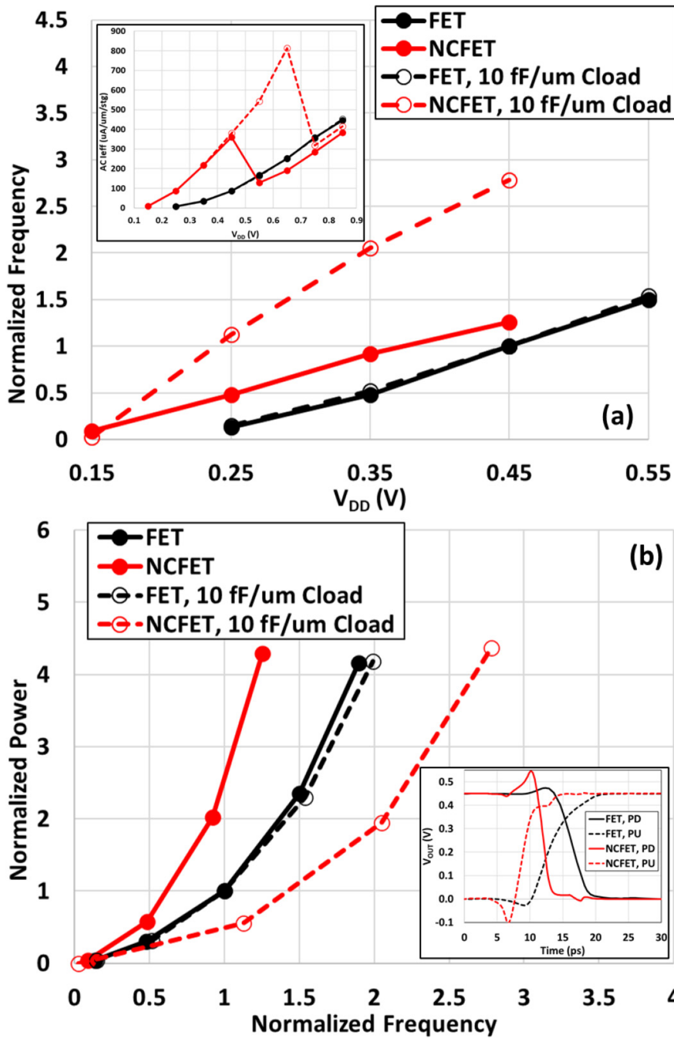


FIGURE 16. Normalized loaded and unloaded FO1 RO (a) performance, (inset) AC I_{eff} vs. V_{DD}, (b) power/performance for LVT MFMIS NCFETs vs. conventional FET reference with the same $x_j = 9$ nm/dec, and (inset) RO stage output voltage V_{OUT} vs. time for unloaded NCFET and FET RO, for both pull-up (PU) and pull-down (PD) events. Normalization is relative to the FET reference at $V_{DD} = 0.45$ V (both with and without C_{load}).

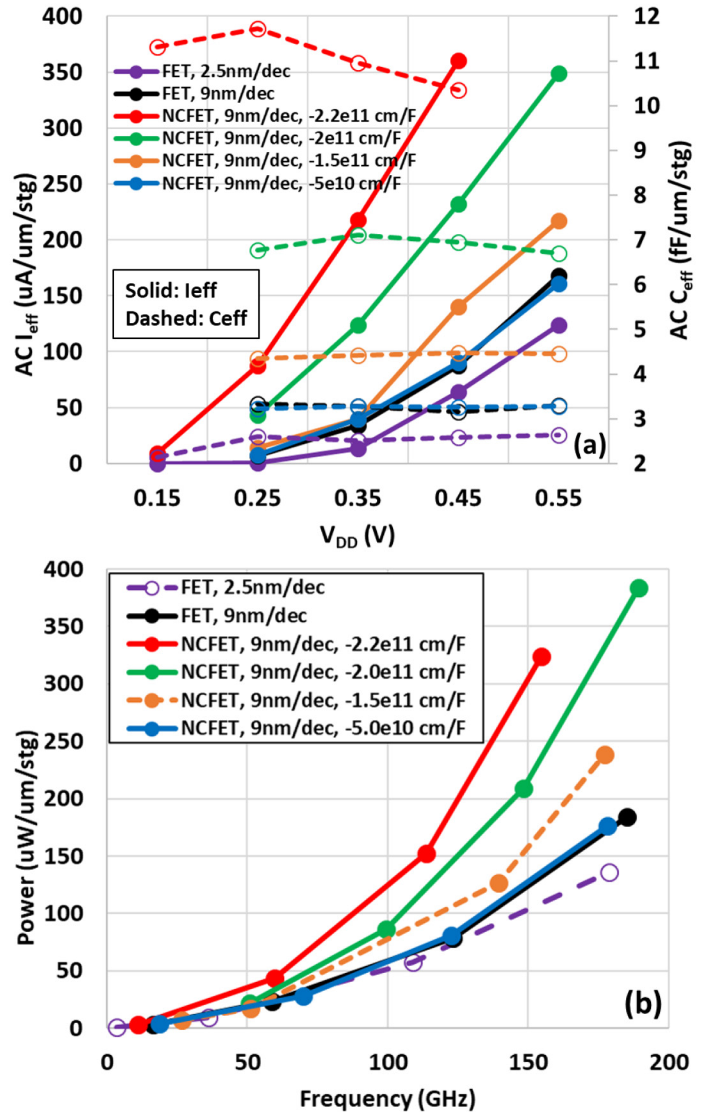


FIGURE 17. (a) AC I_{eff} and C_{eff} vs. V_{DD} for unloaded FO1 RO with CCM and varying α. (b) Unloaded FO1 power/performance for same case as Fig. 16, but with varying α. C_{eff} is derived from Q_{avg}/V_{DD}, where Q_{avg} is the dissipated charge during a switching event, averaged between a rising and falling edge, and comes from integrating the power rail current over the switching event.

and increase I_{OFF}, it also degrades SS and, for a DC-optimal design with $C_{DE} > C_{NC}$, it reduces the operable V_{DD} range in AC due to polarization switching (Fig. 18). This is opposite to lower abs(α), which also reduces C_{eff} but increases the V_{DD} window, as this does not reduce E_{crit} while smaller P_r does reduce E_{crit} at constant abs(α).

The results herein suggest there is not a single NCFET design point with CCM which can achieve an unloaded power/performance advantage over conventional FETs. The next question, then, is whether the DC-optimal x_j is also the AC-optimal x_j in this context. As shown in Fig. 19, reducing x_j does increase the operable V_{DD} window, but a power/performance improvement over a FET reference is only achievable in the polarization switching regime, either at small x_j over a broad V_{DD} range or at large x_j and high V_{DD}. In those regimes, the devices are basically no longer NCFETs, as polarization switching blocks access to the NC regime and so both C_{eff} and I_{eff} are much lower, due to what is essentially a thicker dielectric stack than the FET reference but without internal voltage amplification. It is only in the large x_j regime where significant improvements in standby power (Fig. 20) and current drive (Figs. 16–18) are possible, but no case so far shows an enhancement in unloaded circuit active power/performance over conventional FETs.

It would therefore appear that NCFETs designed for minimum SS are, at best, a *supplementary* CMOS technology and not a replacement CMOS technology, best used in heavily loaded circuit paths requiring high drive current (e.g., long signal propagation and/or high fan-out load). If a chip design

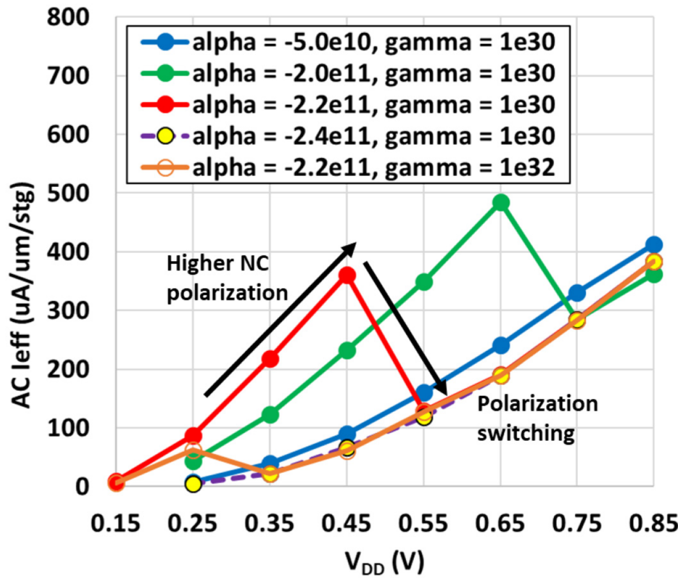


FIGURE 18. AC I_{eff} vs. V_{DD} for unloaded FO1 RO with CCM and varying α and γ. At larger abs(α), the operable V_{DD} window shrinks owing to polarization switching at high V_{DD}, as evidenced by the dramatic reduction in AC I_{eff} at higher voltage. The DC-optimal $\alpha = -2.4x10^{11}$ cm/F is inoperable under AC conditions, owing to polarization switching throughout the entire V_{DD} range. Increasing γ, which reduces P_r, also shrinks the operable V_{DD} window due to polarization switching. Here, $\gamma = 1x10^{32}$ cm^9/FC^4 corresponds to $P_r \sim 5$ μC/cm^2, while $\gamma = 1x10^{30}$ cm^9/FC^4 corresponds to ~ 16 μC/cm^2.

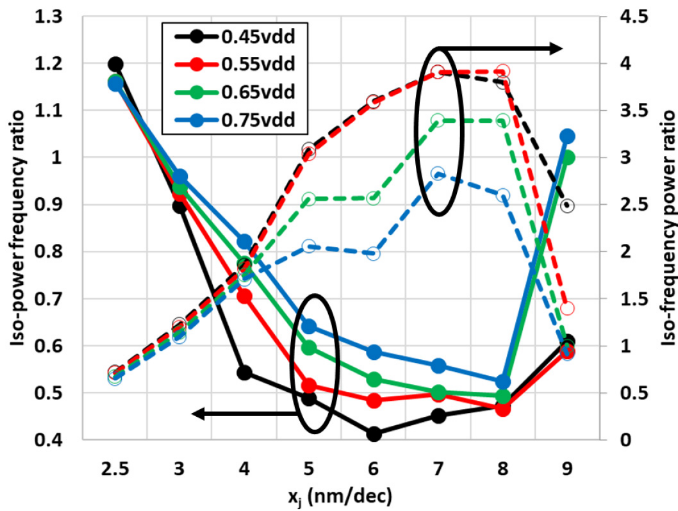


FIGURE 19. NCFET (with CCM) unloaded FO1 RO iso-power performance ratio and iso-performance power ratio vs. x_j and reference V_{DD}, relative to a FET reference with $x_j = 2.5$ nm/dec.

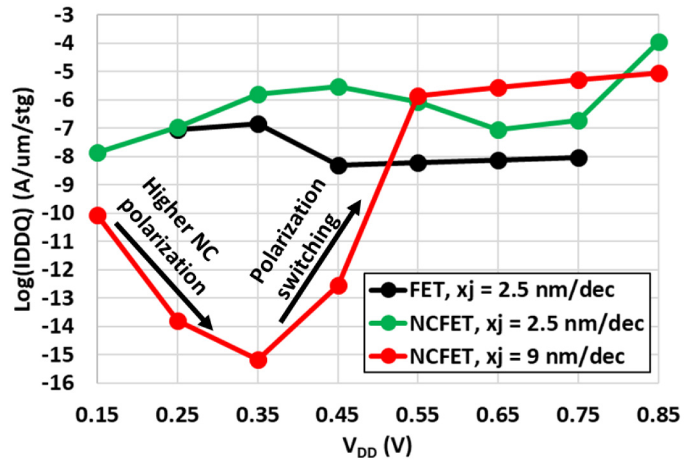


FIGURE 20. Log($IDDQ$) vs. V_{DD} for FO1 RO with either conventional FETs or NCFETs and varying x_j.

comprises more loaded than unloaded (or lightly-loaded) circuit paths, then a net power/performance improvement is possible with standalone NCFETs with CCM, as the sum of the relative power reductions in the loaded paths would more than offset the power increase in the unloaded paths. This may, for instance, be more likely in larger chips with longer maximum signal path lengths than smaller chips. One might also leverage NCFETs with CCM to intentionally slow down faster circuit paths (at iso-power) to reduce hold time violations between latches, which may prove more efficient than adding strings of large, power-hungry buffers to the same circuit path with conventional FETs. If, on the other hand, most circuit path lengths are short and with a small fan-out load, then NCFETs with CCM may not offer substantive value over conventional FETs.

Thus, the projected value of NCFETs with CCM in any chip design is not easily assessed using simple performance benchmarking techniques and would instead require a full Design Technology Co-Optimization (DTCO) study. However, comprehensively performing such a study requires a process design kit (PDK) comprising models for both conventional FETs and NCFETs to determine the appropriate mix, if any, so that foundry customers can pick and choose based on their design need. This would require either a full foundry commitment to FET and NCFET co-integration/compatibility (including the divergent requirements for junction design) or a pre-PDK analysis with some very clever model overrides (more likely, considering the need to further explore NCFET device and circuit co-optimization with efficient design cycle churn). Furthermore, such a supplementary role also implies the need for a usable V_{DD} window (which also informs the optimal degree of capacitance matching), which must be compatible with conventional FETs if both are on the same chip and share the same power grid. $V_{DD} < 0.5$ V is very difficult to achieve with conventional FETs and so co-existence with NCFETs will require some compromise in NCFET design and/or application, most likely in the form of a minimum circuit load requirement, reduced abs(α) (assuming FE layers can be carefully engineered), larger FE/DE area ratio, and/or increased T_{ox} relative to the FET counterpart.

VII. CONCLUSION

NCFETs have been evaluated in TCAD by studying the effect of junction profile and complementary operation

on DC design criteria. Two key design critera emerge: 1.) unlike conventional FETs, NCFETs can benefit from broader junctions; 2.) complementary MFMIS NCFET circuits furthermore benefit from CCM, especially for low-V_t pairs with shared WF IMG. Combining these two can result in a near-perfect switch with super-steep (< 5 mV/dec) non-hysteretic switching in DC. CCM is also possible with a complementary MFIS NCFET pair, but requires a degree of material engineering and patterning which may not be possible. Thus, MFIS CMOS is realistically not a beneficiary of CCM. Pragmatically speaking, though, it is likely that the earliest adoption of NCFETs into a technology platform would invoke MFIS over MFMIS, as it is less disruptive and offers at least some entitlement over conventional CMOS. However, as has been shown here, the "ultimate" theoretical variant appears to be MFMIS with broad junctions, low V_t, and CCM, assuming zero or adequately low gate leakage and a single ferroelectric domain. It is also shown that this DC-optimal NCFET design does not translate to AC power/performance, which is degraded vs. a conventional FET reference for unloaded circuits, while loaded circuits show an improvement. During AC operation, there is also a reduction in the operable V_{DD} window before the onset of polarization switching, forcing a retreat from the DC-optimal design point. Crucially, this study demonstrates two key points: 1.) chasing SS reduction in order to scale V_{DD} and reduce power consumption is not a winning strategy when taken to the theoretical extreme; 2.) even if every possible benefit of the doubt is given to NCFETs, considerable design challenges remain. A realistic technology device menu may therefore need to incorporate both conventional FETs and NCFETs, and perhaps even varying NCFET designs, which presents further challenges for co-optimization and must be the focus of future NCFET studies.

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