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Memory Operation of Z^2-FET Without Selector at High Temperature

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ABSTRACT The electrical performance of Z^2-FET and memory operations of matrix are demonstrated at high temperatures up to 125 °C. The sharp subthreshold slope is maintained and the reliable operation is ensured within the memory window of 229 mV even though the turn on voltage of '0'- and '1'-states are shifted to lower voltage. The '0'-state current remains low while the '1'-state current gradually increases as the temperature increases leading to higher current margin. At the elevated temperature, the potential barriers are slightly reduced but does not collapse, which leads to the successful memory operation. However, increasing the temperature over 125 °C, the potential barrier at the '0'-state is significantly reduced and causes the failure of memory operation with high '0'-state current. The matrix demonstrates reliable memory operations without using selector circuits even at 125 °C.

INDEX TERMS Matrix memory operation, high temperature, Z^2-FET, 1T-DRAM.

I. INTRODUCTION

Scaling issues of the conventional DRAM (dynamic random access memory) has increased the demand for capacitorless 1T-DRAM devices [1]–[4]. Novel memory cells based on SOI exhibit great performance for embedded application such as MSDRAM [5]–[7], A2RAM [8]–[10], and Z^2-FET [11]–[13]. Among them, Z^2-FET has shown great interest for the next generation DRAM device which features sharp switching characteristics with high on/off current ratio, low operation voltage, and scalability [14]–[16]. Also, recent studies have demonstrated memory operations in array structure proving the feasibility of the matrix operation [17]. However, for the temperature conscious applications such as embedded memory in logic circuit and electric vehicles, reliability should be analyzed at higher temperature over than 85 °C that has been popularly tested for the temperature reliability. The main purpose of this work is to experimentally investigate the reliability of Z^2-FET device and matrix memory at wider temperature range from 25 °C to 175 °C through DC and transient characteristics. Also, the failure mechanism of memory operation has been studied through experimental and simulation results unlike previous studies [15], [18], [19]. Lastly, matrix operation without using selector has been successfully demonstrated in elevated temperature for the first time to confirm the reliable matrix memory operation.

II. EXPERIMENTAL

The Z^2-FET device used in this study is fabricated by STMicroelectronics using standard 28nm FD-SOI technology depicted in Fig. 1. The device has a p-i-n structure with the body of the SOI undoped (N_{SOI}=10^{16} cm^{-3}) while the lateral drain and source regions are highly doped with boron and arsenic, respectively ($N_{D/A}$ > 10^{20} cm^{-3}). The film thickness of the SOI (t_{SOI}) is 7 nm whereas the ungated and side electrodes feature a 15 nm epitaxy reaching around 22 nm thickness. The thickness (t_{BOX}) of buried oxide (BOX) is 25 nm and the SiO_2/HfON multilayer front-gate insulator (t_{FOX}) has a 3 nm equivalent oxide thickness (EOT). The front-gate covers only a half of the whole channel placed in the drain side which is called the gated region (L_G) while the other half side is the ungated region (L_{IN}) located near the

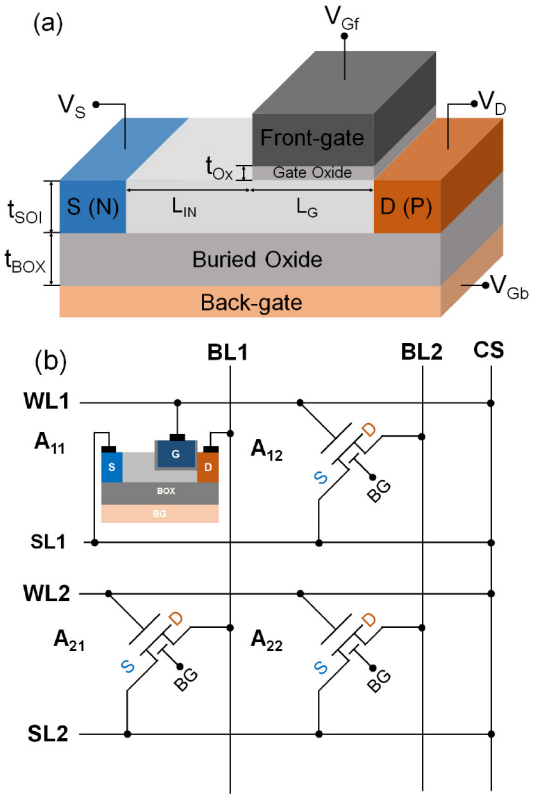

FIGURE 1. (a) Device structure of Z^2-FET with four bias terminal and (b) structure of the 2x2 matrix without selector.

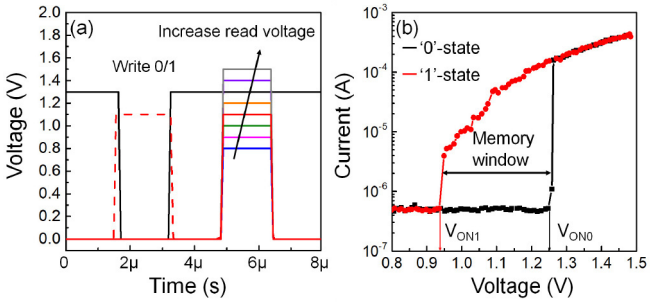

FIGURE 2. (a) Bias waveform to extract memory window as increasing the read voltage by 0.01 V (Write 1 as dashed line) and (b) memory window.

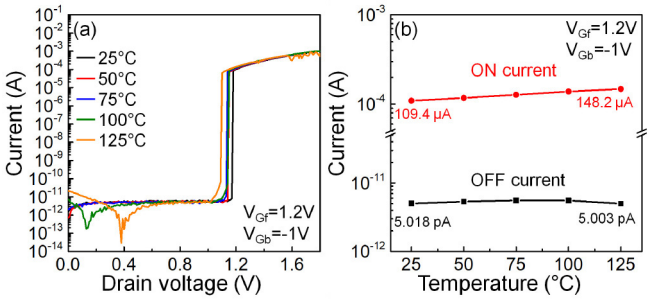

FIGURE 3. (a) I_D-V_D curve and (b) the current of on and off state at various temperature.

source. L_G and L_{IN} are both 200 nm, width is 400 nm, and a highly p-type ground-plane ($N_{GP} \approx 10^{19}$ cm^{-3}) beneath the BOX layer acts a back-gate. KEITHLEY 4200-SCS semiconductor analyzer with custom programmed pulses were used to drive the transient signals. The rise/fall time (t_r/t_f) of the voltage pulse is 50 ns and the pulse width is 1.5 μs. The 2 x 2 matrix structure is shown in Fig. 1 (b) which consist of four Z^2-FET devices with two bitlines (BL) and two wordlines (WL) connected to each drain and front-gate respectively. The back-gate bias is applied all at once which is fixed at -1 V.

III. RESULTS AND DISCUSSION

A. BASIC OPERATION

The operation mechanism of the Z^2-FET is based on the modulation of hole and electron injection barriers formed by the front and back-gate bias. These barriers create two distinct current states depending on the barriers. To turn on the device, the applied drain voltage (V_D) must be high enough for the carriers to overcome these barriers which is the turn on voltage (V_{ON}). As the V_D exceeds the V_{ON}, positive feedback occurs and the device is turned on with high current. The '0'-state has higher potential barriers than the '1'-state which requires more drain voltage to turn on the device whereas the '1'-state requires lower voltage. Therefore, the different V_{ON} between '0'- and '1'-state creates a memory window where distinct current appears when read voltage is applied. To extract the memory window, each state is written and read while increasing the read voltage by 0.01 V as shown in Fig. 2 (a) and the current at each read voltage is plotted in Fig. 2 (b). Notice that the '1'-state has lower V_{ON} than '0'-state which means that it is easier for the carriers to inject into the body and turn on the device. Two distinguishable current levels can be obtained when the read voltage is applied between '1'-state V_{ON} (V_{ON1}) and '0'-state V_{ON} (V_{ON0}).

B. DC CHARACTERISTICS

The Z^2-FET device shows great advantage in switching characteristics with high on/off current ratio and very low subthreshold swing [11]. The switching characteristic is further investigated at elevated temperature from 25 °C to 125 °C shown in Fig. 3 (a). When the drain voltage is swept from 0 V to 1.7 V, the off current remains low and abruptly increases to on state. As the temperature increases, it can be seen that the sharp switching is still observed. The current of on and off state is plotted in Fig. 3 (b). The off current remains low regardless of the temperature while the on current increases as the temperature increases.

C. MEMORY OPERATION

To investigate the effect of temperature in Z^2-FET devices, the memory operation is demonstrated from 25 °C to 125 °C and the performance is shown in Fig. 4. Fig. 4 (a) and (b) shows the read current of write '0'-read (W0-R) and write '1'-read (W1-R) respectively. Fig. 4 (a) clearly shows

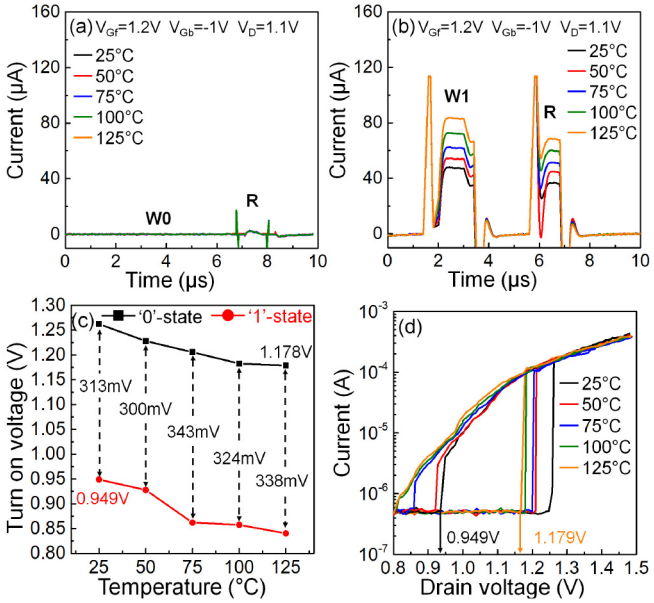

FIGURE 4. **(a) Read current of write '0'-read, (b) read current of write '1'-read, (c) turn on voltage at '0'- and '1'-state, and (d) memory window with increasing the temperature (V_{Gb}=-1 V).**

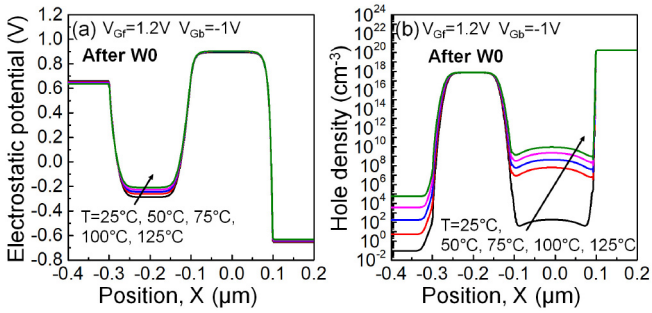

FIGURE 5. **(a) Potential distribution of the device and (b) hole density after write '0' at elevated temperatures.**

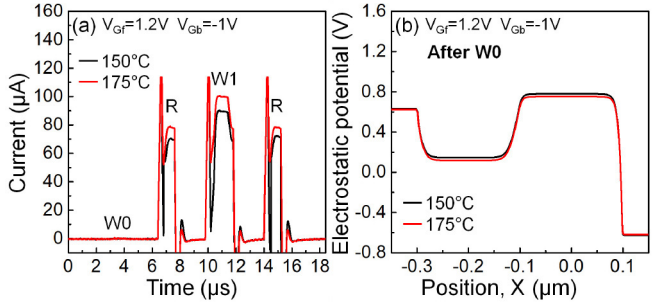

FIGURE 6. **(a) Current during memory pattern and (b) potential distribution after write '0' at 150 °C and 175 °C.**

that the '0'-state current (I_0) maintains low as increasing the temperature up to 125 °C. It is important to sustain low current when reading the '0'-state for proper memory operation even at elevated temperature. Although the '1'-state current (I_1) becomes higher with temperature, the memory operation does not fail since the '1'-state read current is normally high. Therefore, the point is to keep the current margin (I_1-I_0) high enough to distinguish '0'- and '1'-state current by sustaining the I_0 low when the operation temperature is increased. Another requirement of the reliable memory operation is the memory window. Fig. 4 (c) shows the turn on voltage of both '0'-and '1'-state with increasing temperature. The result indicates that the V_{ON0} decreases from 1.263 V to 1.178 V and the V_{ON1} shifts from 0.949 V to 0.840 V due to the lowered potential barriers. However, the voltage difference between the V_{ON0} and the V_{ON1} is very slightly increased with temperature. The memory window has been measured with the temperature range from 25 °C to 125 °C. As shown in Fig. 4 (d), for reliable memory operation, the applied read voltage must be within the voltage range between 0.949 V (the highest V_{ON1} at 25 °C) and 1.178 V (the lowest V_{ON0} at 125 °C) which has 229 mV of memory window. These experimental results clearly indicate that normal memory operation is available when the drain voltage applied for memory operation is 1.1 V because V_D=1.1 V is inside the memory window while increasing the temperature from 25 °C to 125 °C.

To further study the effect of temperature concerning the carrier injection barriers, the potential distribution and hole carrier concentration are simulated with increasing the temperature from 25 °C to 125 °C after writing the '0'-state in Fig. 5. The Shockley-Read-Hall (SRH) generation explains that carrier density of electron and hole may be increased with the temperature in the channel body, which causes the reduction of potential barrier [18]. Consequently, the reliable memory operation depends on whether the potential barrier prevents the carrier injection into the channel body and the '0'-state is sustained or not. Fig. 5 (a) clearly shows that the potential barrier maintains nearly the same height with increasing temperature so that carriers are unable to pass through the barrier. Fig. 5 (b) is the simulated result of hole concentrations along the L_G and L_{IN} after wiring the '0'-state. In this case, the simulation result shows that the hole concentration is abruptly increased while the temperature changes from 25 °C to 50 °C. However, the further increase of hole concentration is not significant with raising the temperature up to 125 °C. As a result, the potential barrier seems to be slightly reduced considering that the increased hole concentration should be divided by the large junction capacitance. This slight reduction of potential barrier explains why the turn on voltage is decreased with temperature in Fig. 4 (c). Thanks to lower potential barrier, the carrier injection occurs easily and the reduction of V_{ON} is comparable with the reduced potential barrier.

In contrast, when the temperature rises from 150 °C to 175 °C the high concentration of carriers collapses the potential barrier. Fig. 6 (a) shows that the read current is very high compared with Fig. 4 (a). The '0'-state becomes unable to be read, meaning that the memory operation has failed at the '0'-state. The potential distribution also shows that after writing the '0'-state, the potential barrier is significantly reduced

compared to the potential barriers in Fig. 5 (a). This collapse of potential barrier leads to the high injection of carriers into the L_G and L_{IN}, causing higher '0'-state current at higher temperature. On the other hand, after writing the '1'-state, although the read current becomes higher with the temperature, there is no limit in the high current range of '1'-state. This does not lead to the failure of memory operation since the '1'-state current should be originally high through the triggering of the positive feedback mechanism [11].

The retention time is another important factor for the Z^2-FET to act as a memory device. However, the degradation of retention time intensely increases above 85 °C (not shown) which more frequent cell refresh should be implemented at very high temperatures to compensate for the higher carrier generation rate. Further optimization is required to improve the retention at very high temperatures.

D. MATRIX OPERATION

In our previous research [17], matrix memory operation has been successfully operated without using selectors by employing select and deselect voltage. In this section, the matrix memory operation without selector is demonstrated at high temperature. The variation of all four devices are examined before the measurement by comparing the memory window which the results show maximum variation of 16 mV.

Since the select and deselect mechanism is based on the applied read voltage locating inside and outside the memory window, it is important to investigate the memory window of select (V_{Gf}=1.2 V) and deselect voltage (V_{Gf}=1.6 V) at high temperature. In order to achieve proper matrix operation at high temperature, two conditions must be satisfied. First, the read voltage must be within the memory window of V_{Gf}=1.2 V at all temperatures. Second, the read voltage must be lower than the memory window of V_{Gf}=1.6 V at all temperatures because the device must be off at all cases when the deselect voltage is applied. Fig. 7 (a) and (b) indicate the memory window of V_{Gf}=1.2 V and V_{Gf}=1.6 V at 25 °C and 125 °C respectively. In Fig. 7 (a), the read voltage must be between 0.949 V and 1.179 V for proper memory operation. When the temperature rises to 125 °C at V_{Gf}=1.6 V (Fig. 7 (b)), the memory window shifts about 60 mv to 70 mv which shifts the '1'-state turn on voltage to 1.147 V. This infers that the read voltage must be below 1.147 V in order to turn off the device. In conclusion, when the read voltage is in the range of 0.949 V to 1.147 V, the matrix memory operation properly works at all temperatures. Fig. 7 (c), (d), and (e) show the final result of the matrix memory operation at 125 °C by applying V_D=1.1 V for read voltage. Each cell is programmed as A_{11}: '1'-state, A_{12}: '0'-state, A_{21}: '0'-state, A_{22}: '1'-state. When the two cells connected to the WL1 (A_{11} and A_{12}) are read, deselect voltage is applied to WL2 and vice versa. During the first read, the high current of BL1 refers to A_{11} and the low current of BL2 refers to A_{12} cell. Likewise, in the second read process, the low current of BL1 refers to A_{21} and the high current of BL2 refers to A_{22} cell. These results indicate that the matrix operates normally at 125 °C with just higher current in '1'-state compared to the current at room temperature represented by dashed line in Fig. 7 (e). As more devices are included to the matrix, it is more likely to have a device with deviation from the average memory window which can impact the memory operation. However, previous study [20] report that the change on V_{ON} is no larger than 170 mV which the 230 mV window would be safe in most situations if the window is adequately centered.

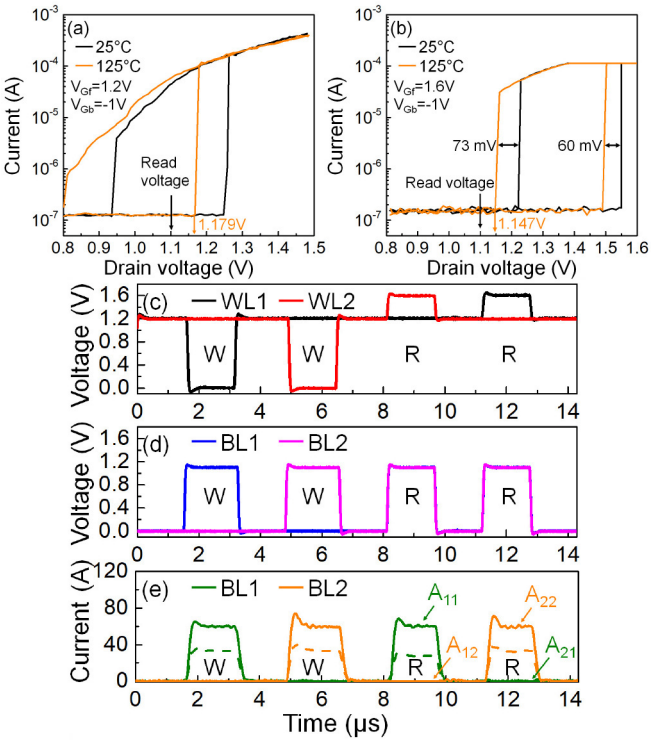

FIGURE 7. Memory window of (a) V_{Gf}=1.2 V (select voltage) and (b) V_{Gf}=1.6 V (deselect voltage) at 25 °C and 125 °C. Bias condition of (c) wordline, (d) bitline, and (e) read current during matrix memory operation at 25 °C (dashed line) and 125 °C.

IV. CONCLUSION

The DC and transient electrical characteristics of Z^2-FET cell devices are demonstrated with the 2x2 matrix while increasing temperature from 25°C to 175 °C. The memory window for the reliable operation maintains 229 mV even though the turn on voltages of both '0'- and '1'-states shift to lower voltage as increasing the temperature from 25 °C to 125°C. The potential barrier seems to be slightly reduced with increasing the temperature because of the increased hole concentrations. However, the '0'- and '1'-states are able to read and write till 125 °C since the high potential barrier is maintained. At 150 °C the barrier starts to collapsed, resulting in the failure of memory operation of '0'-state. The matrix performance is successfully demonstrated without using selectors by employing select and deselect front-gate bias via WL even at 125 °C.

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