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Time-Dependent Dielectric Breakdown of Commercial 1.2 kV 4H-SiC Power MOSFETs

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ABSTRACT Constant-voltage time-dependent dielectric breakdown (TDDB) measurements are performed on recently manufactured commercial 1.2 kV 4H-SiC power metal-oxide-semiconductor (MOS) field-effect transistors (MOSFETs) from three vendors. Abrupt changes of the electric field acceleration parameters (γ) are observed at oxide electric fields (E_{ox}) around 8.5 MV/cm to 9 MV/cm for all commercial MOSFETs. Gate leakage currents and threshold voltage shifts are also monitored under different oxide fields (E_{ox} = 8 MV/cm and 10 MV/cm). The results suggest the failure mode under high oxide electric field is modified by impact ionization or Anode Hole Injection (AHI) induced hole trapping. This observation agrees with previously published oxide reliability studies on SiC MOSFETs and suggests that constant-voltage TDDB measurements need to be carefully performed under low oxide fields to avoid lifetime overestimation caused by hole trapping. The extrapolated $t_{63\%}$ lifetimes (times to 63% failures) from TDDB measurements performed at $E_{ox} < 8.5$ MV/cm are longer than 10^8 hours at 150°C for all vendors. The predicted lifetimes at $E_{ox} = 4$ MV/cm demonstrate more than 10^5 times increases than the oxide lifetimes reported a decade ago, showing promising progress in SiC technology.

INDEX TERMS Electron and hole trapping, impact ionization, gate oxide reliability, lifetime, silicon carbide (SiC) power MOSFETs, time-dependent dielectric breakdown (TDDB).

I. INTRODUCTION

Silicon carbide (SiC) power metal-oxide-semiconductor (MOS) field-effect transistors (MOSFETs) are replacing Silicon (Si) insulated-gate bipolar transistors (IGBTs) in applications such as electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs) [1]–[3] because of the superior material properties of SiC compared to Si for power electronics designs [4], [5]. Due to the safety-critical nature and the operational lifetime requirement of the automotive industry, the long-term integrity of the gate oxides of SiC power MOSFETs is a primary concern.

The gate oxide reliability has been extensively studied throughout the development of SiC power MOSFETs [6]–[21]. The progress of material properties and device fabrications [22]–[24] enabled significant device performance and reliability advancements. Improved lifetime extrapolations were reported for TDDB studies conducted on small area SiC MOS capacitors and SiC DMOSFETs [17]–[19]. Recent studies also show encouraging lifetime predictions for 1.2 kV SiC power MOSFETs from commercial vendors [11], [15]. However, to meet the automotive industry's oxide reliability requirement, more rigorous TDDB measurements are needed. The mentioned TDDB studies cannot fully reflect the oxide reliability of the currently available commercial SiC power MOSFETs for the following reasons.

First, constant-voltage TDDB performed on MOS capacitors cannot faithfully reflect the oxide reliability of SiC power MOSFETs because SiC power MOSFETs and SiC MOS capacitors have different fabrication processes. The SiC power MOSFETs go through extra fabrication processes such as ion implantation and activation annealing to activate the implanted ions. These process steps generate extended and point defects and increase the surface roughness [25]–[27]. Increased surface roughness produces a non-homogeneous oxide electric field profile, creates local weak spots, and degrades oxide reliability [28]. TDDB reported in [17], [19] shows predominantly worse results for the SiC vertical DMOSFETs than the SiC MOS capacitors.

Second, currently available commercial SiC power MOSFETs typically have active areas that are orders of magnitudes larger than the reported small area SiC MOS capacitors and SiC DMOSFETs. More area-dependent extrinsic defects, which control the early failures of the MOS devices [29], can be included in the oxide with larger active areas at a given defect density. More significant portions of early failures caused by extrinsic defects are indeed observed for devices with larger active areas [17], [19]. Even though all vendors screen their commercial SiC MOSFETs for the area-dependent extrinsic defects [30], most gate voltage screens do not remove 100% of the parts with extrinsic defects due to the poor screening efficiency in devices with relatively thin gate oxides of 50 nm or less (lower $V_{GS,scr}/V_{GS,use}$) [7].

Third, constant-voltage TDDB needs to be performed under lower oxide electric fields to avoid overestimating the lifetime predictions. Higher electric field acceleration parameters (γ), which lead to lifetime overestimation under normal operating conditions, are observed under oxide electric fields (E_{ox}) higher than 8.5 MV/cm to 9 MV/cm [16]–[19]. Matocha *et al.* [19] suggest that the failure mode under high oxide might be modified by impact ionization at oxide fields greater than 8.5 MV/cm to 9 MV/cm for oxide thickness of 50 nm in the typically SiC power MOSFET designs. Gate leakage currents reported by Moens *et al.* [8] show rapid increases of gate leakage currents when $E_{ox} > 9$ MV/cm, suggesting that the failure mode under $E_{ox} > 9$ MV/cm is altered by impact ionization induced hole trapping. Murakami and Okamoto [6] also presented similar gate leakage current behavior and recommended that constant-voltage TDDB measurements be carefully applied by examining the gate leakage current behavior under different gate voltage stresses.

In summary, direct TDDB measurements on SiC power MOSFETs at lower oxide electric fields are needed to evaluate the gate oxide reliability of these commercial products accurately. This paper presents the oxide reliability studies on recently manufactured commercial 1.2 kV 4H-SiC power MOSFETs under a wide range of oxide electric fields. The gate leakage currents and threshold voltage shifts are also monitored under different gate voltage stresses to investigate the underlying failure mechanisms at different oxide fields.

TABLE 1. Tested 1200 V commercial SiC planar power MOSFETs.

Properties	Vendor		
	H	I	E
Typical R_{on} @RT (mΩ)	60	80	300
Estimated Active Area (mm^2)	20	18	5
Mean V_{th} @RT (V)	4.9	4.7	4.5
Standard Deviation of V_{th} @RT (V)	0.08	0.19	0.2
Mean Oxide V_{BR} @150°C (V)	45	57	51
Estimated t_{ox} (nm)	41	52	46

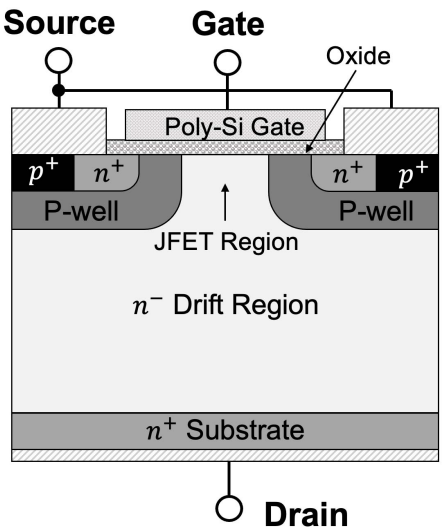


FIGURE 1. A typical cross-sectional view of a commercial SiC vertical planar power MOSFET (DMOSFET) is shown.

II. EXPERIMENTAL METHODS

Constant-voltage TDDB measurements are performed at 150°C on commercial 1.2 kV SiC power MOSFETs (TO-247-3 packaged). Table 1 includes the general information of the commercial SiC MOSFETs. The cross-sectional view of a typical planar power MOSFET (DMOSFET) is shown in Fig. 1. The active areas are estimated from the current ratings (assuming a constant current density of 200 Acm^{-2}) to provide a relative comparison between vendors. The oxide thicknesses are estimated from the mean oxide breakdown voltages at 150°C, assuming that the critical oxide breakdown electric field is 11 MV/cm ($t_{ox} = V_{ox}/E_{ox}$).

All commercial devices are characterized by a semiconductor parameter analyzer (B1505A, Keysight, Inc) and carefully selected so that the threshold voltage variation among each group is less than 0.1 V. This ensures that the devices under test (DUTs) sustain similar gate oxide electric fields under the same experimental condition.

The threshold voltages are extracted with the linear extrapolation method [31] at $V_{DS} = 0.1$ V. The on-resistances are measured at the maximum allowed gate voltages with $V_{DS} = 1$ V. Gate oxide breakdown voltages (V_{BR}) at 150°C are measured by ramping up the gate voltage while measuring the gate leakage current until dielectric breakdown with

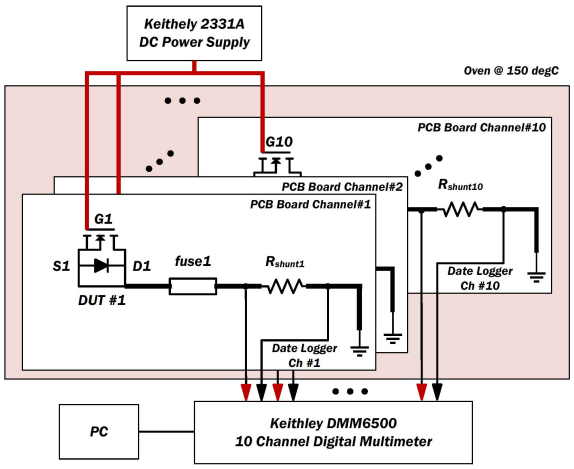


FIGURE 2. The diagram represents the schematic of the TDDB setup. A customized high-temperature PCB board is designed to hold ten commercial MOSFETs in parallel. The PCB board is placed inside an oven at 150°C during the TDDB measurements.

the source and drain terminals of the DUTs shorted to the ground.

During the constant-voltage TDDB experiment, a constant gate voltage is applied simultaneously to all the gate electrodes of 10 DUTs with their source and drain electrodes grounded (Fig. 2). Failure times are logged with a 10-channel digital multi-meter (DMM 6500, Keithley, Inc), then analyzed with Weibull statistics (method described in more details in [32]). The cumulative percentage of failure is estimated using the median rank method [33].

For the gate leakage current and threshold voltage shift measurements, separate devices independent of the TDDB test are used. The B1505A semiconductor parameter analyzer is used to apply a constant bias to the gate terminal of the DUT and monitor the gate leakage current while the source and drain of the DUT are grounded. The stress is interrupted regularly while the same equipment is used for rapid (in less than 10 seconds) threshold voltage measurements.

III. RESULTS AND DISCUSSION

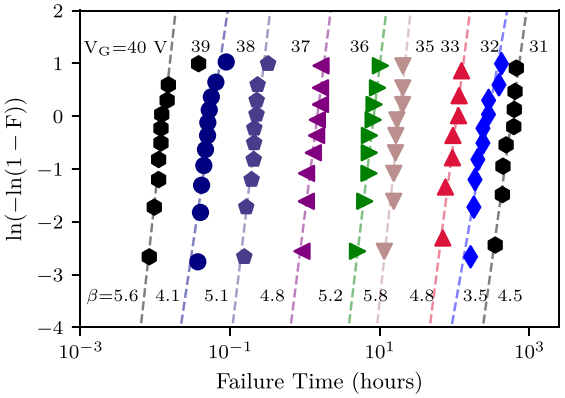
This section introduces the Weibull statistics used to analyze the TDDB measurements, followed by the results and discussion of the lifetime extrapolations. Gate leakage currents and threshold voltage shifts under constant gate stresses are also monitored on separated devices that are independent of the TDDB measurements to study the different failure mechanisms under different oxide electric fields.

A. WEIBULL STATISTICS AND WEIBULL DISTRIBUTIONS

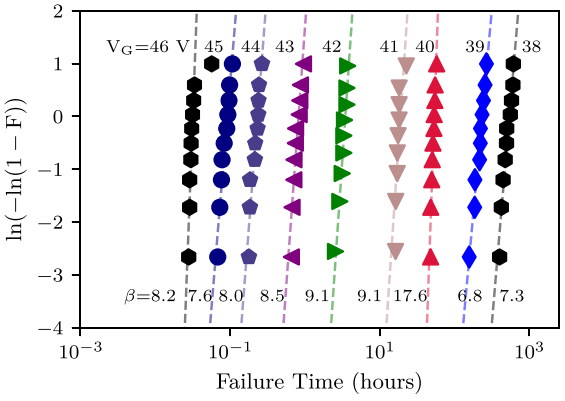
The failure times obtained from TDDB measurements are analyzed with Weibull distribution described by

$$F(t) = 1 - e^{-(t/t_{63\%})^{\beta}}, \tag{1}$$

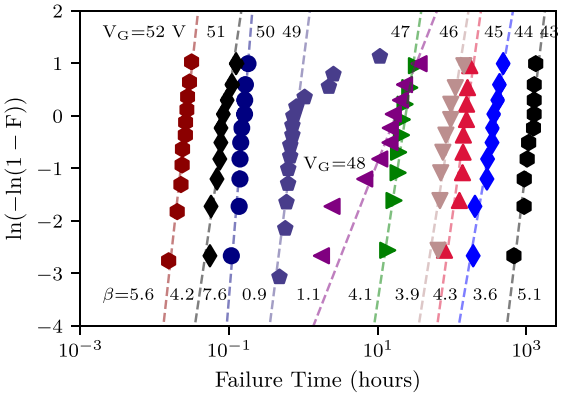
where $F(t)$ is the cumulative percentage of failures at a given time t, $t_{63\%}$ is the time that 63.2% of the sample



(a) Vendor H



(b) Vendor E



(c) Vendor I

FIGURE 3. Weibull distributions of measured lifetimes at 150°C with different gate voltage stress for (a) vendor H, (b) vendor E, and (c) vendor I.

population fails (often referred to as characteristic lifetime or η), and β is the Weibull slope parameter. Less variation in the failure times produces larger β and suggests better gate oxide uniformity.

Equation (1) can be rewritten as

$$ln(-ln(1-F)) = \beta ln(t) - \beta ln(t_{63\%}). \tag{2}$$

A $ln(-ln(1-F))$ vs. failure time plot is often referred to as the Weibull plot. Figure 3 shows the Weibull plots for the

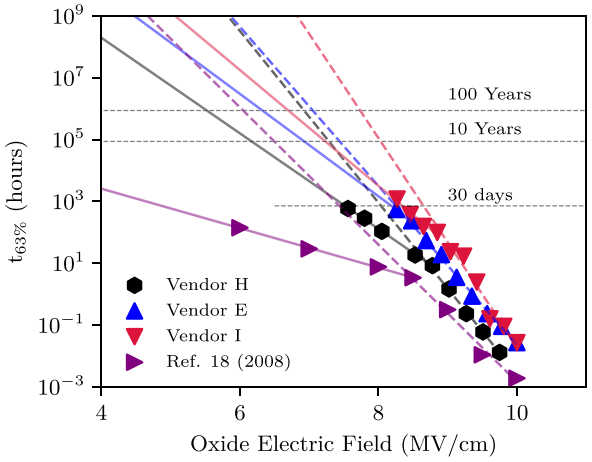


FIGURE 4. $t_{63\%}$ vs. E_{ox} at 150°C for all commercial SiC MOSFETs are shown. TDDB measurements on small-area DMOSFETs in [19] are also reconstructed here.

commercial SiC MOSFETs for all three vendors. Based on (2), β can be extracted from the slope of the fit line, while $t_{63\%}$ can be calculated by extracting the time when the fit line equals zero. Apparent extrinsic failures that distinctively fall outside of the lifetime distributions are ignored when extracting β.

β of intrinsic oxide is independent of stress voltages. Therefore, the uniformity of the β across different gate voltage stresses for vendor H [Fig. 3(a)], and vendor E [Fig. 3(b)] are indications of uniform oxide qualities. Weibull distributions for vendor I at $V_G = 49$ V and 48 V show significant lifetime variations. These variations can be caused by varying oxide quality. Alternatively, the lifetime variations might be explained by the bi-modal Weibull distribution in [8], while the authors attribute the variations to the transition between different current conduction mechanisms under different oxide electric fields.

B. DIFFERENT γ UNDER DIFFERENT OXIDE ELECTRIC FIELDS

Assume $E_{ox} \approx V_G/t_{ox}$, the extracted $t_{63\%}$ as a function of E_{ox} for all the commercial SiC MOSFETs are plotted in Fig. 4. Lifetime predictions under the typical operating condition ($E_{ox} = 4$ MV/cm at 150°C) are made based on the commonly used thermal-chemical E-model [34]. The model states that the breakdown time (t_{BD}) in the log scale is proportional to oxide electric fields with a slope of $-\gamma$ ($ln(t_{BD}) \propto -\gamma E_{ox}$). The slope parameter γ is often referred to as the electric field acceleration factor, which describes how fast t_{BD} changes with E_{ox}.

Two distinctly different field acceleration factors are observed for the $t_{63\%}$ under high and low oxide electric fields (Fig. 4) for all vendors. TDDB measurements on small-area SiC MOS capacitors [17] and SiC DMOSFETs [19] also report the same phenomenon. The abrupt change of field acceleration factors happens at oxide electric fields around 8.5 MV/cm to 9 MV/cm both in our measurements and the published studies. Clearly, for the purpose of lifetime prediction, $E_{ox} < 8.5$ MV/cm should be used. The discussion in the next section will shed more light on the reason behind the abrupt change in γ.

C. FAILURE MECHANISMS UNDER DIFFERENT OXIDE ELECTRIC FIELDS

The abrupt change in field acceleration factors implies different failure mechanisms under different oxide electric fields. Recently published charge-to-breakdown studies on SiC n-epi MOS capacitors [8] showed that electron and hole trapping are the causes for the different behaviors under different oxide electric fields. The authors observed distinct gate leakage current behaviors and failure distributions under different oxide electric fields. The gate leakage current under high oxide electric field stress increases until the device breaks down, which indicates positive charge build-up induced by the hole trapping near the injecting boundary.

The energy band diagrams in Fig. 5 explain the different failure mechanisms under different oxide electric fields. Under high fields, holes are generated by impact ionization in the oxide or Anode Hole Injection (AHI) or both in the poly-silicon gate [35]. These holes drift towards SiC, and get trapped near the SiC/SiO2 interface (Fig. 5(a)). The trapped holes enhance the oxide electric field near the interface, reduce the barrier width, and increase the F-N tunneling current. The enhanced electron injection causes more hole current due to intensified impact ionization and consequently initiates a positive feedback process. This feedback process may or may not be stopped depending upon the relative densities of electron and hole traps.

The focus of this work is on the consequence of the positive charge build-up on oxide reliability measurements. Therefore, the exact generation and trapping mechanisms of the holes are beyond the scope of this paper.

Under lower fields, holes are not generated. Electrons that tunnel across the barrier trap both near the interface and throughout the bulk of the gate oxide (Fig. 5(b)). The trapped electrons (represented by a sheet charge located at the centroid of the distribution) relax the oxide electric field at the injecting boundary, extend the tunneling barrier, and reduce the F-N tunneling currents.

D. GATE LEAKAGE CURRENTS AND THRESHOLD VOLTAGE SHIFTS

To further investigate the different failure mechanisms, the gate leakage currents and threshold voltage shifts are monitored for vendor E devices under different gate voltage stresses for up to 24 hours. The gate voltages are selected so that the oxide electric fields are 8 MV/cm and 10 MV/cm. The results are presented in Fig. 6.

Under the high oxide field ($E_{ox} = 10$ MV/cm), both the electron and hole trappings are present in the gate oxide. However, hole trapping dominates when $E_{ox} = 10$ MV/cm, so the gate leakage current increases throughout the measurement. The threshold voltage reduction also reflects the

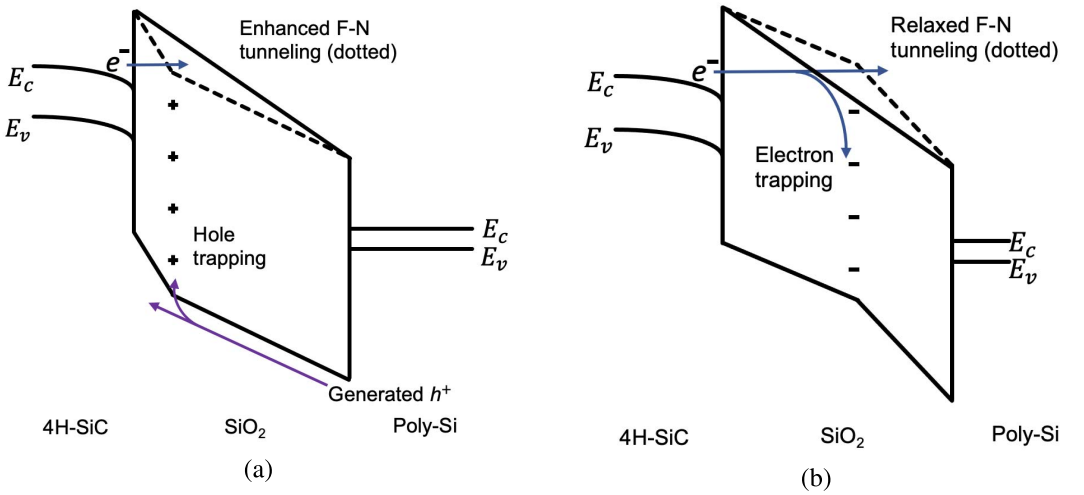


FIGURE 5. Energy band diagrams showing the effects of (a) hole trapping and (b) electron trapping on the barrier widths and F-N tunneling currents at the injecting boundary.

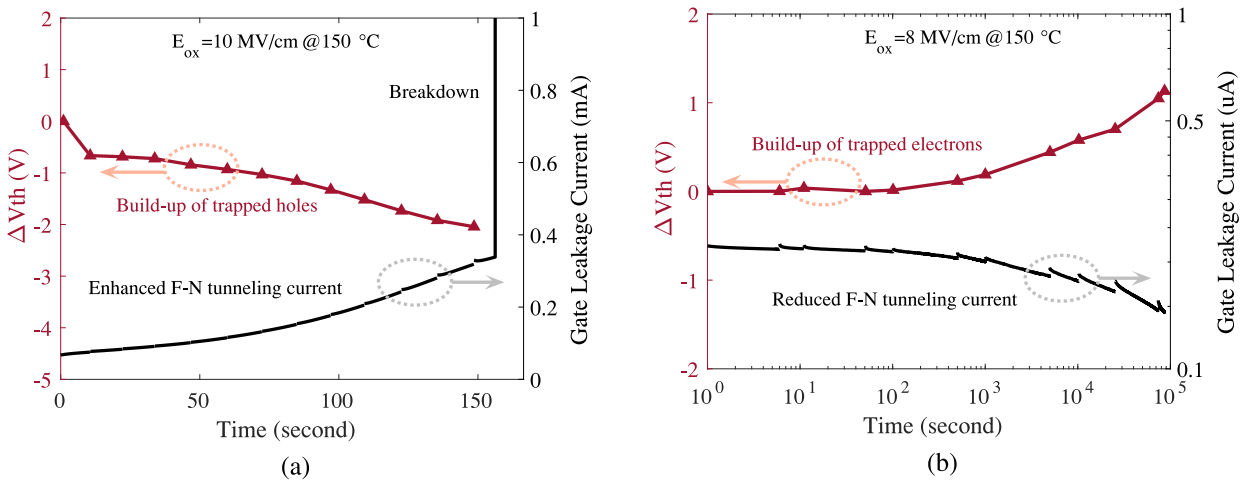


FIGURE 6. Gate leakage current behaviors and threshold variations of vendor E DUTs under constant gate voltage stress with oxide electric fields of (a) 10 MV/cm and (b) 8 MV/cm. The trends of the threshold voltage shifts reflect the build-up of the trapped charges, while the behaviors of the gate leakage currents indicate the effects of the trapped charges on the F-N tunneling currents.

build-up of the positive charge. Under the lower oxide field ($E_{ox} = 8$ MV/cm), electron trapping continuously relaxes the gate leakage current and increases the threshold voltage.

IV. IMPLICATION OF THE MEASUREMENTS

A. IMPLICATIONS FOR LIFETIME PREDICTIONS

Hole trapping under high oxide electric fields enhances the F-N tunneling currents. Therefore, oxide degrades faster under higher oxide fields and hence the much larger γ. Lifetime predictions can be significantly overestimated with a larger γ if the TDDB measurements are conducted only at high oxide electric fields.

As shown in Fig. 4, significant overestimation is observed for all lifetime extrapolations based on high oxide field TDDB measurements (dashed lines in Fig. 4). Considering the stringent oxide reliability requirement of the SiC power MOSFETs, TDDB measurements need to be done at oxide electric fields lower than 8.5 MV/cm to avoid hole trapping and ensure more reliable lifetime predictions. The good news is that, extrapolating from the TDDB measurements done at $E_{ox} < 8.5$ MV/cm (solid lines in Fig. 4), all three vendors show $t_{63\%}$ predictions longer than 10^8 hours at $E_{ox} = 4$ MV/cm and 150°C. Compared to the oxide reliability studies reported a decade ago, the predicted lifetimes in this study demonstrate more than five orders of magnitude increase, showing encouraging progress the technology has achieved.

B. IMPLICATIONS ON MEASUREMENT TIMES

Doing TDDB measurements at lower oxide fields often requires prohibitively long measurement times. Higher temperatures can be applied to shorten the measurement time at the lower oxide electric fields without compromising the lifetime prediction accuracy. Gurfinkel *et al.* [18] observed that the oxide electric field at which γ changes abruptly is

independent of temperature from 230°C to 365°C. Therefore, the lifetime at typical operating temperature can be extrapolated from the higher temperature measurements since the E-model assumes an Arrhenius temperature dependence of the oxide lifetimes ($ln(t_{BD}) \propto 1/T$).

Unfortunately, this method does not work for the packaged commercial devices in this study since the packages are only rated between 150°C and 175°C.

V. SUMMARY

TDDB measurements are applied to recently manufactured 1.2 kV 4H-SiC power MOSFETs from three vendors at 150 °C under moderate and high oxide electric fields. All three vendors show encouraging oxide reliability. The extrapolated $t_{63\%}$ under typical use conditions ($E_{ox} = 4$ MV/cm and 150°C) from TDDB measurements at $E_{ox} < 8.5$ MV/cm are longer than 10^8 hours for all vendors!

Different electric field acceleration parameters (γ) under different E_{ox} are observed for all three vendors. The change of γ indicates that the failure mode is modified under high oxide electric fields. The gate leakage current behavior and threshold voltage shift at $E_{ox} = 10$ MV/cm confirm the effects of hole trapping as previously reported by others, suggesting that impact ionization or Anode Hole Injection (AHI), or both could be the failure mechanism at high oxide electric fields.

Higher γ leads to lifetime overestimation if the TDDB measurements are only performed under E_{ox} larger than 8.5 MV/cm to 9 MV/cm. Therefore, constant-voltage TDDB needs to be performed at lower oxide electric fields to avoid hole trapping and establish more reliable lifetime predictions. It is further suggested that gate oxide screening should be performed under 8.5 MV/cm to avoid hole generation and trapping!

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REFERENCES

[1] M. Yamamoto, T. Kakisaka, and J. Imaoka, "Technical trend of power electronics systems for automotive applications," *Jpn. J. Appl. Phys.*, vol. 59, p. SG0805, Apr. 2020.

[2] X. Ding, M. Du, T. Zhou, H. Guo, and C. Zhang, "Comprehensive comparison between silicon carbide MOSFETs and silicon IGBTs based traction systems for electric vehicles," *Appl. Energy*, vol. 194, pp. 626–634, May 2017.

[3] M. Furuhashi, S. Tomohisa, T. Kuroiwa, and S. Yamakawa, "Practical applications of SiC-MOSFETs and further developments," *Semicond. Sci. Technol.*, vol. 31, no. 3, 2016, Art. no. 034003.

[4] S. Dimitrijev, "SiC power MOSFETs: The current status and the potential for future development," in *Proc. IEEE 30th Int. Conf. Microelectron. (MIEL)*, Nis, Serbia, 2017, pp. 29–34.

[5] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide bandgap technologies and their implications on miniaturizing power electronic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 374–385, Sep. 2014.

[6] E. Murakami and M. Okamoto, "Anomalous behavior of gate current and TDDB lifetime by constant voltage stress in NO-annealed SiC-MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1207–1213, Mar. 2021.

[7] T. Aichinger and M. Schmidt, "Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Dallas, TX, USA, 2020, pp. 1–6.

[8] P. Moens, J. Franchi, J. Lettens, L. De Schepper, M. Domeij, and F. Allerstam, "A charge-to-breakdown (QBD) approach to SiC gate oxide lifetime extraction and modeling," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Vienna, Austria, 2020, pp. 78–81.

[9] T. Liu *et al.*, "Gate oxide reliability studies of commercial 1.2 kV 4H-SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Dallas, TX, USA, 2020, pp. 195–199.

[10] S. Yu *et al.*, "Threshold voltage instability of commercial 1.2 kV SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Dallas, TX, USA, 2020, pp. 1–5.

[11] D. J. Lichtenwalner *et al.*, "Gate oxide reliability of SiC MOSFETs and capacitors fabricated on 150mm wafers," in *Materials Science Forum*, vol. 963, Trans Tech Publ., 2019, pp. 745–748. [Online]. Available: https://doi.org/10.4028/www.scientific.net/msf.963.745

[12] D. Xing *et al.*, "Design strategies for rugged SiC power devices," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2019, pp. 1–5.

[13] S. Chowdhury, L. Gant, B. Powell, K. Rangaswamy, and K. Matocha, "Reliability and ruggedness of 1200v SiC planar gate MOSFETs fabricated in a high volume CMOS foundry," in *Materials Science Forum*, vol. 924, Trans Tech Publ., 2018, pp. 697–702. [Online]. Available: https://doi.org/10.4028/www.scientific.net/msf.924.697

[14] Z. Chbili *et al.*, "Modeling early breakdown failures of gate oxide in SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3605–3613, Sep. 2016.

[15] Z. Chbili *et al.*, "Time dependent dielectric breakdown in high quality SiC MOS capacitors," in *Materials Science Forum*, vol. 858, Trans Tech Publ., 2016, pp. 615–618. [Online]. Available: https://doi.org/10.4028/www.scientific.net/msf.858.615

[16] M. K. Das, S. K. Haney, J. Richmond, A. Olmedo, Q. J. Zhang, and Z. Ring, "SiC MOSFET reliability update," in *Materials Science Forum*, vol. 717, Trans Tech Publ., 2012, pp. 1073–1076. [Online]. Available: https://doi.org/10.4028/www.scientific.net/msf.717-720.1073

[17] C. Y. Liangchun, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of SiC MOSFETs: A technology for high-temperature environments," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 418–426, Dec. 2010.

[18] M. Gurfinkel *et al.*, "Time-dependent dielectric breakdown of 4H-SiC/SiO_2 MOS capacitors," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 4, pp. 635–641, Dec. 2008.

[19] K. Matocha, G. Dunne, S. Soloviev, and R. Beaupre, "Time-dependent dielectric breakdown of 4H-SiC MoS capacitors and DMOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1830–1834, Aug. 2008.

[20] M. M. Mathur and J. A. Cooper, "Time-dependent-dielectric-breakdown measurements of thermal oxides on n-type 6H-SiC," *IEEE Trans. Electron Devices*, vol. 46, no. 3, pp. 520–524, Mar. 1999.

[21] L. A. Lipkin and J. W. Palmour, "Insulator investigation on SiC for improved reliability," *IEEE Trans. Electron Devices*, vol. 46, no. 3, pp. 525–532, Mar. 1999.

[22] A. Agarwal and S. Haney, "Some critical materials and processing issues in SiC power devices," *J. Electron. Mater.*, vol. 37, no. 5, pp. 646–654, 2008.

[23] P. Jamet and S. Dimitrijev, "Physical properties of N2O and NO-nitrided gate oxides grown on 4H SiC," *Appl. Phys. Lett.*, vol. 79, no. 3, pp. 323–325, 2001.

[24] G. Y. Chung *et al.*, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Electron Device Lett.*, vol. 22, no. 4, pp. 176–178, Apr. 2001.

[25] T. Kimoto, "Material science and device physics in sic technology for high-voltage power devices," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, 2015, Art. no. 040103.

[26] M. A. Capano *et al.*, "Surface roughening in ion implanted 4H-silicon carbide," *J. Electron. Mater.*, vol. 28, no. 3, pp. 214–218, 1999.

[27] V. Heera and W. Skorupa, "Ion implantation and annealing effects in silicon carbide," in *MRS Online Proceedings Library Archive*, vol. 438, Cambridge Univ. Press, 1996. [Online]. Available: https://doi.org/10.1557/PROC-438-241

[28] J. Senzaki, K. Kojima, T. Kato, A. Shimozato, and K. Fukuda, "Correlation between reliability of thermal oxides and dislocations in n-type 4H-SiC epitaxial wafers," *Appl. Phys. Lett.*, vol. 89, no. 2, 2006, Art. no. 022909.

[29] K. P. Cheung, "SiC power MOSFET gate oxide breakdown reliability—Current status," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Burlingame, CA, USA, 2018, pp. 2–3.

[30] Y. Zheng, R. Potera, and T. Witt, "Characterization of early breakdown of SiC MOSFET gate oxide by voltage ramp tests," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2021, pp. 1–5.

[31] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. T. Barrios, J. J. Liou, and C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 53, no. 1, pp. 90–104, 2013.

[32] T. Liu *et al.*, "Gate leakage current and time-dependent dielectric breakdown measurements of commercial 1.2 kV 4H-SiC power MOSFETs," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Raleigh, NC, USA, 2019, pp. 195–199.

[33] J. C. Fothergill, "Estimating the cumulative probability of failure data points to be plotted on weibull and other probability paper," *IEEE Trans. Elect. Insul.*, vol. 25, no. 3, pp. 489–492, Jun. 1990.

[34] J. W. McPherson and H. C. Mogul, "Underlying physics of the thermochemical *E* model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films," *J. Appl. Phys.*, vol. 84, no. 3, pp. 1513–1523, 1998.

[35] P. Samanta and K. C. Mandal, "Leakage current conduction, hole injection, and time-dependent dielectric breakdown of n-4H-SiC MOS capacitors during positive bias temperature stress," *J. Appl. Phys.*, vol. 121, no. 3, 2017, Art. no. 034501.