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Investigation of Re-Program Scheme in Charge Trap-Based 3D NAND Flash Memory

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ABSTRACT Early retention or initial threshold voltage shift (IVS) is one of the key reliability challenges in charge trapping memory (CTM) based 3D NAND flash. Re-program scheme was introduced in quad-level-cell (QLC) NAND (Shibata *et al.,* 2007, Lee *et al.,* 2018, Shibata *et al.,* 2019, and Khakifirooz *et al.,* 2021), and the IVS improvement by re-program scheme was reported. In this work, it is found that re-program can suppress ~81% of IVS in 3D NAND, which is much more significant than that of 2D NAND ~50% (Chen *et al.,* 2010). The mechanisms of IVS improvement by re-program scheme in 3D NAND are investigated. Both vertical de-trapping in the BE-tunneling oxide and charge lateral migration (LM) in the charge-trap layer are suppressed in re-program. Re-program is effective in vertical de-trapping suppression both in checker-board pattern (C/P) and solid-board pattern (S/P) cases, and is effective in LM suppression only in C/P case. Furthermore, the LM improvement by re-program scheme is more pronounced with gate length (Lg) and inter-gate space (Ls) scaling down, showing potential in the reliability improvement of advanced 3D NAND technologies.

INDEX TERMS 3D NAND flash, QLC, re-program, IVS, LM.

I. INTRODUCTION

Over the past years, 3D NAND flash has become the mainstream of non-volatile memory due to its ultra-high storage density, lower bit cost [1]–[4]. As the vertical cells of 3D charge trapping NAND flash share a common charge-trap layer, the trapped charge can migrate laterally along the channel direction. Hence, the retention characteristics of CTM device are considered to be inferior to that of the floating gate device [5]. In advanced QLC technologies, the read margin window is very small [6], which results in strict requirement of IVS characteristics.

Chen *et al.* proposed a "refill" method to reduce fast charge loss in CTM based 2D NAND flash [7]. The mechanism of "refill" is that the shallowly trapped electrons de-trap from the charge-trap layer after the 1st program, and the same amount of electrons will be filled into both shallow and deep level traps of charge-trap layer during the 2nd program to reach the original threshold voltage (V_{th}). Eventually, there are less shallowly trapped electrons in the charge-trap layer, which improves the IVS. Benefit of re-program scheme is also demonstrated in 3D QLC NAND [8]–[10]. However, there is no available mechanism study on re-program scheme in 3D NAND flash yet. BE-tunneling oxide is commonly adopted in 3D NAND, thus the charge trapped in tunneling oxide are primarily responsible for IVS, instead of charge-trap layer [11]. Also, another key charge loss mechanism in 3D CTM device is lateral migration (LM), which is associated with the continuous charge-trap layer. In this work, the mechanisms of re-program scheme for IVS improvement in CTM based 3D NAND flash are investigated. Experimental analysis and TCAD simulations are used to interpret the

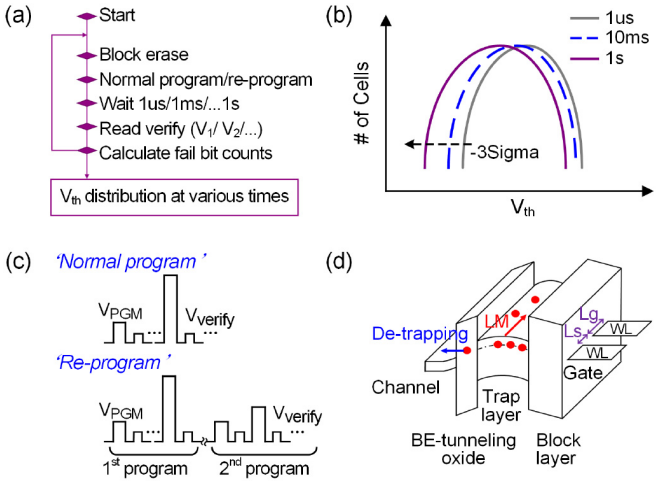

FIGURE 1. **(a) Test approach of V_{th} distribution in IVS period. (b) Schematic diagram of V_{th} distribution during IVS period after programming. (c) Schematic diagram of normal program and re-program scheme [8]. (d) Schematic energy band diagram during IVS and possible scenarios of charge loss mechanisms in CTM based 3D NAND cell.**

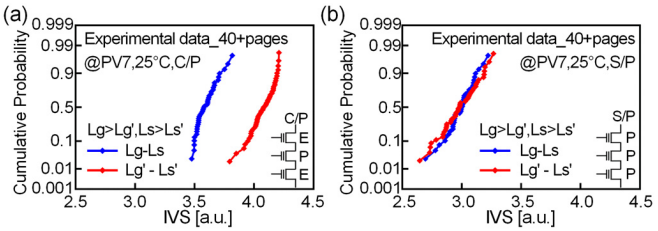

FIGURE 2. **IVS statistical data @1s after programming with (a)C/P and (b) S/P pattern, with different Lg-Ls test samples.**

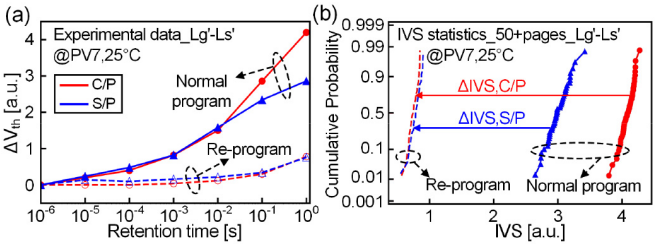

FIGURE 3. **(a) V_{th} shift (ΔV_{th}) within 1s after normal program and re-program. (b) IVS statistical data @1s of normal program and re-program.**

observations. Re-program scheme in 3D NAND suppresses not only vertical de-trapping in the BE-tunneling oxide but also LM in the charge-trap layer. In particular, LM improvement by re-program is more pronounced with Lg-Ls scaling down.

II. DEVICE AND EXPERIMENTS

In this work, the experiments are based on two types of 3D vertical channel charge trapping NAND flash [2], [3] with Lg-Ls = 33/24nm and Lg'-Ls' = 31/20nm, respectively. The BE-tunnel oxide in our device is stacked SiO2 + SiON (silicon oxynitride) structure. To study the array level IVS characteristics, V_{th} distribution of one page in IVS period (within 1s after programming) is measured by fail bit counts. Fig. 1(a) shows the test approach. The maximum delay time between the program and the read is 1 second. Usually, it takes at least ~ one hour of idle time to trigger temporary read errors (first read issue) [12], [13]. Therefore, the influence of first read issue is ruled out in this work. In addition, the −3sigma shift of V_{th} distribution from 1us to 1s after programming is regarded as a measure of IVS in this work, as shown in Fig. 1(b).

The fast charge loss mechanisms in CTM based 3D NAND flash are considered to contain charge de-trapping in the BE-tunneling oxide, vertical redistribution (VR) and LM in the charge-trap layer [14]. The experimental data in our sample shows no obvious inflection points within 10ms after programming (as shown in Fig. 3(a)), which was attributed to VR based on observation of single cell IVS characteristics in previous studies [14], [15]. Therefore, VR is omitted due to no obvious influence on array level IVS in our sample. And charge de-trapping in the BE-tunneling oxide and LM in the charge-trap layer are focused in this work, as shown in Fig. 1(d).

III. RESULTS AND DISCUSSION

A. CHARACTERISTICS OF IVS IN 3D NAND

Firstly, IVS are measured on test samples with two types of Lg-Ls. Compared to large Lg-Ls test sample, the IVS of small Lg'-Ls' test sample increases significantly in the checker-board pattern (C/P) case, as shown in Fig. 2(a). Fig. 2(b) shows that there is no obvious IVS difference between the two types of test samples in solid-board pattern (S/P) case. It is generally considered that the charge loss in S/P case is primarily attributed to the vertical de-trapping, while in C/P case is due to both vertical de-trapping and LM [3], [16]. Therefore, as Lg-Ls scaling down, the IVS increases in C/P cases, due to deteriorated LM [17].

B. CHARACTERISTICS OF RE-PROGRAM SCHEME IN 3D NAND

Re-program scheme is evaluated for IVS suppression in this work. As shown in Fig. 1(c), re-program or "refill" scheme has two consecutive programming operations [7], [8] and the program verify level is equivalent (PV = PV7) in this work. Fig. 3(a) shows the V_{th} shift ($\Delta V_{th} = V_{th(t=0)} - V_{th(t>0)}$) within 1s after normal program and re-program in C/P and S/P case, respectively. The max magnitude of initial charge loss in our sample is about 200mv. Fig. 3(b) shows IVS statistical @1s data after normal program and re-program in both patterns. In normal program case, The IVS in C/P is larger than that of S/P, which is due to the larger LM component in C/P [15]. As shown in Fig. 3(a), the difference between C/P and S/P appears at 10ms after programming, since the LM component has longer time constant (τ) than de-trapping component [14]. In re-program case, it shows that the IVS induced V_{th} shifts under C/P and S/P cases have been suppressed by about 81 % and 73%, respectively.

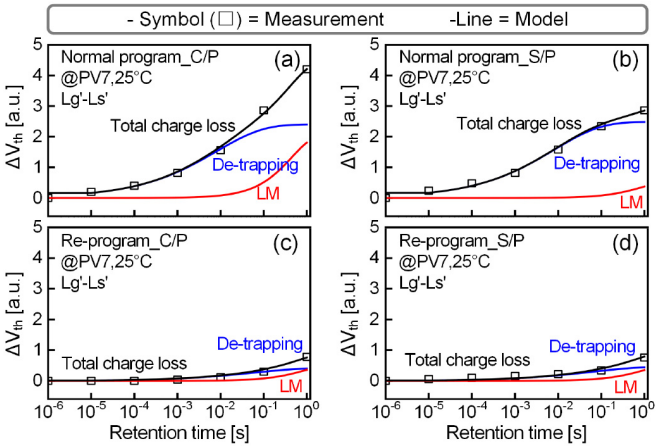

FIGURE 4. ΔV_{th} vs. retention time corresponding to (a) normal program in C/P, (b) normal program in S/P, (c) re-program in C/P, and (d) re-program in S/P. The model matches well with the measurement data.

TABLE 1. The summary of limiting conditions for extracting parameters according to mechanism [11], [15].

	C/P	S/P
Normal program	ΔV_{th}(De-trapping) ≥ ΔV_{th}(LM), ΔV_{th}(LM,C/P) > ΔV_{th}(LM,S/P)	
	τ(De-trapping) < τ(LM), τ(LM,C/P) < τ(LM,S/P)	
	0<β<1	

In addition, re-program can also effectively suppress IVS at different PV levels and temperatures (data not shown).

C. MECHANISMS OF RE-PROGRAM SCHEME IN 3D NAND

To study the mechanisms of re-program in 3D NAND, the stretched exponential function is used to model charge loss mechanisms [14], [15], [18]–[22]. As mentioned above, only two main charge loss components in IVS are considered in this work. Thus, the overall V_{th} shift can be expressed and modeled as the sum of behavior of each mechanism [14], [15], [18]–[22]:

$$\Delta V_{th} = \Delta V_{th,De-trapping}\left(1-\exp\left(-\left(\frac{t_R}{\tau_{De-trapping}}\right)^{\beta_{De-trapping}}\right)\right) + \Delta V_{th,LM}\left(1-\exp\left(-\left(\frac{t_R}{\tau_{LM}}\right)^{\beta_{LM}}\right)\right) \quad (1)$$

where t_R, ΔV_{th}, τ and β are the retention time, final ΔV_{th}, time constant, and shape parameter of the retention curve for each mechanism, respectively. The sum of each mechanism (black line) is in good agreement with the measurement data, as shown in Fig. 4. Table 1 and 2 show the limiting conditions for extracting model parameters. The ΔV_{th} extracted for each mechanism indicates that de-trapping is suppressed for about 83% by re-program in both patterns. And LM is suppressed by up to 80% in C/P but less than 6% in S/P. β is relevant to the degree of variation on each mechanism [18]–[19]. β can also characterize the dispersion of electron trapping or charge loss time constant. The larger β, the smaller dispersion of τ. Because the V_{th} shift induced by IVS is small and has insignificant effect on the dispersion of τ. Therefore, we considered that β is almost unchanged after re-program.

TABLE 2. The summary of limiting conditions for extracting parameters according to program scheme.

Mechanisms	C/P	S/P
De-trapping	ΔV_{th}(Normal program) > ΔVth(Re-program)	
	τ(Normal program) < τ(Re-program)	
	β(Normal program) = β(Re-program)	
LM	ΔVth(Normal program) ≥ ΔVth(Re-program)	
	τ(Normal program) ≤ τ(Re-program)	
	β(Normal program) = β(Re-program)	

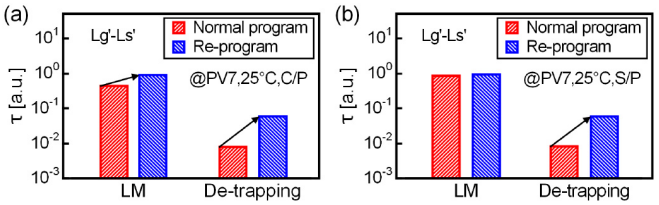

FIGURE 5. τ extracted for each failure mechanism of normal program and re-program scheme under (a) C/P and (b) S/P.

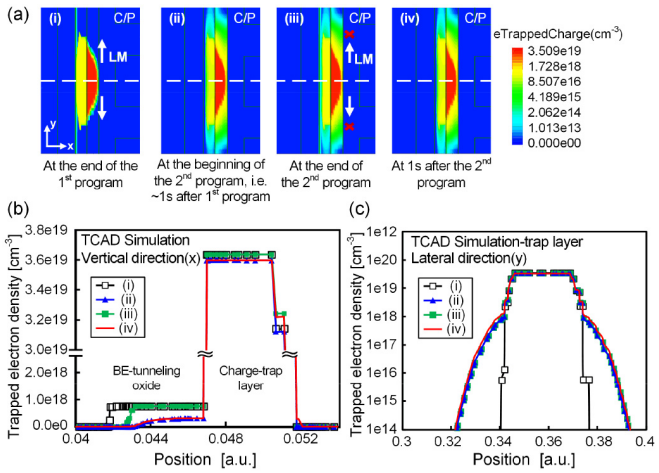

FIGURE 6. TCAD simulation results of (a) contours of electron distribution and (b) trapped electron density along the direction perpendicular to the channel and (c) trapped electron density in the charge-trap layer along the channel in C/P at (i) 0s after the 1st program / normal program, (ii) the beginning of the 2nd program, i.e., ~1s after the 1st program, (iii) 0s after the 2nd program / re-program and (iv) 1s after the 2nd program / re-program.

Fig. 5 shows τ extracted for each mechanism of normal program and re-program. After re-program, τ of de-trapping increases significantly in both patterns, and τ of LM in C/P increases slightly whereas in S/P is almost unchanged, which will be explained in the following.

TCAD simulation is carried out to explore the mechanisms of re-program. For the LM improvement by re-program, the trapped electron distribution at different moment of

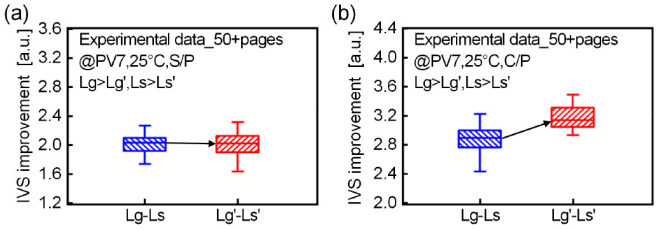

FIGURE 7. IVS improvement ($\Delta IVS = IVS_{Normal\ program} - IVS_{Re-program}$) by re-program scheme with (a) S/P and (b) C/P pattern, with different Lg-Ls test samples.

re-program in C/P is simulated, as shown in Fig. 6(a) and (c). During the 1st and 2nd program, a proportion of electrons in the charge-trap layer migrated towards adjacent cells, as shown in (i) and (ii) of Fig. 6(a) and (c). Thus, the density of empty trap sites decreases at the inter-cell region. The Poole-Frenkel model and Drift-Diffusion model are usually used to describe the process of LM [19], [23]–[26], and the probability of LM depends on the density of empty trap sites at the inter-cell region. Therefore, after re-program, LM is suppressed by the lateral migrated electrons, as shown in (iii) and (iv) of Fig. 6(a) and (c). In addition, as shown in Fig. 5(a), τ of LM in C/P increases slightly after re-program, which is due to the longer distance from empty trap sites. But in S/P case, due to the negligible LM of IVS after the 1st program, there is no visible LM improvement from re-program, and τ of LM is also almost unchanged after re-program, as shown in Fig. 5(b).

For the vertical charge loss improvement by re-program, the trapped electron density along the direction perpendicular to the channel at different moments is simulated, as shown in Fig. 6(b). After the 1st program, electrons de-trap from the BE-tunneling oxide to the poly-Si channel (black and blue lines). During the 2nd program, the same amount of electrons that induced V_{th} shift will be filled into both BE-tunneling oxide and charge-trap layer simultaneously (green line). Eventually, there are less electrons in the BE-tunneling oxide, which improves the vertical charge loss (green and red lines). Note that the simulation result of vertical charge loss in S/P is similar to that in C/P (result not shown). In addition, the increased τ of de-trapping in Fig. 5 implies that the energy level of trapped charge in BE-tunneling oxide is deeper after re-program, which is similar to the mechanism of 'refill' in the charge-trap layer of 2D NAND [7].

The IVS improvement by re-program scheme in different Lg-Ls test samples are evaluated. Fig. 7 shows the typical experimental results. In S/P case, the IVS improvement is not affected by Lg-Ls scaling down. While in C/P case, the IVS improvement increases as Lg-Ls scaling down. As mentioned above, the IVS in S/P is primarily attributed to vertical de-trapping, while in C/P is due to both vertical de-trapping and LM. As LM plays more significant role in cell retention with Lg-Ls scaling down, re-program can further improve LM in the advanced 3D NAND technologies.

IV. CONCLUSION

In this work, the mechanisms of re-program scheme for IVS improvement in CTM based 3D NAND device are investigated. As trapped charge in BE-tunneling oxide is primarily responsible for vertical charge loss of IVS in 3D NAND, re-program scheme can suppress vertical charge loss through reducing the trapped electrons in the BE-tunneling oxide. The increased τ of de-trapping implies that the energy level of trapped charge in BE-tunneling oxide is deeper after re-program. Also, LM can be suppressed by the lateral migrated electrons that occurred during the re-program. As LM plays more significant role in cell retention with Lg-Ls scaling down, re-program scheme is a potential approach to improve LM in the advanced 3D NAND technologies.

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