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Slit Field Plate Power MOSFET for Improvement of Figure-Of-Merits

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ABSTRACT A new low-voltage power MOSFET is proposed to improve the figure-of-merits (FOMs) for power loss reduction. Slit field plate (Slit FP) structure is effective to cope with both the on-resistance $R_{on}A$ reduction and high speed switching due to flat electric field distribution and low gate density by the slit oxide. Therefore, Slit FP power MOSFET achieves better $R_{on}A$-$R_{on}Q_{sw}$ and $R_{on}A$-$R_{on}Q_g$ tradeoff characteristics compared with conventional FP power MOSFET. TCAD simulation result shows 12% of $R_{on}A$, 11% of $R_{on}Q_{sw}$, and 20% of $R_{on}Q_g$ can be reduced simultaneously by the Slit FP power MOSFET compared with the conventional FP power MOSFET at the lowest $R_{on}A$ design.

INDEX TERMS Field plate, power MOSFET, on-resistance, $R_{on}Q_{sw}$, figure-of-merit.

I. INTRODUCTION

Power MOSFETs are the key devices for the high efficiency power converters. For the power loss reduction of the power MOSFETs, the conduction loss and the switching loss must be reduced. For this requirement, the on-resistance $R_{on}A$, $R_{on}Q_{sw}$, and $R_{on}Q_g$ are used as figure-of-merits (FOMs) to evaluate both the conduction loss and the switching loss. For the reduction of these FOMs, various device structures and process technologies have been developed [1].

Recently, Field-Plate (FP) structure has been employed for the FOMs reduction of low-voltage power MOSFETs. The FP structure is effective to reduce the $R_{on}A$ by the increase of drift layer doping concentration due to charge compensate concept and stress induced electron mobility enhancement [2]–[10]. In addition, the $R_{on}Q_{sw}$ can be reduced by small C_{gd} due to the shield effect of FP electrode. However, it is difficult to continue the $R_{on}A$ reduction trend only by the design parameter optimization [11]. Moreover, it cannot be obtained to reduce the $R_{on}A$ and the $R_{on}Q_{sw}$ simultaneously, because narrow lateral pitch increases the gate density, although the drift doping concentration can be increased [12]. This leads that high efficiency operation requires custom design for power loss reduction, because the ratio of conduction loss and switching loss depends on the switching frequency of the application circuit. Therefore, a new approach from the other direction is necessary for further loss reduction in all low-voltage power MOSFET applications.

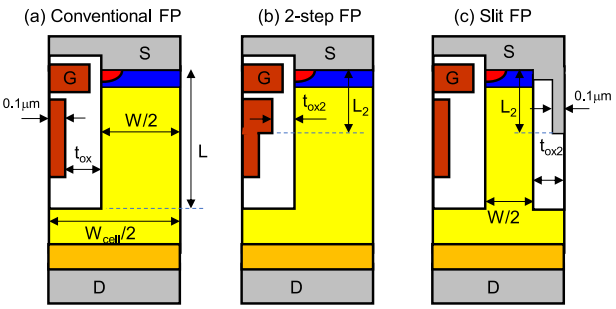

FIGURE 1. The device structure of (a) conventional FP power MOSFET, (b) 2-step FP power MOSFET, and (c) Slit FP power MOSFET.

In this paper, a new structure of Slit FP power MOSFET is proposed to improve the FOMs by flat electric filed and low gate density by the slit oxide.

II. DEVICE STRUCTURE AND OPTIMIZATION STEPS

Three types of 100 V-class FP power MOSFET were designed as shown in Fig. 1. The optimum design parameters for the minimum $R_{on}A$ are shown in Table 1. In the previous work [8], an advanced structure of 2-step FP power MOSFET was proposed and demonstrated better FOMs than the conventional FP power MOSFET by more flat electric field distribution due to thin FP oxide at upper FP region.

TABLE 1. Device parameters of FP-MOSFETs.

Parameters	Conventional FP [12]	2-step FP	Slit FP
W_{cell}	1.7μm	1.4μm	1.84μm
W	0.5μm	0.4μm	0.4μm
N_{D1}	8.1×10^{16} cm^{-3}	14×10^{16} cm^{-3}	14.3×10^{16} cm^{-3}
N_{D2}	3.3×10^{16} cm^{-3}	7.0×10^{16} cm^{-3}	7.7×10^{16} cm^{-3}
L	7.3μm	7.4μm	6.6μm
L_2	–	2.4μm	1.8μm
t_{OX}	500nm	400nm	370nm
t_{OX2}	–	200nm	150nm

In contrast, Slit FP power MOSFET has additional FP electrode connected to the source and slit oxide under the source electrode. The electric field distributions of three devices are shown in Fig. 2. 2-step FP power MOSFET obtains flat electric field distribution by 2-step FP oxide due to the charge compensate concept. In contrast, flat electric distribution in Slit FP structure is caused by the electric filed in the slit oxide [13], [14]. In addition, the additional FP electrode decreases C_{gd} due to the shield effect. In the Slit FP power MOSFET, the surface electric field is the lowest in three devices and breakdown point is the bottom of the drift region. It is effective to improve the avalanche withstanding capability and breakdown voltage stability, because the parasitic bipolar transistor action and hot carrier injection into the trench oxide can be avoided [15].

TCAD process and device simulations of Synopsys [16] were used to investigate these structures. In the process simulation, the mechanical stress induced by thermal oxidation was calculated. Then, the stress induced electron mobility enhancement was calculated in the device simulation. The fabrication process flow is shown in Fig. 3. Firstly, FP and gate electrodes are formed as same as the conventional FP power MOSFET [12]. Then, the second trench is formed by RIE and the trench is filled by oxidation. The additional FP is formed by RIE and poly Si filling. The p-base and n-source layers are formed after remove of surface oxide, and then source and drain electrodes are formed by metallization process.

The $R_{on}A$ was calculated from the on-state drain voltage V_{ds} at the drain current density J_d of 1 A/mm^2 and the gate-source voltage V_{gs} of 10 V. The breakdown voltage V_B was calculated from the V_{ds} at the J_d of 1 mA/mm^2. The Q_{sw} and Q_g were calculated at the supply voltage of 50 V, the J_d of 5 A/mm^2, and the V_{gs} of 10 V. The process margin from the minimum V_B of 110V was taken account for trench depth L, L_2, drift doping concentration N_{D1} and N_{D2} of $+/-10\%$, and oxide thickness t_{ox} and t_{ox2} of $+/-5\%$. The drift layer doping applies 2-step profile, each depth of which is half of the epi layer thickness.

The optimization steps considering with process margin were as follows. As the first step, the W, t_{ox}, and t_{ox2} typical values were fixed. Then, the L, L_2, N_{D1}, and N_{D2} typical values were optimized considering the above process margin from the minimum V_B. These calculations were executed for the other W, t_{ox}, and t_{ox2} conditions. Optimized parameters for the minimum $R_{on}A$ at three devices are summarized in Table 1.

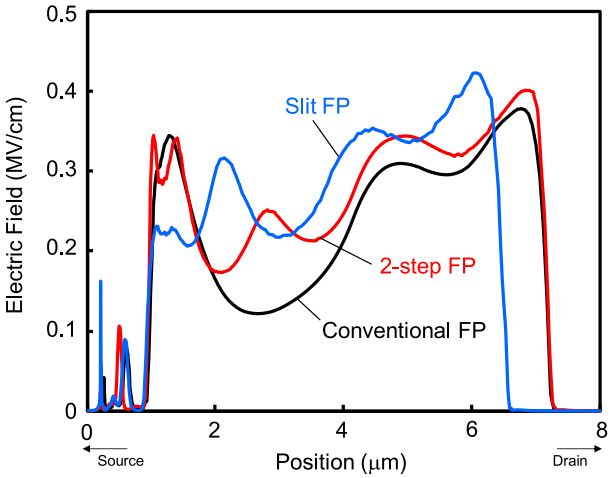

FIGURE 2. The electric field distributions at breakdown voltage in the drift layer at the distance of 0.1 mm from the FP oxide interface for conventional FP, 2-step FP and Slit FP power MOSFETs.

TABLE 2. Resistance breakdown and stress effect on $R_{on}A$ of FP-MOSFETs.

Parameters	Conventional FP [12]	2-step FP	Slit FP
R_{ch}	6.2mΩmm^2	5.1mΩmm^2	6.7mΩmm^2
R_{drift}	17.5mΩmm^2	14.5mΩmm^2	14.2mΩmm^2
R_{sub}	1mΩmm^2	1mΩmm^2	1mΩmm^2
$R_{on}A$ with Stress	24.7mΩmm^2	20.6mΩmm^2	21.9mΩmm^2
$R_{on}A$ without Stress	27.2mΩmm^2	22.1mΩmm^2	23.9mΩmm^2
$\Delta R_{on}A$ by Stress	9.0%	7.0%	8.4%
Maximum Stress	381MPa	424MPa	499MPa

III. SIMULATION RESULTS AND DISCUSSIONS

For three devices, $R_{on}A$ dependences on the lateral pitch W_{cell}, which is changed by W are shown in Fig. 4. The $R_{on}A$ is reduced with lateral pitch narrowing due to increase of the doping concentration and the stress induced electron mobility enhancement. However, too narrow lateral pitch structure increases the $R_{on}A$ for all device. This is because that L is increased with the lateral pitch narrowing dramatically due to the V_B decrease induced by the lateral electric field increase [11]. Therefore, the $R_{on}A$ reduction by lateral pitch narrowing is limited. 2-step FP power MOSFET achieves lower $R_{on}A$ than conventional FP power MOSFET with the narrower lateral pitch achieved by flat electric field. On the other hand, Slit FP power MOSFET can reduce the $R_{on}A$ even with wide pitch due to the flattest electric field distribution in three devices as shown in Fig. 2.

The resistance breakdown of three devices is shown in Table 2. The drift resistance R_{drift} is a dominant factor for

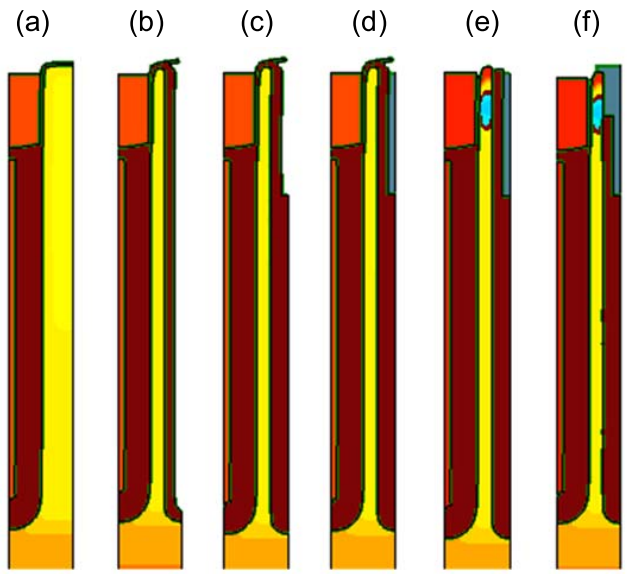

FIGURE 3. Fabrication process of Slit FP power MOSFET (a) FP electrode formation, (b) slit oxidation, (c) the second FP formation, (d) p-base and n-source diffusion, and (e) electrode formation.

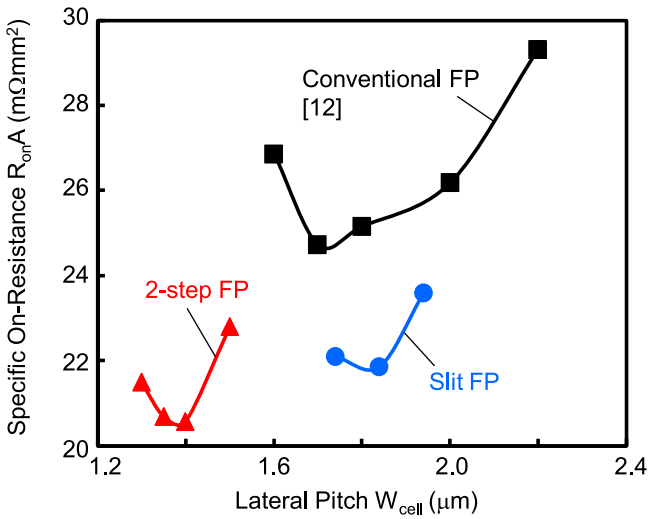

FIGURE 4. $R_{on}A$ dependence on the lateral pitch of conventional FP power MOSFET, 2-step FP power MOSFET, and Slit FP power MOSFET.

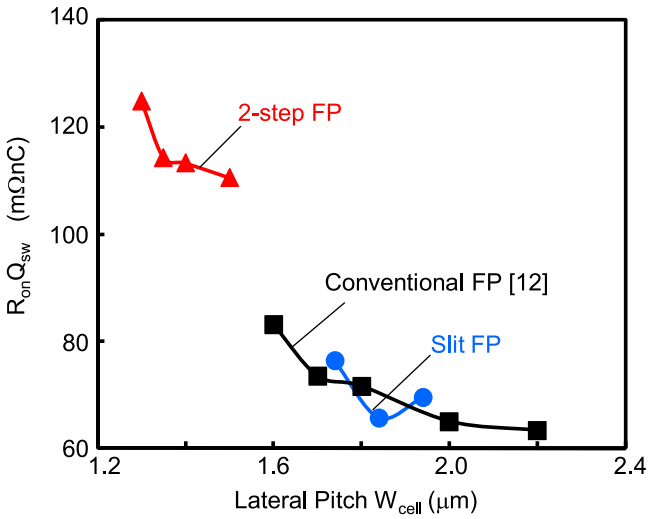

FIGURE 5. $R_{on}Q_{sw}$ dependence on the lateral pitch of conventional FP power MOSFET, 2-step FP power MOSFET, and Slit FP power MOSFET.

$R_{on}A$ in all devices due to 100 V-class power MOSFET. The R_{drift} is reduced in 2-step FP and Slit FP power MOSFETs, because the drift doping concentration can be increased by flat electric field distribution. However, the channel resistance R_{ch} of Slit FP power MOSFET is higher than that of 2-step FP power MOSFET due to wide lateral pitch. Therefore, 2-step FP is the lowest $R_{on}A$ in three devices. The minimum $R_{on}A$ of 2-step FP power MOSFET is 20.6 mΩ·mm^2, which is 17% lower than that of conventional FP power MOSFET. This is caused by the nearly ideal gradient FP structure. In contrast, the minimum $R_{on}A$ of Slit FP power MOSFET is 21.9 mΩ·mm^2, which is 12% lower than that of conventional FP power MOSFET due to flat electric field by the slit oxide. Higher $R_{on}A$ of Slit FP power MOSFET compared with the 2-step FP power MOSFET is caused by lower gate density.

The stress induced electron mobility enhancement was taken into account for the $R_{on}A$ simulation. In the previous work [10], it was estimated that the threshold silicon stress to cause a lot of crystal defects by cracking is about 500 MPa. Three devices were designed with the maximum mechanical stress within the threshold silicon stress in this work. The wafer stress induced by the trench oxide leads to not only local crack in the chip but also the wafer warpage. Therefore, to avoid errors in vacuum adsorption and wafer handling, the control of wafer warpage in process integration is necessary [17], [18].

The reduction of $R_{on}A$ by the stress induce electron mobility was less than 10% as shown in Table 2. Therefore, the effect of the increase of the drift layer doping concentration enabled by the lateral pitch narrowing is greater than that of the stress induced electron mobility enhancement and the lateral pitch optimization is the most important design point for minimization of $R_{on}A$.

The $R_{on}Q_{sw}$ dependence on lateral pitch of three devices are shown in Fig. 5. In contrast with the $R_{on}A$ characteristics, narrow lateral pitch increases the $R_{on}Q_{sw}$, because the Q_{sw}/A is increased with the gate density and the doping concentration. Therefore, it cannot be achieved to reduce $R_{on}A$ and $R_{on}Q_{sw}$ simultaneously [12]. The 2-step FP power MOSFET shows high $R_{on}Q_{sw}$, because gate-drain capacitance C_{gd} is increased with high drift doping concentration and high gate density by narrow lateral pitch as shown in Fig. 6. In contrast, the Slit FP power MOSFET shows lower $R_{on}Q_{sw}$ than 2-step FP power MOSFET, because low gate density by wide lateral pitch and additional FP reduces C_{gd}

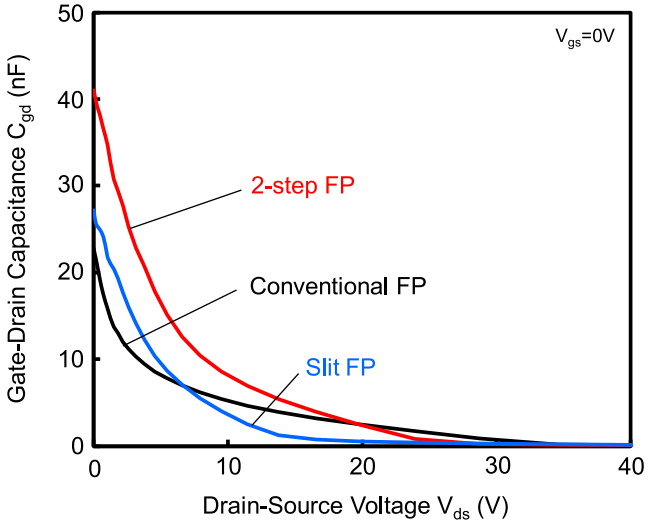

FIGURE 6. C_{gd}-V_{ds} characteristics of conventional FP power MOSFET, 2-step FP power MOSFET, and Slit FP power MOSFET.

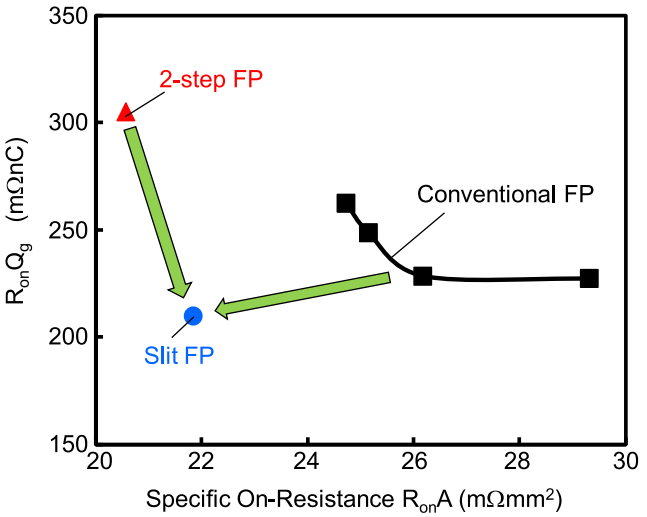

FIGURE 8. $R_{on}A$-$R_{on}Q_g$ tradeoff characteristics of conventional FP power MOSFET, 2-step FP power MOSFET and Slit FP power MOSFET.

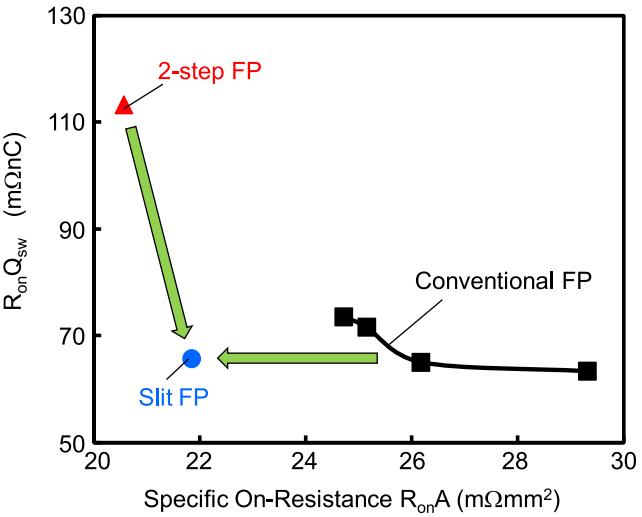

FIGURE 7. $R_{on}A$-$R_{on}Q_{sw}$ tradeoff characteristics of conventional FP power MOSFET, 2-step FP power MOSFET and Slit FP power MOSFET.

as shown in Fig. 6. Therefore, the Slit FP power MOSFET obtains to reduce $R_{on}A$ and $R_{on}Q_{sw}$ simultaneously.

$R_{on}A$-$R_{on}Q_{sw}$ and $R_{on}A$-$R_{on}Q_g$ tradeoff characteristics are shown in Figs. 7 and 8, respectively. The 2-step FP power MOSFET has high doping concentration and high gate density due to narrow lateral pitch. Although $R_{on}A$ can be reduced, Q_{sw}/A is increased. Therefore, the 2-step FP power MOSFET does not improve $R_{on}A$-$R_{on}Q_{sw}$ and $R_{on}A$-$R_{on}Q_g$ tradeoff characteristics. In contrast, the Slit FP power MOSFET shows better tradeoff characteristics, because the flat electric field distribution reduces the $R_{on}A$ compared with the conventional FP power MOSFET and the low gate density by the slit oxide avoids to increase Q_{sw}/A.

The Slit FP power MOSFET achieves 12% lower $R_{on}A$, 11% lower $R_{on}Q_{sw}$, and 20% lower $R_{on}Q_g$ simultaneously compared with the conventional FP power MOSFET at the lowest $R_{on}A$ design. From these results, although 2-step FP power MOSEFT is a good choice only for low switching frequency application from a viewpoint of the $R_{on}A$ reduction, the Slit FP power MOSFET is attractive for power loss reduction in all low-voltage power MOSFET applications.

IV. CONCLUSION

Slit FP power MOSFET was proposed to reduce $R_{on}A$, $R_{on}Q_{sw}$, and $R_{on}Q_g$ simultaneously. TCAD simulation results show that although 2-step FP power MOSFET is effective to reduce the $R_{on}A$ due to increase of doping concentration and narrow lateral pitch, the $R_{on}Q_{sw}$ is increased by high doping concentration and high gate density. In contrast, the Slit FP power MOSFET achieves lower $R_{on}A$ and $R_{on}Q_{sw}$ compared with the conventional FP power MOSFET, because the slit oxide induces flat electric filed distribution and high doping concentration even with low gate density. The Slit FP power MOSFET improves $R_{on}A$-$R_{on}Q_{sw}$ and $R_{on}A$-$R_{on}Q_g$ tradeoff characteristics and achieves 12% lower $R_{on}A$, 11% lower $R_{on}Q_{sw}$, and 20% lower $R_{on}Q_g$ simultaneously compared with the conventional FP power MOSFET at the lowest $R_{on}A$ design. From these results, although 2-step FP power MOSEFT is a good choice only for low switching frequency application from a viewpoint of the $R_{on}A$ reduction, the Slit FP power MOSFET is attractive for power loss reduction in all low-voltage power MOSFET applications.

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