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Capacitor Reused Gate Driver for Compact In-Cell Touch Displays

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ABSTRACT A thin-film transistor (TFT) integrated gate driver is proposed for compact in-cell touch display, where one capacitor is reused for both turning on low-level maintaining transistors via voltage coupling and maintaining the re-start charge during the touch sensing period. The gate terminal of buffer transistor is thus free of electrical stress during touch sensing period, and can be re-charged for the subsequent re-start period, leading to minimal variations in the transient response. With the capacitor reusing scheme and a capacitor stacking structure, the area of the single stage gate driver is decreased to 645 μm × 210 μm. The fabricated a-Si TFT gate driver with 8 cascaded stages shows that the rising and falling time variations among re-start and normal gate driver stages are less than 1 μs. Versatile touch sensing modes and bidirectional scanning functions are verified.

INDEX TERMS Capacitor reusing, gate driver, in-cell touch, bidirectional scanning, display.

I. INTRODUCTION

Gate driver circuit integration using thin-film transistors (TFTs) becomes important for the-state-of-the-art active matrix displays. Thanks to the gate driver integrations at the peripheral area, high resolution displays with narrow bezel, simplified module process and reduced cost can be achieved [1], [2]. Although already being widely used in TFT-LCD products of mobile phones, tablets, and TV displays, TFT integrated gate driver design is still challenging for the in-cell touch TFT-LCD display. For the conventional displays, consecutive row scanning pulses are provided by the gate driver for the whole display frame [3], [4]. In contrast, for the in-cell touch display, discontinuous row scanning pulses are required [5]. This is because gate driver output should be maintained with low voltage (i.e., V_L), during touch sensing periods, to minimize interferences from display driving signals. Furthermore, it is preferred to detect touch events evenly distributed within the display frame, instead of by the end of the display frame, for better display quality and reducing touch-sensing related display defects [6]. Therefore, for a high-end in-cell touch display, the gate driver is required to operate in a scanning-pausing mode, i.e., after outputting dozens of continuous scanning pulses of display addressing, the gate driver outputs pause for consecutive touch sensing periods. As the gate driver should re-start for display addressing after the touch detection period, the re-start charge should be well maintained within the touch sensing periods.

Previously, there were primarily two types of TFT integrated gate driver for in-cell touch display, depending on the location to store the re-start charge. Moon et al. demonstrated the first type gate driver, where the re-start charge is maintained by the gate electrode of buffer transistor, i.e., the main transistor with large width-to-length ratio for pulling-up and pulling-down the voltage level of loading capacitor and resistors of gate lines [7]. Although this type of gate driver exhibits concise circuit structure and fewer TFTs, the corresponding buffer transistor to store re-start charge is prone to undergo longer voltage stress compared with other buffer transistors of normal stages. For in-cell touch display with a-Si:H TFTs, the duty ratio variations of buffer TFT for different stages lead to significant line defects after

long operating time, especially for high temperature operations over long stressing time. Lin *et al.* demonstrated the second type gate drivers, to store re-start charge by incorporating additional capacitors [8]–[10]. Then, the voltage stressing conditions for buffer transistor of different gate driver stages can be retained almost the same, as all the buffer transistors are turned off for the touch sensing periods. However, the drawback is that the additional capacitor and the related switching TFTs seem complicated. Furthermore, the bi-directional gate scanning function is necessary for extending the display application range. However, it is not easy to implement TFT integrated gate driver with both bi-directional scanning and re-start charge maintaining functions for in-cell touch display [11]–[13].

In this paper, a capacitor reusable method is adopted to store the re-start charge within the touch sensing period. Then a new gate driver for in-cell touch display is proposed incorporating the proposed re-start module and the reused capacitor. In the following section, operations of a new in-cell touch gate driver circuit are presented firstly. And then details of the proposed capacitor reusable gate driver implementation using a-Si:H TFT process are discussed. Transient performances of fabricated circuit samples will be characterized through measurements at the final part.

II. THE PROPOSED GATE DRIVER

The schematic of the proposed capacitor reusable gate driver is shown in Fig. 1(a). The timing diagram of the proposed circuit is illustrated in Fig. 1(b). The single-stage circuit consists of bidirectional input module (T1 and T3), output module (T2 and C1), low-level-maintaining module (T4, T5, T6, T7 and C2), and re-start module (T8, T9, T10, T11 and T12). Here, C2 is coupled with CK to turn on the low-level-maintaining module, for eliminating feed-through noise at the output electrode for display periods. In addition to this basic function, C2 is also connected with the re-start module and maintaining the re-start charge during the touch sensing periods.

For every gate driver stage, the external signals and power sources, i.e., RCK, TP, V_{SS}, V_F, and V_B, are connected in the same manner as shown in Fig. 1. However, the connections of two complementary clock signals, i.e., CK and XCK, are different for adjacent gate driver stages. For odd (even) gate driver stages, drain electrodes of buffer transistors, i.e., T2, are connected with CK (XCK), while the gate electrodes of T7 and T8 are connected with XCK (CK). The bootstrapping operation and low-level-maintaining principle can be found in the previous publications [11]–[13]. Therefore, only the operations of the re-start module are described in detail here.

A. DISPLAY DRIVING PERIOD

To suppress the crosstalk noise between the display driving and the touch sensing, the voltage level of TP and RCK are kept low during the display period as shown in Fig. 1(b). Then, T9 and T12 are turned off to isolate the touch detection module with input and output modules. When CK switches

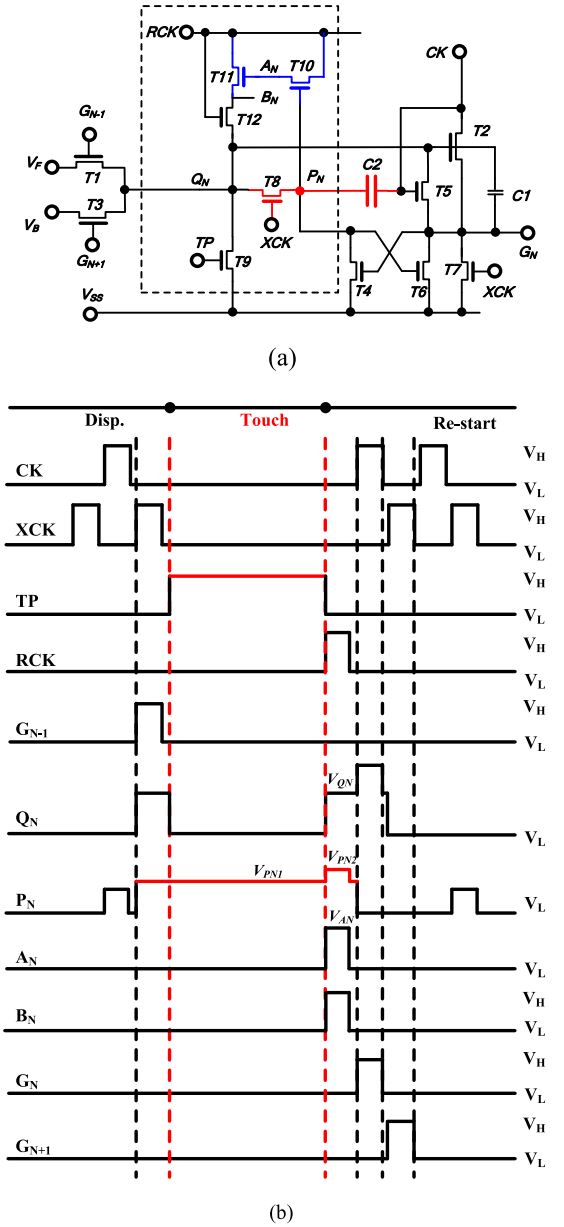

FIGURE 1. The proposed a-Si:H TFT gate driver for in-cell touch displays with (a) schematic of a single stage gate driver circuit, and (b) the timing diagram, with the display driving, touch sensing, and re-start periods.

to high, node P_N is coupled with high level through C2, and then T10 is turned on to remove the remaining charge on A_N. Meanwhile, T6 is also turned on to keep the gate driver output, i.e., G_N, at a low level. In other words, although the re-start module is inserted, the gate driving operations is not disturbed for the display period. The gate driver would experience the pre-charging, pulling-up, pulling-down, and low-level-maintaining processes successively, which are explained in [1] and [12].

B. TOUCH SENSING PERIOD

During the touch sensing period, the clock signals (CK and XCK) are switched to low, thus all the gate driver stages

output low level voltage. The level of TP is turned high to discharge Q_N through T9. Therefore, the line-by-line scanning of display driving is suspended to reduce the feed-through effects and noise voltage, which benefits increasing the signal-to-noise ratio of in-cell touch sensing. Meanwhile, the re-start charge for the consequent sub-frame display is maintained by C2, which has been charged through T8 in prior to the touch sensing period. As all the transistors connected to node P_N are turned off to prevent leakage currents, the re-start charge can be well maintained by C2 for the whole touch sensing period.

C. RE-START PERIOD

As the level of signal TP is switched to low, T9 is turned off. Then, RCK is switched to high level, i.e., V_H. Consequently, for different gate driver stages, whether Q_N is re-charged or maintained at low level is dependent on the charge storage state of C2. If the re-start charge is retained by C2, which is connected to node P_N, then T10 is turned on to pull up the gate electrode of T11. Consequently, Q_N can be re-charged through the serially connected T11 and T12. For the other gate driver stages, as there is no re-start charge stored by C2, T10 is kept off. Node A_N is maintained at low level. Therefore, Q_N is maintained at low level for the other gate driver stages.

In Fig. 1, the level of V_{PN} (i.e., V_{PN1}) for the touch sensing period can be expressed as

$$V_{PN1} = V_H - V_{TH} - \Delta V_0. \tag{1}$$

ΔV_0 is the voltage loss due to the leakage current. Due to the leakage currents of TFTs, the voltage waveform distortion on node P_N is inevitable in the touch sensing period. Thanks to the voltage bootstrapping method, node Q_N can be re-charged with a full voltage swing. Hence, for the consequent re-start period, the voltages associated with the internal nodes of the touch detection module can be expressed as follows.

$$V_{PN2} = V_{PN1} + \Delta V_{RCK} * C_{GST10}/C_{PN}. \tag{2}$$
$$V_{AN} = V_H + \Delta V_{RCK} * C_{GST11}/C_{AN}. \tag{3}$$
$$V_{BN} = V_H. \tag{4}$$
$$V_{QN} = V_H - V_{TH12}. \tag{5}$$

Note that the proposed gate driver has high flexibility for various display applications with different touch detection rates. By adjusting the timing sequence, i.e., the starting and duration time of TP and RCK signals, touch sensing operations can be placed between any two adjacent gate driver scanning pulses. Furthermore, the scanning direction can be regulated by changing the voltage polarity of V_F and V_B and the activation sequence of T1 and T3, which are controlled by G_{N-1} and G_{N+1}, respectively. In the case that V_F is at high level and V_B is at low level, the scanning sequence is $G_{N-1} \rightarrow G_N \rightarrow G_{N+1}$. Otherwise, if V_F is low and V_B is high, the scanning sequence is inverted as $G_{N+1} \rightarrow G_N \rightarrow G_{N-1}$.

TABLE 1. The electrical and geometrical parameters of the proposed gate driver.

Design parameter	Value
CK,XCK,RCK,TP	-10 V to 17 V
V_{SS}	-10 V
L	4.5 μm
$(W)_{T1,T3,T6,T9,T12}$	250 μm
$(W)_{T7,T10}$	200 μm
$(W)_{T2}$	2800 μm
$(W)_{T4}$	300 μm
$(W)_{T5}$	25 μm
$(W)_{T8,T11}$	100 μm
C1	1.2 pF
C2	1.6 pF

In addition, the proposed gate driving circuit features uniform transient response in the display-driving and re-start periods. When the re-start module is enabled, the node Q_N can be re-charged through T11 and T12. As node B_N is then charged with full voltage swing due to the bootstrapping principle as shown in (3) and (4), the driving ability of T12 is approximately the same with that of T1/T3. Then the driving ability derivations among the display driving periods and re-start periods can be decreased.

III. RESULTS AND DISCUSSIONS

For a-Si:H TFT in the integrated gate driver circuit, the thickness of gate metal layer (Mo/Al), gate insulating layer (SiNx), active layer (a-Si:H), source drain metal layer (Mo/Al), first passivation layer (SiNx), and ITO layer, are 200 nm, 400 nm, 200 nm, 180 nm, 400 nm, and 50 nm, respectively. Then, the equivalent gate insulating capacitance is 14.8 nF/cm^2. The electrical characteristics of discrete a-Si:H TFT samples are measured with Keithley 4200. Using the standard Level 1 current-voltage model of field-effect transistors, the key electrical parameters for the fabricated a-Si:H TFT samples can be obtained. The extracted threshold voltage is 0.26 V. The field-effect mobility is 1.0 cm^2/(V.s). The sub-threshold voltage swing is 1.8 V/dec.

SPICE simulations are performed to iteratively optimize the geometrical parameters of TFTs and capacitors. The voltage levels of the clock signals and the geometrical parameters of the transistors and capacitors in the proposed circuit are listed in Table 1. The proposed gate driver with 8 stages is fabricated by using the standard a-Si:H process. The fabricated single stage gate driver is shown in Fig. 2(a). As shown in Fig. 2(b), C1 and C2 are implemented with a vertical stack structure. Different from the previous dual-gate method [14], here the ITO layer is acting as the second capacitor electrode. Both the gate insulating layer and the passivation layer are employed for capacitor dielectric. Furthermore, the top ITO layer is connected to the gate metal layer through a contact hole. Then, the parallel capacitors are formed both between the gate metal and source metal layers, and between the ITO layer and source metal layer. Due to the stack capacitor structure, the layout area of a single stage gate driver can be decreased to 645 μm × 210 μm. Compared with the

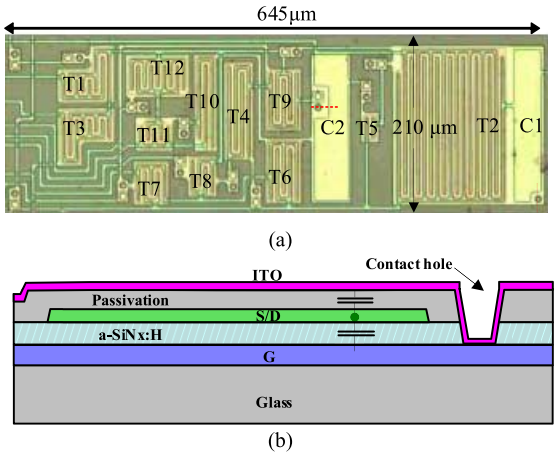

FIGURE 2. The optical image of the fabricated gate driver sample with a single stage(a), and the conceptual cross sectional view of the stack capacitor, i.e., C1 and C2 as shown in the single stage gate driver circuit (b).

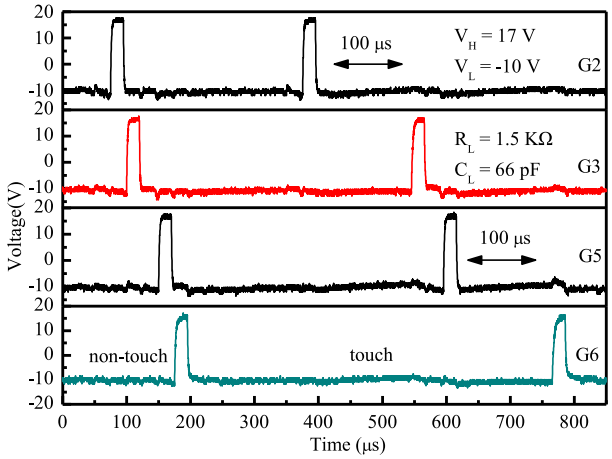

FIGURE 3. The measured 2nd, 3rd, 5th and 6th gate driver output in the display and re-start periods, for rising and falling time comparison.

conventional structure, the stack capacitor structure features an 11% reduction in the overall layout area.

During the measurements, the gate driver is connected to an external test board using a probe card with 32 needles, which is fixed on the probe station. The external testing board for TFT circuit evaluations comprises voltage source, voltage level shifter module, and timing controller on the basis of the FPGA board (XILINX ZYNQ 7000 platform), which is programmed through computer by using Verilog code. To mitigate the light effects, all the electrical performance characterizations are conducted on the dark manual probe station with ambient light shielded. The transient voltage waveforms are captured using the Tektronix oscilloscope (MDO3054). The output electrodes of the integrated gate driver are externally connected with loading resistor of 1.5 KΩ and loading capacitor of 66 pF, to mimic the RC loading condition of a 5.5-inch TFT-LCD mobile display. The high level and low level of clock and other touch-sensing controlling signals are 17 V and -10 V, respectively. The period of the complementary clock signals for display and a re-start period is 50 μs, with a duty ratio of 40%.

The measured transient output waveforms for the 2nd, 3rd, 5th, and 6th gate driver stages are shown in Fig. 3, for the consecutive display, touch sensing, and re-start periods, with $V_H = 17$ V and $V_L = -10$ V. In the display period, the line-by-line scanning waveforms are sequentially generated. In the touch sensing and re-start periods, there are two touch detection intervals with duration of 100 μs, one placed between the 2nd and 3rd pulse waveforms, and the other located between the 5-th and 6-th pulse waveforms. These results prove that the touch detection intervals can be flexibly arranged between the adjacent gate driver stages, by changing the turning sequence of TP and RCK signals. Thus, the proposed gate driver is suitable for diverse touch display modules. Although the measured voltage level of the gate driver output can reach V_H and V_L with full swing, there are observed variations between the rising (ΔTr) and falling (ΔTf) times of adjacent gate driver stages. On the other hand, for every single gate driver stage, taking the 3rd gate driver stage for example, ΔTr and ΔTf for the display and re-start periods are less than 1.0 μs. Therefore, the variations of rising time and falling time among different gate driver stages might be caused by the non-uniformity of the electrical characteristics of TFTs for diverse gate driver stages, almost being independent of the insertion of re-start module. As the fabricated gate driver sample is located at the peripheral zone of the mother glass, the electrical uniformity among diverse gate driver units is worse than that of the central display area.

The measured transient response and the extracted rising and falling time versus the high voltage level of clock signals, i.e., V_H, being increased from 15 V to 25 V are shown in Fig. 4. The first pulse belongs to the display period as shown in Fig. 4a. The second pulse is the re-triggered one after the touch sensing period with a width of 100 μs. It is observed that, for the 3rd gate driver output, the rising time of the first pulse and the second pulse are 2.6 μs and 3.2 μs, respectively, for V_H of 17 V. In other words, the measured ΔTr and ΔTf for the 3rd gate driver are 0.6 μs and 1.0 μs, respectively. As V_H is increased to 25 V, the measurement value of ΔTr and ΔTf are reduced to 0.1 μs and 0.2 μs, respectively. The reason for ΔTr and ΔTf decreasing is that, as expressed by (2), the increased V_H helps to enhance the bootstrapping ability of the re-start structure. These measurements verify that the proposed gate driver enables the decreasing of delay time variations between the display and re-start periods, provided that there is sufficient over-drive voltage to trigger the re-start module.

In Fig. 5, the measured consecutive output waveforms for the 1-st to 4-th gate driver stages for the forward (upper image) and backward (lower image) scanning modes, respectively, in the display period are illustrated. The same fabricated circuit sample is used to perform the gate driver bidirectional measurements, while only the polarities of V_F

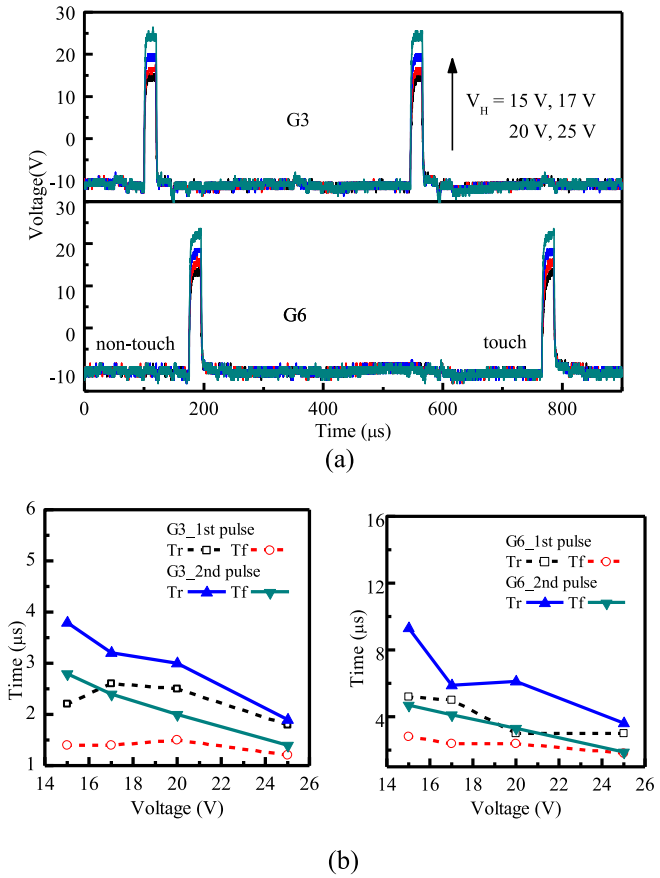

FIGURE 4. The measured transient response of the gate driver sample for the 3-rd and 6-th stages using increased V_H (a), the extracted rising time and falling time versus the increased V_H for the 3-rd (left) and the 6-th (right) gate driver stage (b).

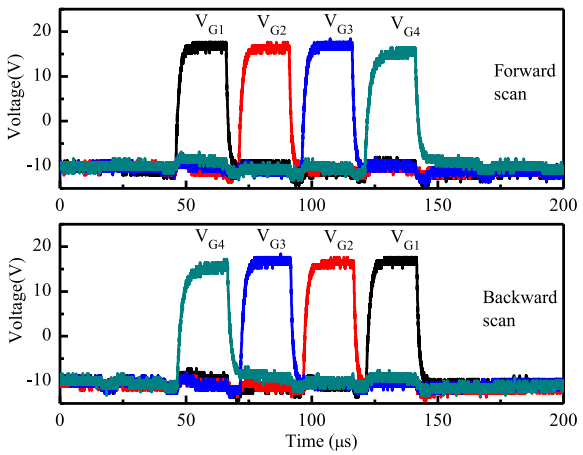

FIGURE 5. The measured 1st to 4th gate driver output in the forward scanning mode (upper one), and 1st to 4th gate driver output in the backward scanning mode (lower one).

and V_R are reversed. The timing of the start and reset signals are adjusted accordingly. This measurement proves that the proposed gate driver enables bi-directional gate scanning, with concise circuit topology and simple timing sequence. It is further observed that, for both the forward and backward scanning modes, the rising time and falling time of V_{G4} is larger than that of other stages by 2.0 μs approximately. These further confirm that the variations of the transient response of gate driver are caused by the spatial distributions of TFTs, rather than the pre-charge voltage distributions of gate driver units. Therefore, it is also important to maintain the electrical characteristic uniformity of transistors within the gate-driver integration area to improve display quality.

TABLE 2. Merits comparison among related works.

	Ref. [10]	Ref. [15]	Ref. [16]	This work
Structure	12T3C	11T3C	11T2C	12T2C
TFT type	a-Si:H	a-IGZO	LTPS	a-Si:H
Channel length (μm)	4.0	5.0	7.0	4.5
Control signals	8	5	5	7
Buffer TFT duty ratio	low	high	low	low
Layout area (μm×μm)	1393×122	N.A.	N.A.	645×210
Capacitor metal layers	2 layers	N.A.	N.A.	3 layers
Capacitor to keep charges	Extra cap. 0.81pF	Bootstrap cap. 2pF	Extra cap. 0.3pF	Coupling cap. 1.6pF
Bi-directional scan	Yes	No	No	Yes
Low-level maintain TFT	AC stress	DC stress	DC stress	AC stress

The merit comparisons with related works are listed in Table 2. It is clear that, due to the re-use of capacitor, the proposed gate driver shows the advantages of reduced layout areas, bi-directional scanning function, and reduced duty ratio of the low-level maintaining TFTs.

IV. CONCLUSION

A new TFT integrated gate driver with a bi-directional scanning function for an in-cell touch display is demonstrated. A new re-start module with a reused capacitor is proposed for compact circuit layout and uniform transient response. The conventional coupling capacitor to enable low-level-maintaining module, is re-used to store charge during the touch sensing period. The proposed gate driver is implemented using the standard 5-mask a-Si:H TFT process. To save layout area, vertically stacked capacitor structure, which incorporates the ITO-source/drain metal-gate metal layers, is employed. The fabricated gate driver sample is measured using FPGA board. Measurements demonstrate that the minimum operating voltage for the proposed gate driver is approximately 15 V. The variations of rising time and falling time for display and re-start periods can be reduced to within 0.2 μs. Test results also validate the bidirectional gate scanning function. Compared with conventional schemes, the proposed gate driver shows the advantages of reduced layout areas, and enhanced reliability and uniformity due to the reduction of duty ratio of the low-level maintaining TFTs. Therefore, the demonstrated compact bi-directional gate driver is promising for high-end in-cell touch display panels.

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