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Improved Low-Frequency Noise in Recessed-Gate E-Mode AlGaN/GaN MOS-HEMTs Under Electrical and Thermal Stress

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ABSTRACT 1/f noise provides essential information on the interface trapping effect as well as the scattering mechanism in transistors. In this work, a systematic 1/f noise study has been carried out on the recessed-gate enhancement-mode (E-mode) GaN MOS-HEMTs under electrical and thermal stress together with the depletion-mode (D-mode) counterpart. Low-frequency (1-1000 Hz) measurement has been performed at room (25 °C) and elevated (100 °C) temperatures at different carrier densities at the drain bias of 2 V and 10 V. The results show the E-mode device has much better noise characteristics under high voltage and high temperature compared with the D-mode counterpart. Moreover, charge-noise model reveals that the improved noise behavior of the E-mode device at high density and high drain bias at 100 °C originating from the energy band alignment at high biases, where the D-mode device suffers from extra charge trapping scattering in the gate edge near the gate-to-drain access region.

INDEX TERMS GaN MOS-HEMTs, 1/f noise, trapping effect, phonon scattering, carrier-number-fluctuation, mobility-fluctuation.

I. INTRODUCTION

High electron mobility transistors (HEMTs) based on AlGaN/GaN have shown great potential in high-frequency and high-power electronic applications because of the superior electrical properties such as wide bandgap, high electron mobility, high breakdown field and high thermal conductivity [1]–[3]. In particular, extensive research efforts have been devoted to E-mode devices which are highly desirable for simplification of circuit design and fail-safe operation [4]–[10]. In spite of the proven excellent DC performance under E-mode operation, systematical low-frequency noise study under stress is still lacking, and needs to be addressed due to reliability concerns. Mobility and carrier number fluctuations generated from scattering and trapping/de-trapping process provide important information for the device operation under various electrical and thermal conditions [11]–[13]. As a result, the 1/f noise measurement is one of the most important efficient tools commonly used to analyze the dynamic trapping and scattering behaviors for the entire device including the channel region and the access region [14]–[17].

In this work, D-mode and E-mode GaN MOS-HEMTs have been fabricated on the same sample simultaneously. The two types of devices share an identical fabrication process except for the E-mode device recess etching step. To obtain detailed insights on the physical mechanisms of D-mode and E-mode devices, low-frequency characterizations at room temperature and elevated temperature of 100 °C under small and high transverse electric field have been carried out in both devices at different gate biases. The origins and dominant factors of low-frequency noise have been discussed in detail, which can be used not only to evaluate the device reliability, but also for further performance optimization.

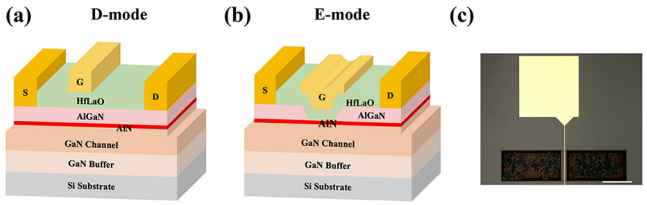

FIGURE 1. Cross section schematic views of the D-mode (a) and E-mode (b) GaN MOS-HEMTs. (c) Optical micrograph of the fabricated GaN MOS-HMET, the scale bar is 50 μm.

II. DEVICE FABRICATION

Fig. 1 (a) and (b) show the cross-section schematic views of the D-mode and E-mode AlGaN/GaN MOS-HEMTs. The two types of devices share the same substrate consisting of a 4-μm C-doped GaN buffer, a 300-nm undoped GaN channel, a 1-nm AlN interlayer, and a 20-nm $Al_{0.25}Ga_{0.75}N$ barrier. Multi-energy ion implantation was applied for device isolation to define the active region. A 60-nm AlN layer grown by plasma-enhanced atomic layer deposition (PEALD) served as etching mask for the following window opening process using photolithography. Atomic layer etching (ALE) process was adopted to realize the recessed-gate structure for E-mode device. This process consists of a thin layer oxidation of the top AlGaN barrier and the subsequent oxide removal by low-power BCl_3 dry etching. The precisely controlled process results in a steep side wall and a uniform channel region [18]. After removal of etching mask, source-drain ohmic contacts can be formed using multilayer metal deposition of Ti/Al/Ni/Au and rapid thermal annealing (RTA) at 870 °C for 30 s in nitrogen atmosphere. The extracted contact resistance is around 0.36 Ω·mm from transfer-length-method (TLM). 20 nm HfLaO composite layer consists of 8 cycles of HfO_2 deposition using precursors of $[(CH_3)(C_2H_5)N]_4Hf$ and ozone followed by 1 cycle of La_2O_3 deposition using precursors of $La((iPr_2N)_2CH)_3$ and ozone at 300°C. Finally, the gate region was patterned by electron beam lithography (EBL) and Ni/Au gate metal stack was deposited by electron beam evaporation (EBE). Fig. 1 (c) depicts the optical micrograph of the fabricated GaN MOS-HEMT, both D-mode and E-mode MOS-HEMTs have a gate length of 1 μm, a gate-source spacing of 3 μm, a gate-drain distance of 5 μm and a gate width of 50 μm.

III. RESULTS AND DISCUSSION

Due to the existence of two-dimensional electron-gas (2DEG) induced by spontaneous polarization and piezoelectric polarization at the heterostructure interface, the typical GaN MOS-HEMTs are intrinsically normally-on [19]. In our recessed-gate devices, the reduced AlGaN barrier layer thickness leads to the depletion of 2DEG density, resulting in positive shift of threshold voltage (V_{TH}) and eventually reaches E-mode operation. Fig. 2 (a) shows the transfer characteristics and gate leakage current of D-mode and E-mode devices in semi-log scale at room-temperature. Owing to the high-quality high-κ gate dielectric, the gate leakage current is suppressed with a high on/off current ratio over 10^{10}. It also enables an efficient electro-static gate control with a low subthreshold swing of 77 mV/dec for both types of devices. When the measurement temperature is elevated to 100 °C, the gate leakage current increases by an order of magnitude, with a current on/off ratio still larger than 10^9.

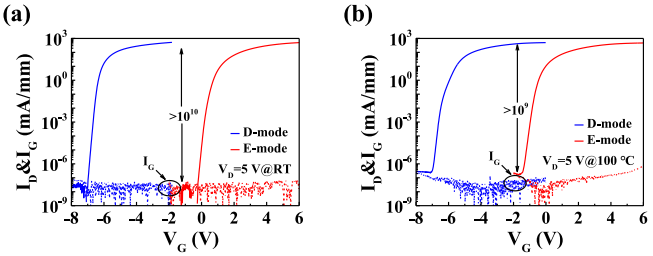

FIGURE 2. Transfer characteristics and gate leakage of D-mode and E-mode devices in semi-log scale at room-temperature (a) and elevated temperature of 100 °C (b).

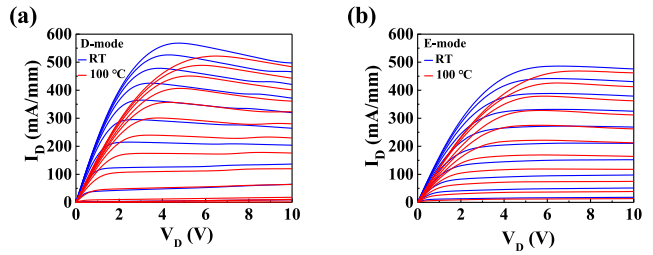

FIGURE 3. Comparison of output characteristics measured at room-temperature and 100 °C of D-mode (a) and E-mode (b) devices.

Fig. 3 (a) and (b) compare the output characteristics measured at room-temperature and 100 °C of D-mode and E-mode devices, respectively. The maximum output current and the ON-resistance degrade slightly at the elevated temperature under the same gate overdrive voltage (V_{GT}) for both devices, mainly because of the mobility decreases from enhanced phonon scattering. The apparent negative differential resistance (NDR) of D-mode device under high drain bias and high current density is much more pronounced than E-mode device at different temperatures, indicating that the self-heating from hot carriers and current collapse induced by charge trapping is more severe.

Current fluctuations at low frequencies typically leads to the generation of 1/f noise. A thorough investigation of the low-frequency noise is needed to understand the physical mechanisms which can also help improve the device reliability. The drain current in transistors can be expressed as:

$$I \propto qN\mu \tag{1}$$

And the current fluctuation can be formulated as:

$$\delta I \propto q(\delta N)\mu + qN(\delta\mu) \tag{2}$$

where q is the charge of elementary charge, N is the number of charge carriers and μ is the carrier mobility [20]. Carrier

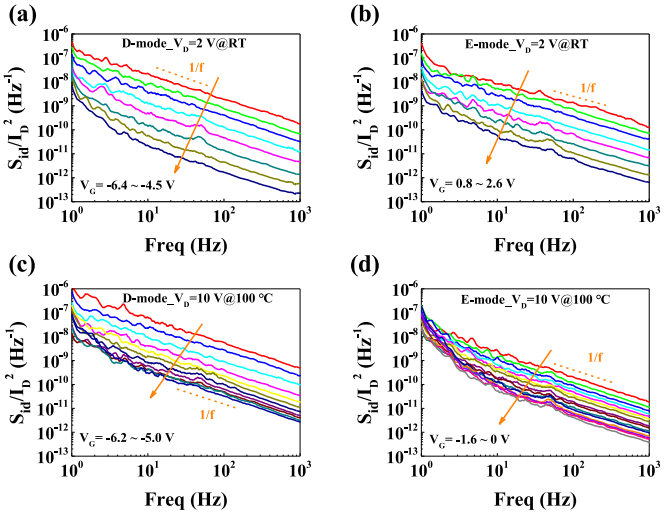

FIGURE 4. Noise spectral density (S_{id}/I_D^2) as a function of frequency for D-mode at 2V and RT (a), E-mode at 2V and RT (b), D-mode at 10V and 100 °C (c), E-mode at 10V and 100 °C (d).

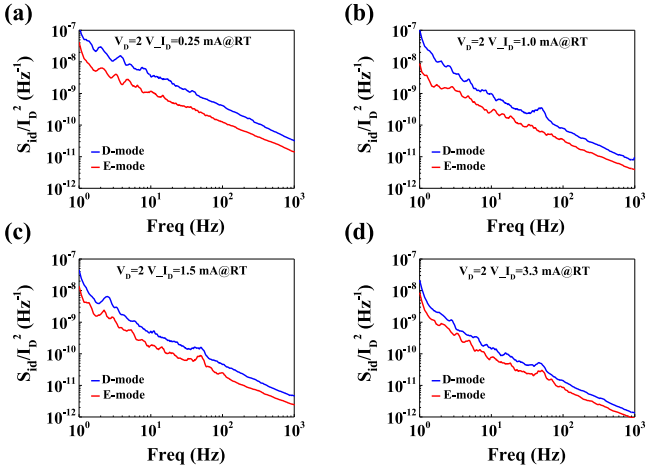

FIGURE 5. Noise spectral density (S_{id}/I_D^2) as a function of frequency for D-mode device and E-mode devices at V_D = 2 V at room-temperature with drain current of 0.25 mA (a), 1 mA (b), 1.5 mA (c) and 3.3 mA (d).

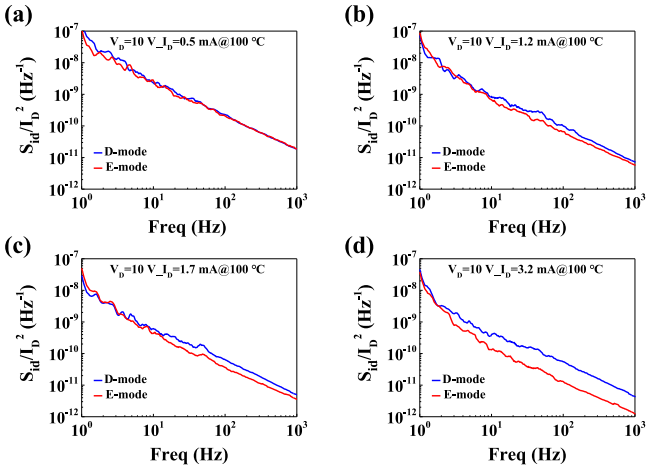

FIGURE 6. Noise spectral density (S_{id}/I_D^2) as a function of frequency for D-mode device and E-mode devices at V_D = 10 V at 100 °C with drain current of 0.5 mA (a), 1.2 mA (b), 1.7 mA (c) and 3.2 mA (d).

number-fluctuation and mobility-fluctuation are the two commonly used models to describe the 1/f noise behavior. Fig. 4 (a)-(d) show a series of normalized current noise spectral density (S_{id}/I_D^2) as a function of frequency for D-mode and E-mode devices at V_D = 2 V and V_D = 10 V under room-temperature and 100 °C, respectively. Both D-mode and E-mode devices exhibit typical 1/f dependence and can be quantitatively characterized by:

$$S_{id} = A_0 I_D^2 / f^{\gamma} \tag{3}$$

where S_{id} is the current noise power spectral density, A_0 is the noise amplitude, I_D is the drain current through the device channel, f is the frequency, and γ is the frequency exponent close to 1 in both types of devices [21]. In subthreshold region, the 2DEG density increases with gate voltage with stronger electrostatic screening effect. The trapping and de-trapping rate of trap centers with large time constant decreases drastically at high frequency. Thus, the current fluctuation is suppressed at increased gate voltage and frequency, leading to a decreased noise power spectral density.

In order to investigate the noise mechanisms of device operation type, the low-frequency noise characteristics for both devices under various conditions are compared systematically. The (S_{id}/I_D^2) as a function of frequency for D-mode and E-mode devices under identical drain current at V_D = 2 V are shown in Fig. 5. It is obvious that the noise level of D-mode devices is always higher than E-mode device and the difference between the two reduces when the drain current increases. However, when the drain voltage increases to 10 V at an elevated temperature of 100 °C, the low-frequency noise behaviors start to change oppositely as shown in Fig. 6. At low drain current density, the noise level of D-mode and E-mode devices nearly overlaps with each other, but deviates quickly when the drain current increases, exhibiting much lower noise level for the E-mode devices. Similarly, the input-referred noise spectral density (S_{vg}) for fixed drain voltage and different gate bias of both D-mode and E-mode devices has the same trend as S_{id} and thus is not shown here, where the slope γ of the $1/f^{\gamma}$ dependence in all spectra range is close to 1 and no generation-recombination (g-r) noise bulges are observed, indicating that the flicker noise dominates the low-frequency in GaN MOS-HEMTs. The low-frequency noise is at a quite low level compared with the previous works [22]–[24] at the same frequency thanks to the high-quality of heterostructure and gate dielectric in this work.

To analyze the evolution trend of the noise characteristics, the energy band of D-mode and E-mode devices in the subthreshold region where the noise measurement is carried out is compared as shown in Fig. 8. With the reduced thickness of AlGaN barrier layer, the V_{TH} shifts positively as discussed in Fig. 2. In order to induce the same carrier density, the applied gate overdrive voltage V_{GT} for both types of devices is about 5 V. As a result, the gate voltage of D-mode

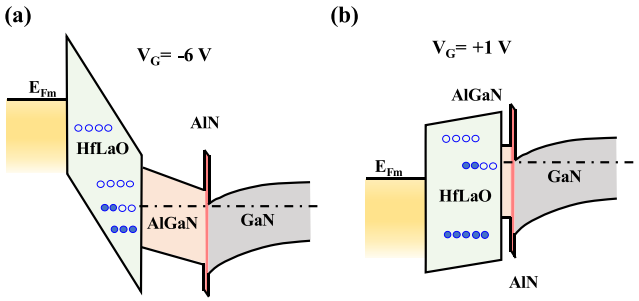

FIGURE 7. Energy band diagram of D-mode (a) and E-mode (b) MOS-HEMTs in subthreshold region.

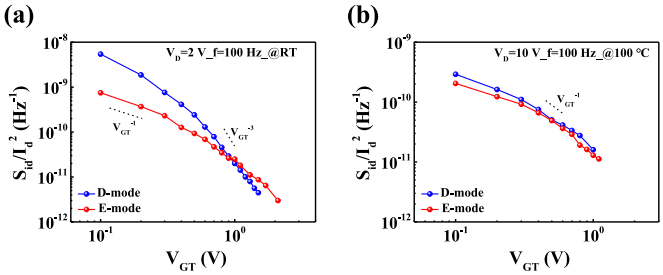

FIGURE 8. Noise spectral density (S_{id}/I_D^2) as a function of gate overdrive voltage (V_{GT}) for D-mode device and E-mode devices at V_D = 2 V at room-temperature (a) and at V_D = 10 V at 100 °C (b).

and E-mode devices is set as $V_G = -6$ V and $V_G = 1$ V, respectively. As shown in Fig. 7 (a), the large negative gate voltage of D-mode device forms a triangular barrier at the surface of HfLaO dielectric, while the small gate voltage of E-mode device causes much less bending in the energy band of HfLaO as shown in Fig. 7 (b). Therefore, there are more bulk and interface traps in the D-mode devices participating in carrier trapping and de-trapping process, resulting in increased current fluctuations. In addition, the diffusion time of carriers in D-mode device is much longer than E-mode device due to the thicker AlGaN barrier layer, responding more efficiently to the low frequencies. For the above reasons, the noise spectral density of D-mode device is notably larger than E-mode device at small electric field region with $V_D = 2$ V. When the drain current increases, the influence of the traps reduces gradually and the high carrier density effectively screens the interface scattering, thus the noise level difference of the two types of devices reduces as shown in Fig. 5. However, the evolution trend of the noise behavior is opposite when V_D and temperature increase to 10 V and 100 °C, respectively. At elevated temperature alone, the thermally-activated charged trapping induced mobility fluctuation is enhanced and thus dominates in both cases, which narrows the difference of noise spectral density for the E-mode and D-mode devices. On the other hand, when the drain voltage increases to 10 V, a local electric field peak emerges near the gate edge in the gate-to-drain access region due to the large negative V_{GD} beyond pinch-off. This field is much higher in the D-mode case due to the threshold voltage difference of 7 V which is known to cause extra charge trapping scattering, similar to the current collapse behavior. Therefore, when the drain current increases, the screening effect from the increased carrier density will be much more efficient for the E-mode device as can be observed in Fig. 6d.

The contribution of contact noise is also analyzed. Since the total resistance between source and drain is $R = R_{ch}+R_c$, where the R_{ch} is channel resistance and R_c is contact resistance. Following the derivation in earlier work [25],[26], the measured noise spectral density S_R can be written as:

$$S_R = S_{R_{ch}} + S_{R_c} = \frac{R_{ch}^2 \alpha_{ch}}{f N_{ch}} + S_{R_c} \approx \frac{e\mu R_{ch}^3 \alpha_{ch}}{f L_{ch}^2} + S_{R_c} \quad (4)$$

where f, μ, L_{ch} and α_{ch} are frequency, electron mobility, channel length and Hooge parameter, respectively. $N_{ch} = L_{ch}^2/e\mu R_{ch}$ is the total number of carriers in the channel. Since the first term of the equation (4) is proportional to $V_{GT}{}^{-3}$, and the second term is proportional to $V_{GT}{}^{-1}$, the gate-bias dependence of noise spectral density is an effective method to distinguish different sources of the device under test. The analysis of $S_{id}/I_D{}^2$ versus gate overdrive voltage (V_{GT}) at different drain bias conditions and test temperature are shown in Fig. 8. The R_{ch} is larger than R_c at room-temperature when the V_{GT} is relatively low for both D-mode and E-mode devices because of the low carrier density in the channel, where $S_{id}/I_D{}^2$ is proportional to $V_{GT}{}^{-1}$. When V_{GT} further increases, the R_{ch} decreases gradually and becomes comparable with R_c in the D-mode devices, leading to a different $S_{id}/I_D{}^2$ trend with $V_{GT}{}^{-3}$ dependence. While in E-mode device, $S_{id}/I_D{}^2$ is still approximately proportional to $V_{GT}{}^{-1}$due to the R_{ch} degradation in gate recessing. When the drain bias increases to 10 V at an elevated temperature of 100 °C, enhanced electric field-induced trapping/de-trapping and phonon scattering cause the increase in R_{ch} which becomes larger than R_c, changing the $S_{id}/I_D{}^2$ dependence to $V_{GT}{}^{-1}$ in both D-mode and E-mode devices. The gate overdrive voltage dependence of $S_{id}/I_D{}^2$ indicates the noise is mainly generated from gate region and varies under different bias and temperature conditions.

Previous charge-noise model has proposed a combination of noise component capacitively coupled to gate voltage and a resistor-like component [27]. In our device structure, the gate edge near to drain (in access region) plays an important role in the transport especially under a large drain bias which will cause extra charge scattering as mentioned above. This access region is essentially not electric-statically coupled to the gate and thus can be regarded a noise source in series with the channel region. Thus, the total noise spectrum density of GaN MOS-HEMTs can be described as:

$$\frac{S_{\mathrm{id}}}{I_D^2} = S_{input}\left(\frac{g_m}{I_D}\right)^2 + A \quad (5)$$

where the first and last items represent the noise associated with the gated region and the access region, respectively. The major difference of D-mode and E-mode devices is

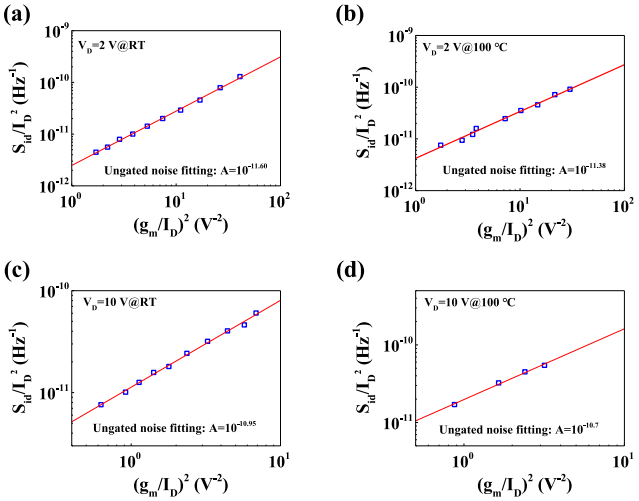

FIGURE 9. Noise spectral density (S_{id}/I_D^2) as the function of the transconductance to drain current ratio squared $(g_m/I_D)^2$ at 100 Hz for D-mode device with V_D = 2 V at room-temperature (a), V_D = 2 V at 100 °C (b), V_D = 10 V at room-temperature (c) and V_D = 10 V at 100 °C (d).

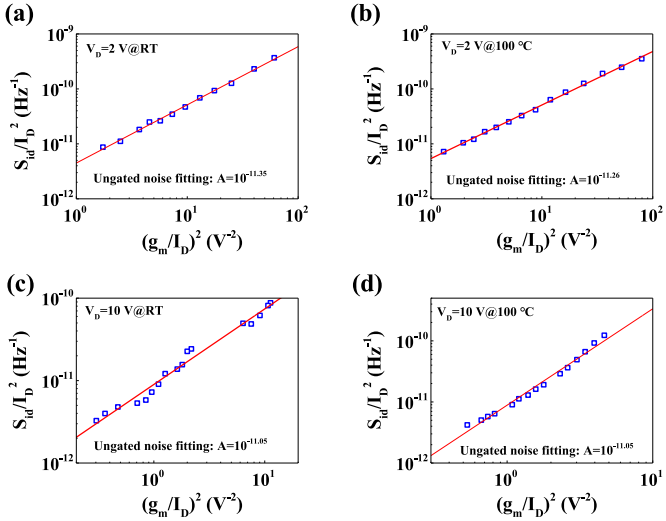

FIGURE 10. Noise spectral density (S_{id}/I_D^2) as the function of the transconductance to drain current ratio squared $(g_m/I_D)^2$ at 100 Hz for E-mode device with V_D = 2 V at room-temperature (a), V_D = 2 V at 100 °C (b), V_D = 10 V at room-temperature (c) and V_D = 10 V at 100 °C (d).

the threshold voltage shift from the reduced barrier thickness which results in the difference of effective traps. As depicted in Fig. 5 and Fig. 6, both devices follow similar trend at each condition, indicating the same physical mechanisms. The noise generates at access region near the gate edge can affect the total noise behavior depending on various bias and temperature conditions. In order to further discuss the effect, the last term of equation (5) is discussed in detail. Fig. 9 and Fig. 10 show the total normalized noise spectral density (S_{id}/I_D^2) as a function of the transconductance to drain current ratio squared $(g_m/I_D)^2$ under different measurement conditions of D-mode and E-mode devices, respectively. The carrier number fluctuation generated at the access region (i.e., ungated region) can be expressed by the parameter A and the value can be obtained through liner fitting of (S_{id}/I_D^2) and $(g_m/I_D)^2$. With the increase of V_D and temperature, the influence of access region on low-frequency becomes more evident for both types of devices owing to the extra charge trapping induced current fluctuations originated from the electric field peak near the gate edge of L_{GD}.

To investigate the difference between D-mode and E-mode devices, the comparisons of the extracted parameter A are carried out using the relative change at different voltage and temperature as plotted in Fig. 11. It is noticeable that the change of measurement conditions has much more pronounced impact on D-mode device whether it is V_D or temperature. When the temperature changes alone, the relative change of parameter A for both the E-mode and D-mode device is minimal. However, when V_D increases to 10 V alone, the relative change of parameter A for D-mode is larger than 4 while for E-mode is about 2, indicating that the carrier number fluctuation induced by carrier trapping/de-trapping is more severe in D-mode device at high drain bias. When the two conditions are added up, the relative change of parameter A for D-mode is about 8 while for E-mode keeps about 2.

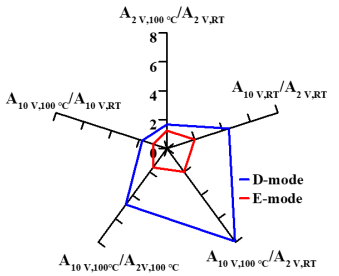

FIGURE 11. The relative change of parameter A at different V_D and temperature for D-mode and E-mode devices.

This shows that the extra trap charge scattering source near gate edge region is much more susceptible for the D-mode under high drain bias and high temperature, indicating better reliability in the recessed-gate E-mode devices.

IV. CONCLUSION

High-performance recessed-gate E-mode AlGaN/GaN MOS-HEMTs have been fabricated. 1/f noise measurement under different voltage bias and different measurement temperatures have been carried out to systematically investigate the current fluctuation mechanism. The difference between D-mode and E-mode is systematically studied in at high drain bias and high temperature. Charge trapping levels in the non-recessed D-mode MOS-HEMTs can induce significant current fluctuations compared with the recessed-gate E-mode devices. The main origin of the extra charge scattering comes from the trapping behavior near the gate edge in the gate-to-drain access region. The recessed-gate E-mode device using ALD high-κ HfLaO dielectric shows much better noise characteristics at high drain bias and high temperature. These results offer viable approaches for further optimizations of

reliability issues for high performance E-mode AlGaN/GaN MOS-HEMTs.

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