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# Phenomenological Model of Gate-Dependent Kink in I-V Characteristics of MoS<sub>2</sub> Double-Gate FETs

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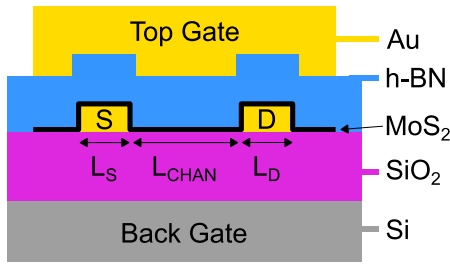
**ABSTRACT** A phenomenological model, accounting for interface states at metal-semiconductor contacts, is proposed to explain particular gate-bias-dependent kinking in I-V characteristics sometimes observed in MoS<sub>2</sub> FETs. The effect is studied in double-gate FETs by varying top-gate voltage ( $V_{TG}$ ) and bottom-gate voltage ( $V_{BG}$ ), with the MoS<sub>2</sub> semiconductor layer overlying source/drain (S/D) metal contacts in contact regions. The kink in  $I_D$ - $V_{TG}$  characteristics is observed for small negative  $V_{BG}$  but not for large negative  $V_{BG}$ . The model divides the FET into S/D and channel regions, with bias-dependent S/D resistance ( $R_{SD}$ ) and channel resistance ( $R_{CHAN}$ ), and with S/D regions having an additional interface state distribution (additional to any interface states associated with semiconductor/dielectric interfaces in the channel region) due to an imperfect metal-semiconductor interface where MoS<sub>2</sub> overlies S/D metal. The additional interface states are modeled as a Gaussian distribution of acceptor-like states in the upper region of the semiconductor bandgap. When  $R_{SD} \geq R_{CHAN}$  ( $V_{BG}$  less negative), filling of these acceptor-like states as  $V_{TG}$  increases creates a kink in  $I_D$ - $V_{TG}$  characteristics since  $R_{SD}$  is a major component of overall resistance limiting drain current,  $I_D$ . Conversely, when  $R_{SD} \ll R_{CHAN}$  ( $V_{BG}$  more negative), filling of these acceptor-like states as  $V_{TG}$  increases does not create an  $I_D$ - $V_{TG}$  kink since  $R_{SD}$  is not the major component of resistance limiting  $I_D$ . The model highlights 1) metal-semiconductor interface states need to be accounted for when modeling MoS<sub>2</sub> FETs, and 2) importance of forming metal-semiconductor interfaces with low interface state density to avoid I-V kinks which are detrimental for analog applications.

**INDEX TERMS** MoS<sub>2</sub>, double-gate FET, I-V kink, interface states, phenomenological model.

## I. INTRODUCTION

Formation of FETs with transition metal dichalcogenide (TMD) semiconductors is an active area of research [1]–[6]. Double-gate FETs are readily formed with a TMD channel, e.g., MoS<sub>2</sub>, bound on each side by a dielectric, with a top and bottom gate formed above and below the top and bottom dielectric, respectively [7], [8]. For a conventional MoS<sub>2</sub> double-gate FET (DGFET), MoS<sub>2</sub> overlies (or underlies) source / drain (S/D) metal contacts. Accordingly, imperfect interfaces that can impact DGFET I-V characteristics, e.g., due to interface states, are the source (and drain) metal / MoS<sub>2</sub> interface, and top (and bottom) dielectric / MoS<sub>2</sub> interface. Dielectric / MoS<sub>2</sub> interface states can

degrade sub-threshold slope [9] or introduce kinks in top-gated DGFET  $I_D$ - $V_{TG}$  but with no dependence shown on the bottom gate voltage,  $V_{BG}$  [10]. Metal / MoS<sub>2</sub> interface states can cause high, non-ohmic S/D resistance ( $R_{SD}$ ) resulting from high Schottky-type contact resistance ( $R_C$ ) due to Fermi-level pinning at the interface and associated large Schottky barrier [11], [12]. Kinks in FET  $I_D$ - $V_G$  characteristics have been reported due to metal / silicon interface states in S/D regions of bulk-silicon Schottky-barrier FETs [13], and due to metal / IGZO interface states at the drain edge of stressed single-gate IGZO FETs [14]. In MoS<sub>2</sub> FETs, high non-ohmic  $R_{SD}$  more generally results from high Schottky-type  $R_C$  caused by low doping of MoS<sub>2</sub> (i.e., low residual



**FIGURE 1.** Schematic cross-section of the MoS<sub>2</sub> DGFET, with the MoS<sub>2</sub> semiconductor layer overlying source / drain metal contacts.

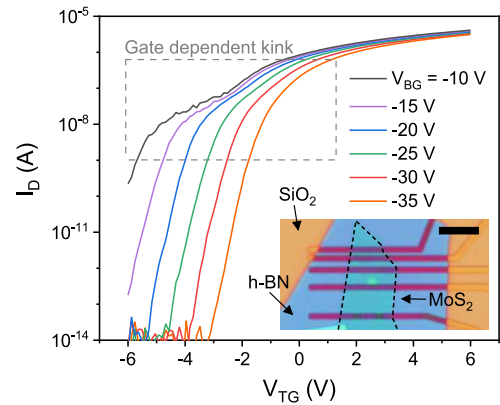
charge density) in contact regions due to difficulty achieving high doping in MoS<sub>2</sub> [15], [16] leading to reliance on electrostatic gating of contact regions to reduce R<sub>C</sub> [17]. For conventional MoS<sub>2</sub> DGFETs, only one gate, e.g., top gate, electrostatically dopes both the contact and channel regions while both gates electrostatically dope the channel [18]. Thus, even with electrostatic gating, the Schottky-type R<sub>C</sub> and overall S/D resistance (R<sub>SD</sub>) of MoS<sub>2</sub> DGFETs can be large relative to channel resistance (R<sub>CHAN</sub>) for various top and bottom gate biases. For biases in which R<sub>SD</sub> is large relative to R<sub>CHAN</sub> (i.e., S/D regions are important), we expect that if electrostatic gating of S/D regions is affected by metal / MoS<sub>2</sub> interface states, e.g., by filling of interface states as V<sub>TG</sub> increases, then the effect of these interface states will be apparent in I<sub>D</sub>-V<sub>TG</sub> characteristics.

In this letter, we present a simple phenomenological model to explain observed top and bottom gate bias dependence of kinked MoS<sub>2</sub> DGFET I<sub>D</sub>-V<sub>TG</sub> characteristics, which is not explained by prior models [10]. First, we describe DGFET fabrication and I<sub>D</sub>-V<sub>TG</sub> characteristics. Second, we develop equations of a phenomenological model which includes a Gaussian distribution of acceptor-like interface states in S/D regions, unlike prior models. Third, we compare the model to our experimental DGFET I<sub>D</sub>-V<sub>TG</sub> characteristics, showing excellent agreement between modeled and experimental I<sub>D</sub>-V<sub>TG</sub>. Lastly, we summarize this work's impact on modeling and fabrication of MoS<sub>2</sub> DGFETs. While most of our data and analysis is with DGFETs, the results also apply to single gate FETs.

## II. DEVICE FABRICATION AND MEASUREMENTS

MoS<sub>2</sub> DGFET fabrication utilizes a heavily-doped n-type Si substrate as the bottom gate with 285 nm of SiO<sub>2</sub> as bottom-gate dielectric. Ni/Au (4 nm / 12 nm) S/D metal contacts were formed by e-beam lithography (EBL), thermal metal evaporation (TME), and liftoff. Exfoliated MoS<sub>2</sub> (bilayer) was placed on top of S/D metal contacts. An exfoliated h-BN flake was transferred to overlay the MoS<sub>2</sub> and S/D metal, to serve as the top-gate dielectric. Finally, Cr/Au (3 nm / 50 nm) top gate and contact pads were patterned by EBL, TME, and liftoff. Each S/D metal contact length (L<sub>S</sub>, L<sub>D</sub>) is 1.5 μm; the channel length (L<sub>CHAN</sub>) is 3 μm (Fig. 1).

Figure 2 shows measured DGFET I<sub>D</sub>-V<sub>TG</sub> characteristics, for varying V<sub>BG</sub>, with an I<sub>D</sub>-V<sub>TG</sub> kink at less negative V<sub>BG</sub>



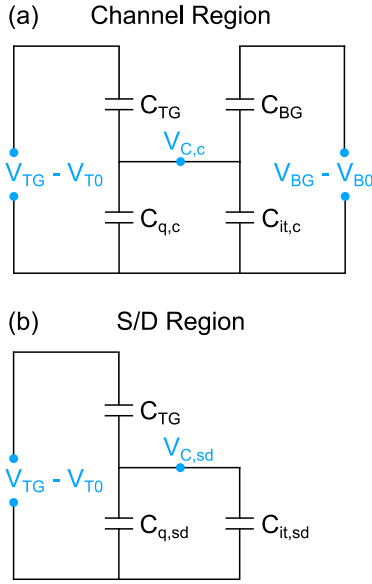
**FIGURE 2.** Measured I<sub>D</sub>-V<sub>TG</sub> characteristic, for varying V<sub>BG</sub>, of the conventional MoS<sub>2</sub> double-gate FET. V<sub>D</sub> = 100 mV. Inset: optical micrograph of the double-gate MoS<sub>2</sub> FET before top gate patterning. Scale bar of inset: 5 μm.

(≥ -25 V), but with no I<sub>D</sub>-V<sub>TG</sub> kink at more negative V<sub>BG</sub> (-30 V, -35 V). The I<sub>D</sub>-V<sub>TG</sub> kink occurs when the gate being swept can electrostatically dope MoS<sub>2</sub> in contact regions, i.e., the top gate.

It is noted that not all fabricated devices (utilizing placement of exfoliated layers onto underlying layers) show these particular I<sub>D</sub>-V<sub>TG</sub> kinks. We observe these particular I<sub>D</sub>-V<sub>TG</sub> kinks in ~25% of our devices. However, it is important to understand the origin of these kinks so that appropriate improvements in MoS<sub>2</sub> FET fabrication can be implemented to avoid these I<sub>D</sub>-V<sub>TG</sub> kinks, which are detrimental for analog applications. For example, improvements in MoS<sub>2</sub> FET fabrication can include optimization of pre-layer placement surface cleaning or post-layer placement annealing at particular steps in the FET fabrication flow so as to improve particular interfacial properties; accordingly, it is important to determine which of the interfaces is the cause of these I<sub>D</sub>-V<sub>TG</sub> kinks as is discussed in the next section.

## III. RESULTS AND DISCUSSION

We next develop equations for a model which includes a Gaussian distribution of acceptor-like interface states (neutral when empty, negatively charged when full, with an energy distribution determined by a fit between modeled and experimental current-voltage characteristics as discussed below) in S/D regions (associated with an imperfect metal / MoS<sub>2</sub> interface where MoS<sub>2</sub> overlies metal contacts), unlike in prior models. Following Jiménez [19] but with modified channel and S/D regions, Fig. 3 shows equivalent capacitive circuits for the MoS<sub>2</sub> DGFET. Figure 3(a) shows the circuit for the channel region; both V<sub>TG</sub> and V<sub>BG</sub> affect channel charge. V<sub>TG</sub>-V<sub>TG0</sub> and V<sub>BG</sub>-V<sub>BG0</sub> are internal voltages from top and bottom gates; V<sub>TG0</sub> and V<sub>BG0</sub> are treated as parameters to fit to experimental data [10], [19]. C<sub>TG</sub> and C<sub>BG</sub> are the top and bottom gate dielectric capacitances, associated with the top h-BN dielectric and bottom SiO<sub>2</sub> dielectric, respectively. Associated with the channel, C<sub>q,c</sub> is the quantum capacitance and C<sub>it,c</sub> is the capacitance due



**FIGURE 3.** (a) Equivalent capacitive circuit in the channel region. (b) Equivalent capacitance circuit in the source / drain contact region, for the conventional MoS<sub>2</sub> double-gate FET.

to the combination of interface states from top and bottom dielectric / MoS<sub>2</sub> interfaces, for thin channel films, as in [10]. Figure 3(b) shows the circuit for S/D regions; only  $V_{TG}$  affects charge (and  $R_{SD}$ ) in the MoS<sub>2</sub> overlying S/D metal contacts since  $V_{BG}$  is screened by the metal contacts. Associated with MoS<sub>2</sub> overlying source (drain) metal contacts,  $C_{q,s}$  ( $C_{q,d}$ ) is the quantum capacitance and  $C_{it,s}$  ( $C_{it,d}$ ) is the capacitance due to the combination of interface states from the source (drain) metal / MoS<sub>2</sub> interface and top dielectric / MoS<sub>2</sub> interface. At low  $V_{DS}$ , we assume same values in S/D regions, i.e.,  $C_{q,s} = C_{q,d} \equiv C_{q,sd}$ , and  $C_{it,s} = C_{it,d} \equiv C_{it,sd}$ .

Equations for charge in MoS<sub>2</sub> and interface states in the channel region (Fig. 3(a)) are:

$$Q_{q,c} + Q_{it,c} = [(V_{TG} - V_{TG0}) - V_{C,c}] \times C_{TG} + [(V_{BG} - V_{BG0}) - V_{C,c}] \times C_{BG} \quad (1)$$

$$Q_{q,c} = q \int_{E_{C,c}}^{\infty} DOS_{2D} \times f(E) dE \quad (2)$$

$$Q_{it,c} = q \int_{E_{mid}}^{E_{C,c}} (D_{it,u} + \alpha \times D_{it,g}) \times f(E) dE \quad (3)$$

where  $Q_{q,c}$  is channel charge corresponding to  $C_{q,c}$ ,  $Q_{it,c}$  is interface charge corresponding to  $C_{it,c}$ ,  $E_{C,c}$  is the semiconductor conduction band energy in the channel ( $E_{C,c} = qV_{C,c}$ ),  $E_{mid}$  is the midgap energy,  $DOS_{2D}$  is the 2D density of states of MoS<sub>2</sub>,  $f(E)$  is the Fermi function,  $D_{it,u}$  is an assumed uniform-in-energy density of interface states (to match modeled and experimental FET sub-threshold slope [9]) and  $D_{it,g}$  is a Gaussian distribution of interface states (to be discussed later) both corresponding to  $C_{it,c}$ ;  $\alpha$

equals 1 or 0 depending if  $D_{it,g}$  is included in the channel region. At low  $V_{DS}$ , we assume  $Q_{q,c}$  and  $Q_{it,c}$  are each constant along the channel.

Using (1)-(3),  $E_{C,c}$ ,  $Q_{it,c}$ , and  $Q_{q,c}$  can be calculated;  $R_{CHAN}$  (and dependence on  $V_{TG}$ ,  $V_{BG}$ ) is then determined from:

$$R_{CHAN} = \frac{L_{CHAN}}{W\mu Q_{q,c}} \quad (4)$$

where  $W$  is channel width, and  $\mu$  is electron mobility in MoS<sub>2</sub>.

Equations for charge in the MoS<sub>2</sub> and interface states in S/D contact regions (Fig. 3(b)) are:

$$Q_{q,sd} + Q_{it,sd} = [(V_{TG} - V_{TG0}) - V_{C,sd}] \times C_{TG} \quad (5)$$

$$Q_{q,sd} = q \int_{E_{C,sd}}^{\infty} DOS_{2D} \times f(E) dE \quad (6)$$

$$Q_{it,sd} = q \int_{E_{mid}}^{E_{C,sd}} (D'_{it,u} + D_{it,g}) \times f(E) dE \quad (7)$$

where  $Q_{q,sd}$  is charge in the MoS<sub>2</sub> overlying S/D metal contacts corresponding to  $C_{q,sd}$ ,  $Q_{it,sd}$  is interface charge corresponding to  $C_{it,sd}$ ,  $E_{C,sd}$  is the semiconductor conduction band energy in the S/D region ( $E_{C,sd} = qV_{C,sd}$ ),  $D'_{it,u}$  is a uniform-in-energy density of interface states ( $\sim 0.5 \times D_{it,u}$  ( $\sim 0.5$  is utilized since there is only a top dielectric / MoS<sub>2</sub> interface in S/D regions) and  $D_{it,g}$  is a Gaussian distribution of acceptor-type interface states (associated with the metal / MoS<sub>2</sub> interface) both corresponding to  $C_{it,sd}$ .  $D_{it,g}$  is modeled as:

$$D_{it,g} = N_{it,g} \times \exp \left[ - \left( \frac{(E_C - E_{it,g}) - E}{W_{it,g}} \right)^2 \right] \quad (8)$$

with peak density  $N_{it,g}$  located at energy  $E_{it,g}$  below the conduction band, and Gaussian distribution width,  $W_{it,g}$ .

Using (5)-(8),  $E_{C,sd}$ ,  $Q_{it,sd}$ , and  $Q_{q,sd}$  can be calculated;  $R_{SD}$  (and dependence on  $V_{TG}$ ) is then determined from:

$$R_{SD} = K \times \frac{L_{SD}}{W\mu Q_{q,sd}} \quad (9)$$

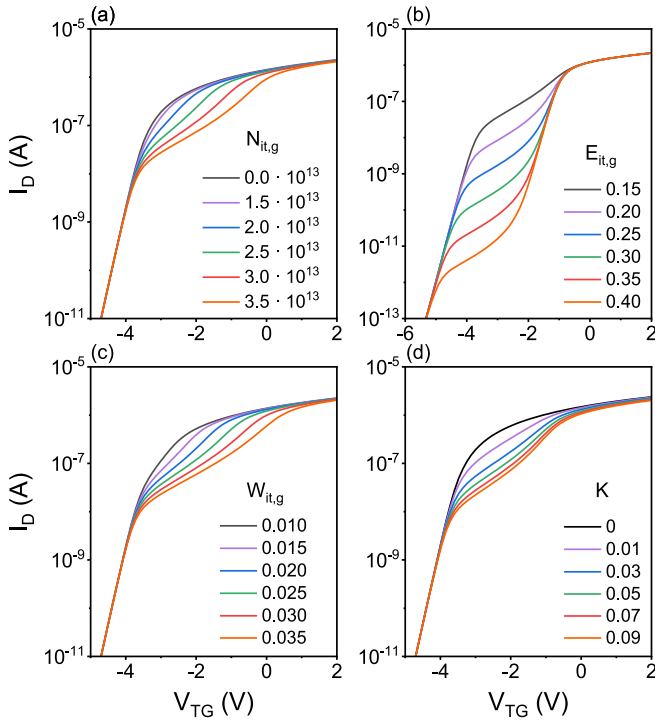
where (9) is derived from a transmission line model for metal / semiconductor regions [20],  $L_{SD} = L_S + L_D$ ,  $K$  is a multiplier factor (chosen to best fit modeled  $I_D$ - $V_{TG}$  to experimental  $I_D$ - $V_{TG}$ ), and  $K \times L_{SD}$  represents the transfer length; (9) is valid if  $K \ll 1$  such that  $\tanh(1/K) \sim 1$  [20]. (It will be shown that  $K = 0.05$ , i.e.,  $K \ll 1$ , enables a best fit between modeled and experimental  $I_D$ - $V_{TG}$ ; thus, (9) is valid).

Lastly, we solve for  $I_D$  vs.  $V_{TG}$  and  $V_{BG}$ , using:

$$I_D = V_D / (R_{CHAN} + R_{SD}) \quad (10)$$

$$I_D = V_D / \left( \frac{1}{W\mu} \left( \frac{L}{Q_{q,c}} + \frac{K \times L_{SD}}{Q_{q,sd}} \right) \right) \quad (11)$$

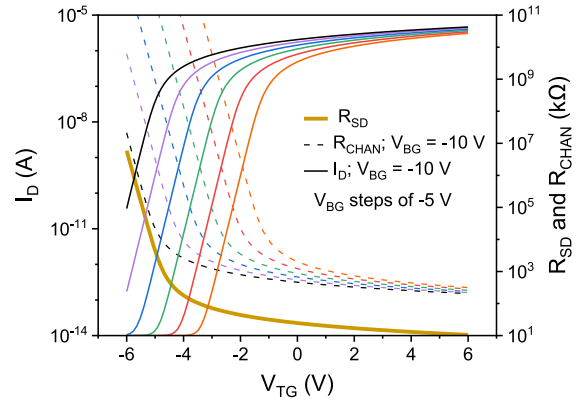
We now compare modeled versus measured  $I_D$ - $V_{TG}$  characteristics showing that excellent agreement can be achieved.



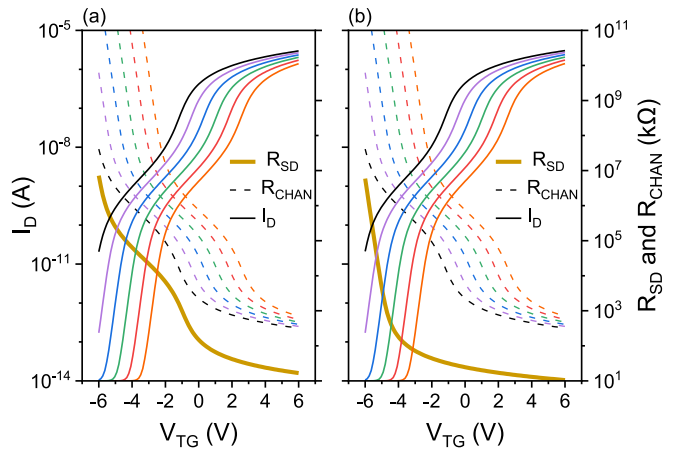
**FIGURE 4.**  $I_D$ - $V_{TG}$  characteristics, at fixed  $V_{BG} = -20$  V, for (a) varying  $N_{it,g}$  at fixed  $E_{it,g} = 0.15$  eV,  $W_{it,g} = 0.035$  eV,  $K = 0.05$ , (b) varying  $E_{it,g}$  at fixed  $N_{it,g} = 3 \times 10^{13}$   $\text{eV}^{-1}\text{cm}^{-2}$ ,  $W_{it,g} = 0.035$  eV,  $K = 0.05$ , (c) varying  $W_{it,g}$  at fixed  $N_{it,g} = 3 \times 10^{13}$   $\text{eV}^{-1}\text{cm}^{-2}$ ,  $E_{it,g} = 0.15$  eV,  $K = 0.05$ , and (d) varying  $K$  at fixed  $N_{it,g} = 3 \times 10^{13}$   $\text{eV}^{-1}\text{cm}^{-2}$ ,  $E_{it,g} = 0.15$  eV,  $W_{it,g} = 0.035$  eV.  $V_D = 100$  mV. (It is noted that the choice of fixed model parameters utilized in Figs. 4 (a)–(d) is based on iterative analysis showing that these fixed model parameters result in a good fit between modeled and experimental  $I_D$ - $V_{TG}$ , as described in later figures.)

(It is noted that only DC  $I_D$ - $V_{TG}$  characteristics are measured and modeled; thus, while the kink effect should be frequency-dependent according to the capture-emission time of interface states, interface state parameters such as capture-emission time constants that affect AC characteristics are not included in this model.) Model values corresponding to Figs. 1 and 2 are extracted for  $C_{TG}$ ,  $C_{BG}$ ,  $V_{TG0}$ ,  $V_{BG0}$ ,  $D_{it,u}$ ,  $L_{CHAN}$ ,  $L_{SD}$ ,  $W$ , and  $\mu$ . Figure 4 shows the effect on  $I_D$ - $V_{TG}$  of varying individual model parameters in (8) for  $D_{it,g}$  ( $N_{it,g}$ ,  $E_{it,g}$ , or  $W_{it,g}$ ) and of varying the model parameter,  $K$ , in (9) for  $R_{SD}$ , while fixing the other model parameters. From Fig. 4, more kinking in  $I_D$ - $V_{TG}$  is observed with increasing  $N_{it,g}$ ,  $W_{it,g}$  and  $K$ , and with a downwards shift in kinking observed with increasing  $E_{it,g}$ . Accordingly, appropriate adjustment of these parameters, using the trends in  $I_D$ - $V_{TG}$  characteristics in Fig. 4 as a guide, can enable a fit between modeled and experimental  $I_D$ - $V_{TG}$ , as shown in subsequent figures.

Figures 5–7 show modeled  $I_D$ - $V_{TG}$ , for varying  $V_{BG}$ , for four cases: 1)  $D_{it,g} = 0$  in the channel ( $\alpha = 0$ ) and S/D regions, 2)  $D_{it,g} \neq 0$  in the channel ( $\alpha = 1$ ) and S/D regions, 3)  $D_{it,g} \neq 0$  in the channel ( $\alpha = 1$ ) region only, and 4)  $D_{it,g} \neq 0$  in the S/D region only ( $\alpha = 0$ ). Figure 5 shows modeled  $I_D$ - $V_{TG}$ , for varying  $V_{BG}$ , for case 1.



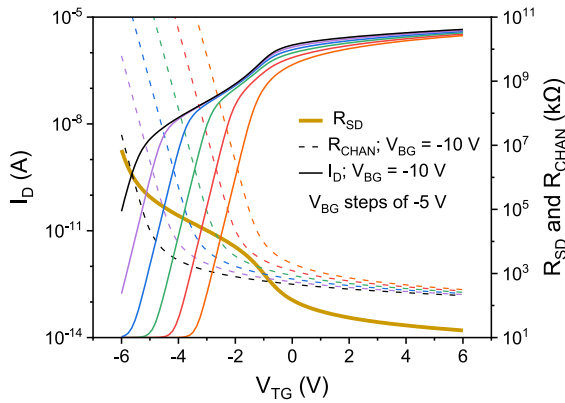
**FIGURE 5.**  $I_D$ - $V_{TG}$  characteristics, for varying  $V_{BG}$ , with  $D_{it,g} = 0$  in channel and S/D regions.  $K = 0.05$ ,  $V_D = 100$  mV.



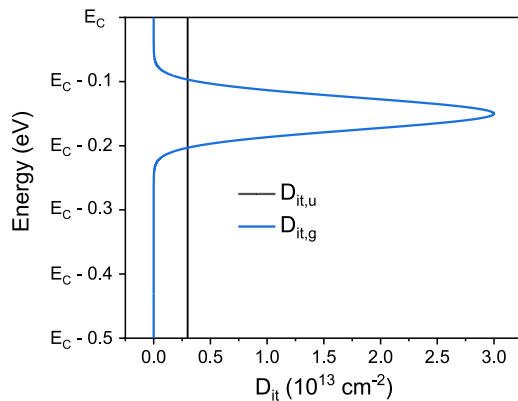
**FIGURE 6.** (a)  $I_D$ - $V_{TG}$  characteristics, for varying  $V_{BG}$  (starting at  $V_{BG} = -10$  V, with  $V_{BG}$  steps of  $-5$  V) for (a)  $D_{it,g} \neq 0$  in both the channel ( $\alpha = 1$ ) and S/D regions, (b)  $D_{it,g} \neq 0$  in the channel ( $\alpha = 1$ ) region only.  $N_{it,g} = 3 \times 10^{13}$   $\text{eV}^{-1}\text{cm}^{-2}$ ,  $E_{it,g} = 0.15$  eV,  $W_{it,g} = 0.035$  eV,  $K = 0.05$ ,  $V_D = 100$  mV.

No  $I_D$ - $V_{TG}$  kinks are observed, unlike experimental  $I_D$ - $V_{TG}$  characteristics (Fig. 2). Figure 6(a) shows modeled  $I_D$ - $V_{TG}$ , for varying  $V_{BG}$ , for case 2. Kinks in  $I_D$ - $V_{TG}$  are observed; however, the kinks are observed for all  $V_{BG}$  unlike experimental  $I_D$ - $V_{TG}$  (Fig. 2). Figure 6(b) shows modeled  $I_D$ - $V_{TG}$ , for varying  $V_{BG}$ , for case 3. Like Fig. 6(a),  $I_D$ - $V_{TG}$  kinks are observed for all  $V_{BG}$ . The kink behavior in Figs. 6(a)–(b), for cases 2 and 3, is consistent to the expectation that when  $R_{CHAN} \geq R_{SD}$ , filling of acceptor-like states located in the channel region as  $V_{TG}$  increases creates an  $I_D$ - $V_{TG}$  kink since  $R_{CHAN}$  is the major component of overall resistance limiting  $I_D$ ; since  $R_{CHAN} \geq R_{SD}$  for all  $V_{BG}$ , the  $I_D$ - $V_{TG}$  kink is observed for all  $V_{BG}$ .

Figure 7 shows  $I_D$ - $V_{TG}$ , for varying  $V_{BG}$ , for case 4 ( $D_{it,g} \neq 0$  in the S/D regions only). For this case, the kinks in the modeled  $I_D$ - $V_{TG}$  characteristics match to experimental  $I_D$ - $V_{TG}$  characteristics (Fig. 2), namely, kinks are pronounced for less negative  $V_{BG}$  but disappear for more negative  $V_{BG}$ . The kink behavior in Fig. 7 is thus consistent



**FIGURE 7.**  $D_{it,g} \neq 0$  in the S/D region only ( $\alpha = 0$  in the channel region).  $N_{it,g} = 3 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ ,  $E_{it,g} = 0.15 \text{ eV}$ ,  $W_{it,g} = 0.035 \text{ eV}$ ,  $K=0.05$ ,  $V_D = 100 \text{ mV}$ .



**FIGURE 8.**  $D_{it,u}$  and  $D_{it,g}$ -energy distribution which results in a good match between the modeled (Fig. 7) and experimental  $I_D$ - $V_{TG}$  characteristics (Fig. 2).

to the expectation that when  $R_{SD} \geq R_{CHAN}$  ( $V_{BG}$  less negative), filling of these acceptor-like states (located in S/D regions only) as  $V_{TG}$  increases creates a kink in  $I_D$ - $V_{TG}$  characteristics since  $R_{SD}$  is the major component of overall resistance limiting  $I_D$ . Conversely, when  $R_{SD} \ll R_{CHAN}$  ( $V_{BG}$  more negative), filling of acceptor-like states (located in S/D regions only) as  $V_{TG}$  increases does not create an  $I_D$ - $V_{TG}$  kink since  $R_{SD}$  is not the major component of resistance limiting  $I_D$ .

It is noted that the fact that the modeled  $I_D$ - $V_{TG}$  characteristics (Fig. 7) match to experimental  $I_D$ - $V_{TG}$  characteristics (Fig. 2) justifies the use of acceptor-like interface states in the model. For completeness, Fig. 8 shows the  $D_{it,u}$  and  $D_{it,g}$ -energy distribution which results in a good match between the modeled and experimental  $I_D$ - $V_{TG}$  characteristics. The value of  $D_{it,u}$  is consistent with the experimentally extracted uniform component of interface state density associated with the gate-dielectric / channel interface in MoS<sub>2</sub> devices [21], [22].

Based on the understanding derived from the model results in this section, it is expected that process optimization including pre-layer placement surface cleaning or post-layer

placement annealing at steps associated with the metal / MoS<sub>2</sub> interface could eliminate this  $I_D$ - $V_{TG}$  kink in all subsequently fabricated devices; however, such optimization remains to be investigated.

#### IV. CONCLUSION

In summary, a phenomenological model is developed which explains particular gate-bias-dependent kinking in  $I_D$ - $V_{TG}$  characteristics of MoS<sub>2</sub> DGFETs, with an  $I_D$ - $V_{TG}$  kink observed for small negative  $V_{BG}$  but not for large negative  $V_{BG}$ . The model incorporates a Gaussian distribution of acceptor-like interface states in S/D regions, as can arise from an imperfect metal-semiconductor interface. When  $R_{SD} \geq R_{CHAN}$  ( $V_{BG}$  less negative), filling of these acceptor-like states as  $V_{TG}$  increases creates a kink in  $I_D$ - $V_{TG}$  characteristics since  $R_{SD}$  is a major component of overall resistance limiting  $I_D$ . Conversely, when  $R_{SD} \ll R_{CHAN}$  ( $V_{BG}$  more negative), filling of these acceptor-like states as  $V_{TG}$  increases does not create an  $I_D$ - $V_{TG}$  kink since  $R_{SD}$  is not the major component of resistance limiting  $I_D$ . The model thus highlights 1) metal-semiconductor interface states need be accounted for when modeling MoS<sub>2</sub> FETs, and 2) the importance of forming metal-semiconductor interfaces with low interface state density (e.g., by optimization of cleaning or annealing steps associated with the formation of this specific interface) to avoid I-V kinks which are detrimental for analog applications.

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