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The Impact of LCE and PAMDLE Regarding Different CMOS ICs Nodes and High Temperatures

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ABSTRACT This paper describes the influence of Longitudinal Corner Effect (LCE effect) and PArallel Connection of Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) with Different Channel Lengths Effect (PAMDLE effect) of Diamond (hexagonal gate shape) MOSFET in different Complementary Metal-Oxide-Semiconductor (CMOS) Integrated Circuits (ICs) technologies (180nm-Bulk and 1μm-Silicon-On-Insulator, SOI) and in a wide range of high-temperatures (from 300K to 573K). The results have shown (average gains of Diamond MOSFET in relation to standard MOSFET: 60% for saturation drain current, 51% for transconductance, 10% for transconductance-over-drain current ratio etc.) that LCE and PAMDLE effects tend to be similar for CMOS ICs technological nodes used and the different high temperatures. Therefore, we can conclude, for the first time, that LCE and PAMDLE effects are kept active in different CMOS ICs technological nodes and when the Diamond MOSFET is exposed at high temperatures.

INDEX TERMS Diamond layout style for MOSFET, High temperature, LCE, PAMDLE.

I. INTRODUCTION

Many researches aim at enhancing the electrical performance of the Metal-Oxide-Semiconductor (MOS) Field Effect Transistor (MOSFET) using new semiconductor materials, manufacturing processes or device structures around the conventional temperature (T) range of, e.g., −25°C to 65-85°C [1]–[7]. Other techniques are based on the simple change of the gate geometry (known as *pn* junctions engineering among the source/channel/drain regions or simply gate layout changing) of MOSFETs [8]. A layout technique has been proposed using non-standard (non-rectangular) gate layout styles for MOSFETs, to boost their electrical performances. This is possible thanks to two intrinsic effects to these structures, called Longitudinal Corner Effect (LCE) and PArallel Connection of MOSFETs with Different Channel Lengths Effect (PAMDLE) [8]. The LCE is responsible for boosting their resultant longitudinal electric fields (RLEF) for specific bias conditions and PAMDLE is able to reduce the effective channel lengths (L_{eff}), in comparison to the standard (rectangular gate shape) MOSFET counterparts, considering that both present the same gate area (A_G) and channel width (W) [8].

The so-called Diamond MOSFET (DM) layout style was first proposed using a hexagonal gate shape [8], [9]. Previous studies have reported remarkable gains in the current-voltage characteristics of DM in relation to Rectangular (rectangular gate layout style – standard MOSFET) MOSFET (RM), from room to high temperature, in SOI technology thanks to LCE and PAMDLE [10], [11]. Besides, a recent study with another layout style for MOSFETs (Ellipsoidal) proved the improvements that this layout technique brings [12].

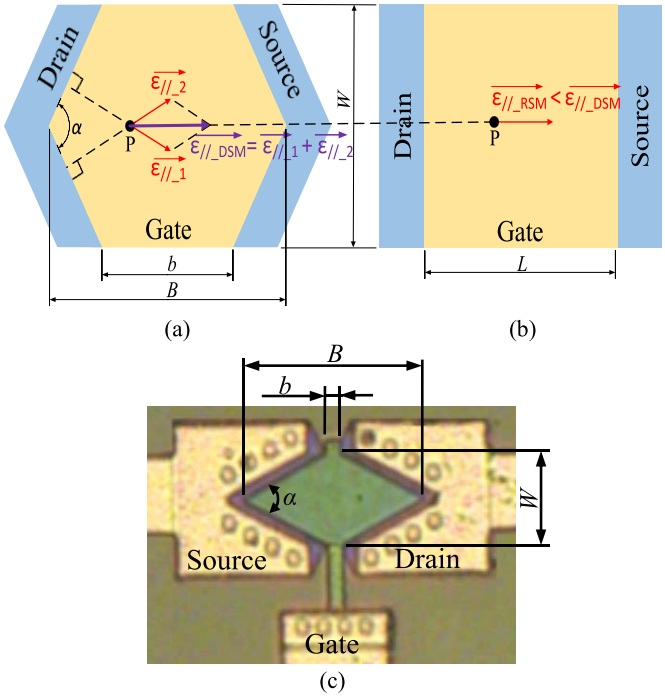

FIGURE 1. Schematic layouts of a DSM (a) and its RSM counterpart (b), illustrating their LEF components ($\overrightarrow{\varepsilon_{//1}}$ and $\overrightarrow{\varepsilon_{//2}}$), with same A_G, W and bias conditions. Besides, in (c) is illustrated a photograph of a Diamond SOI MOSFET manufactured ($\alpha = 90°$).

In this context, this manuscript extends the experimental comparative study of DM and RM to 180nm-Bulk CMOS ICs technology node (same gate area and channel width), for analog applications, notably high-gain amplifiers in a vast range of temperatures (from 300K to 573K). In addition, these results are compared to those obtained and published with similar devices implemented with 1μm Full-Depleted (FD) SOI CMOS technology [Diamond SOI MOSFET, DSM, and Rectangular SOI MOSFET, RSM (same gate area and channel width)] [10], [11], in order to understand the influence of LCE and PAMDLE in two different CMOS ICs technology nodes, i.e., if the gains in electrical performance from Diamond Layout Style (DLS) for MOSFET in relation to Rectangular MOSFET are similar in different CMOS ICs technological nodes, regarding when these devices were exposed at high temperatures.

II. DEVICE'S CHARACTERISTICS AND STRUCTURES

Two examples of simplified SOI MOSFETs layouts (Fig. 1a: DSM and Fig. 1b: RSM) with their dimensional characteristics and their respective LEF components and also an example of a photography of a Diamond SOI MOSFET (α angle equal to 90°) manufactured (Fig. 1c) are illustrated in Fig. 1. Diamond layout style for MOSFET uses the corner effect in the longitudinal direction of the channel region (LCE effect) to enhance RLEF ($\overrightarrow{\varepsilon_{//}}$) in a MOSFET [8], as illustrated in Fig. 1a for DSM.

In Fig. 1, B and b are the largest and smallest channel lengths, respectively, α is the angle between the metallurgical pn junctions of the source/silicon-film (channel region) and the silicon-film/drain regions and L is RSM channel length.

Considering the point P (an arbitrary point in the channel regions of both devices in Fig. 1) in the channel regions of both devices, RLEF of DSM (Fig. 1a) due to the drain bias (V_{DS}) is ($\overrightarrow{\varepsilon_{//\_DSM}}$), which is given by the vector sum of two longitudinal electric field (LEF) components ($\overrightarrow{\varepsilon_{//1}} + \overrightarrow{\varepsilon_{//2}}$). Regarding the same point in RSM counterpart (Fig. 1b), the resultant LEF ($\overrightarrow{\varepsilon_{//\_RSM}}$) is composed by only one LEF component. Therefore, the resultant LEF along the channel length of DSM is higher than the one found in its RSM counterpart, thanks to LCE. The presence of LCE increases the drift velocity of mobile charge carriers ($\overrightarrow{v_{//}}$) in the channel region of DSM and, consequently, its drain current (I_{DS}) is higher than the one measured in RSM counterpart [8]. Besides, due to PAMDLE effect, DSM I_{DS} tends to further flow in the edges of the channel region, because if we consider DSM as a parallel addition of infinites MOSFETs, these edges there are MOSFETs with channel lengths smaller than those in the center of the device. Thus, PAMDLE is able to reduce the L of a DSM [$L_{eff} = (B - b)/[\ln(B/b)]$] in comparison to the one observed in RSM counterpart [$L = (b + B)/2$], regarding that they present the same A_G and W [8]. Therefore, as I_{DS} is inversely proportional to L, DSM I_{DS} tends to be higher than that of RSM counterpart [13]. These two effects (LCE and PAMDLE) produced by the Diamond layout style act jointly and therefore, are capable to boost the electrical performance of MOSFETs [8].

A first-order analytical model for DSM I_{DS} (I_{DS_DSM}) as a function of I_{DS} of RSM counterpart (I_{DS_RSM}) is given in (1) [8]:

$$I_{DS\_DSM} = G_{LCE}.G_{PAMDLE}.I_{DS\_RSM} \tag{1}$$

where G_{LCE} is equal to $\sqrt{2(1+\cos\alpha)}$ for $0° < \alpha \leq 90°$ and $\sqrt{2+\cos\alpha}$ for $90° \leq \alpha < 180°$, respectively, which it is related to LCE effect, and G_{PAMDLE} is equal to L/L_{eff} that represents the gain provided by PAMDLE effect [8], [14]. This simple analytical model of I_{DS_DSM} have been validated through experimental data and presented a maximum error smaller than 10%, regarding 100 measurements [8]. Besides, we would like to point out that all the features described above for DLS for MOSFET implemented in SOI technology apply also to Bulk technology [8].

The dimensional characteristics of fabricated of n-type bulk and SOI MOSFETs implemented with DLS and its Rectangular counterparts used in this study are described in Table 1.

Based on Table 1, it is possible to observe that DM and DSM L_{eff} are 23% and 20%, respectively, smaller than the channel length of its Rectangular MOSFETs counterparts, thanks to PAMDLE effect. Consequently, DM and DSM I_{DS} are boosted by G_{PAMDLE} and it tends to be higher than the one observed in RM and RSM counterpart, respectively.

TABLE 1. Dimensional characteristics of devices.

	L [μm]	B [μm]	b [μm]	α [°]	L_{eff} [μm]	W/L	W [μm]	A_G [μm²]	G_{LCE}	G_{PAMDLE}
DM	0.54	0.90	0.18	90	0.45	1.50	0.81	0.460	$\sqrt{2}$	1.2
RM	0.56	-	-	-	0.56	1.44			-	-
DSM	8.0	14.0	2.0	90	6.17	1.5	12.0	96.0	$\sqrt{2}$	5.33
RSM		-	-	-	8.0				-	-

TABLE 2. Threshold voltages for different temperatures of devices used in this study.

	Temperature [K]						
	300	***323***	***373***	***423***	***473***	***523***	***573***
DM V_{TH} [V]	0.50	0.48	0.44	0.40	0.35	0.30	0.26
RM V_{TH} [V]	0.49	0.46	0.42	0.38	0.34	0.29	0.25
DSM V_{TH} [V]	0.49	0.44	0.41	0.40	0.37	0.34	0.33
RSM V_{TH} [V]	0.48	0.45	0.42	0.39	0.36	0.35	0.32

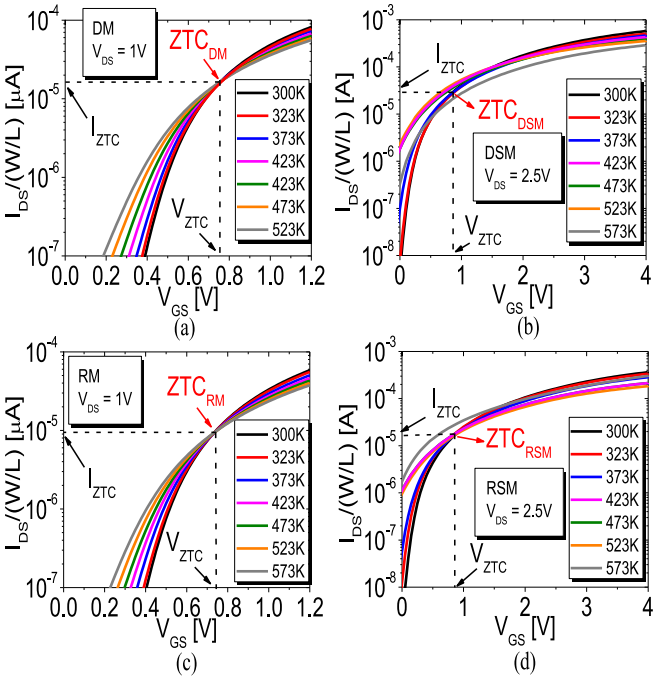

FIGURE 2. Experimental curves of $I_{DS}/(W/L)$ as a function of V_{GS} for different temperatures, highlighting ZTC point for DM (a), DSM (b), RM (c) and RSM (d).

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

The methodology used in this work was to evaluate the analog performance of MOSFETs implemented with the Diamond layout style in Bulk and SOI technologies in relation to the results presented by their respective Rectangular MOSFETs counterparts, through the analysis of electrical device parameters such as: threshold voltage (V_{TH}), zero-temperature coefficient, saturation drain current (I_{DS_SAT}), leakage current (I_{LEAK}), transconductance (gm), output conductance (g_D), early voltage ($V_{EA} = I_{DS}/g_D$), transconductance-over-drain current ratio (gm/I_{DS}) and intrinsic gain [$A_V = gm/g_D = V_{EA} \cdot (gm/I_{DS})$].

The key figures of merit of a MOSFET given in the literature for the design of analog integrated circuits are I_{DS_SAT}, gm and g_D in saturation regime. Besides, together with these figures of merit, gm/I_{DS} and V_{EA} are the figures of merit of technology indicating the efficiency of the devices to convert DC power into AC frequency and voltage gain performance [15].

The measured threshold voltages of the all devices are presented in Table 2, which were obtained through second-derivative method for V_{DS} equal to 50mV [16] and different high temperatures. These results have shown identical reduction with the temperature in all devices, according to the dependence with the Fermi potential (Φ_F), as expected [13], [17] and the values of V_{TH} presented by DLS for MOSFETs are similar to those found in Rectangular MOSFETs style in all temperatures studied, regarding that the comparative between both devices are performed on the same CMOS ICs technological node.

The transfer characteristics of the devices are presented in Fig. 2, in the saturation region and normalized by the aspect ratio (W/L), highlighting the zero-temperature coefficient.

The zero-temperature coefficient (or ZTC point) condition of MOSFET, by definition, is the voltage bias between the gate and source (V_{GS}) which ensures that I_{DS} does not vary with the temperature [18], [19]. Remember that I_{DS} increases when mobility of the mobile charge carriers increases and when V_{TH} decreases, and that mobility and V_{TH} both decrease as the temperature increases [13], [17], [20]. Thus, it can be proved that both effects can cancel each other at a certain bias voltage. Thus, ZTC condition derives from the mutual cancelation of the effects of the temperature in the mobility of the mobile charge carriers in MOSFET's channel and V_{TH}, at a particular V_{GS} bias [18], [19]. This condition defines a bias point of MOSFET defined by a V_{GS} of ZTC (V_{ZTC}) and an I_{DS} of ZTC (I_{ZTC}). In this bias condition, MOSFETs I_{DS} present a low sensitivity to the temperature variations [18], [19].

Analyzing Fig. 2, ZTC V_{GS} (V_{ZTC}) for DM and RM are both approximately equal to 0.75V, for a V_{DS} equal to 1V. When we analyze the SOI devices, Fig. 2 illustrates that both devices did not present a V_{ZTC} value well defined, because up to 473K, ZTC points are quite well defined and only above 523K, they are a bit off. The reason could be that at 523K, the SOI devices turn from FD to slightly partially depleted (PD), because gm/I_{DS} ratios between Bulk and SOI devices are similar, as will be observed when we will describe the behavior of gm/I_{DS} of devices at high temperatures [21], [22]. Therefore, we defined ZTC point up to a temperature of 473K for both devices, resulting in V_{ZTC} approximately equal of 0.85V for DSM and RSM counterpart. The simple fact that V_{ZTC} are the same between

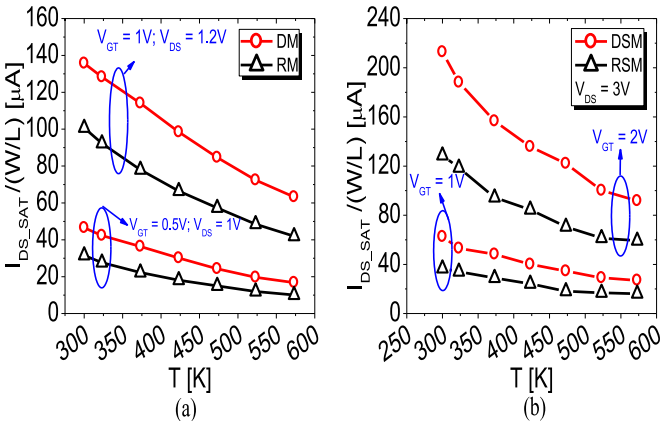

FIGURE 3. Experimental curves of $I_{DS\_SAT}/(W/L)$ as a function of the temperature for Diamond and Rectangular layout styles for MOSFETs implemented in Bulk (a) and SOI (b) technologies, respectively.

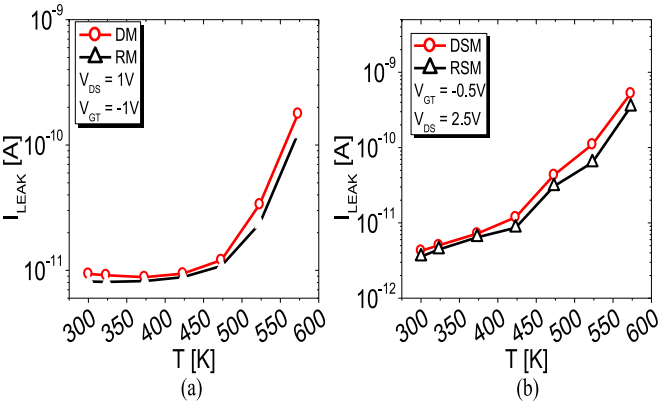

FIGURE 4. Experimental curves of I_{LEAK} as a function of temperature for Diamond and Rectangular layout styles for MOSFETs implemented in Bulk (a) and SOI (b) technologies, respectively.

Diamond layout style and rectangular layout style, according to each manufacturing technology, confirming the identical trends of V_{TH} (Table 2) and the mobility of the mobile charge carriers with the temperature [13], [17], [20]. However, *ZTC* current, I_{ZTC}, of the devices are different. The I_{ZTC} for RM is equal to 9.4μA, while it is equal to 16.3μA for DM, which corresponds to 73% of gain. In SOI technology, DSM I_{ZTC} is equal to 29μA, which represents a gain of 81% in relation than the one found in its RSM counterpart (16μA). These gains presented by DLS for MOSFET, in both technologies, are thanks to LCE and PAMDLE [G_{LCE} and G_{PAMDLE} in (1)], which are able to boost DM and DSM I_{DS}, throughout the large temperature range that we considered.

Furthermore, based on Fig. 2, we observe that below *ZTC* bias point, I_{DS} is higher for the high temperatures, mainly due to reduction of V_{TH}. Above this value, I_{DS} becomes smaller at high temperatures, mainly due to the reduction of the mobility of the mobile charge carriers in the channel and increase of the series drain/source resistances [18], [19].

The experimental curves of I_{DS_SAT} normalized by the aspect ratio [$I_{DS\_SAT}/(W/L)$] as a function of the temperature are presented in Figs. 3a and 3b, for the Diamond and Rectangular layout style for MOSFET in Bulk and SOI technologies, respectively. The devices were measured for overdrive gate voltages ($V_{GT} = V_{GS} - V_{TH}$) above and below of the V_{ZTC} value of each manufacturing technology (for SOI devices only to $V_{GT} > V_{ZTC}$) and V_{DS} values above V_{GT}, in order to ensure that the devices are in the saturation region.

Fig. 3 shows that $I_{DS\_SAT}/(W/L)$ reduces with temperature as the temperature increases, due to the degradation of the mobility of the mobile charge carriers with increasing temperature, as expected [13], [17], [20]. However, DM and DSM $I_{DS\_SAT}/(W/L)$ always remain higher at all temperatures studied than those observed in RM and RSM counterparts. As example, DM and DSM present minimum gain of 46% and 54% in relation to RM and RSM counterparts, respectively, and the percentage of gain is similar in the two manufacturing technologies.

In OFF conditions, MOSFET leakage current (I_{LEAK}) is proportional to the area of reverse-biased drain and source-to-substrate *pn* junctions, and is given by (2) [23]:

$$I_{LEAK} = q.A\sqrt{\frac{D_n}{\tau_n}}.\frac{n_i^2}{N_A} + q.A.\frac{n_i.W_d}{\tau_e} \quad (2)$$

where q is the electron charge, A the area of reverse-biased drain and source-to-substrate *pn* junctions, D_n the electrons diffusion coefficient, τ_n the electron lifetime in p-type semiconductor, n_i the intrinsic charge carriers concentration, N_A the doping concentration in p-type semiconductor (channel region), W_d the width of the depleted junction region and τ_e is the effective lifetime related to the thermal generation process (Shockley–Read–Hall generation) in the depletion regions of reverse- biased pn junctions between the drain/body and body/source regions [23].

The I_{LEAK} dependence with the temperature is mostly related to n_i, which is highly dependent on temperature [13], [17]. Considering temperatures below of 423K, I_{LEAK} follows $n_i(T)$, where the generation component is the dominant mechanism, corresponding to the second term in (2). However, I_{LEAK} varies as a function of $n_i^2(T)$ for temperatures above 423K, whose dominant mechanism is the carriers' diffusion and is described by the first term in (2) [23].

Figs. 4a and 4b illustrate the experimental curves of the I_{LEAK} as a function of the temperature for Bulk and SOI MOSFETs, respectively.

The DLS MOSFETs structure always presented I_{LEAK} values slightly higher than those found in the rectangular one in both CMOS technologies. For instance, when the temperatures are equal to 300K, 423K and 523K, DM I_{LEAK} is 24%, 30% and 51% and DSM I_{LEAK} is 20%, 37% and 50%, respectively, higher than their respective MOSFETs with rectangular layout style counterpart. This is related to the areas of the reverse-biased drain and source-to-substrate

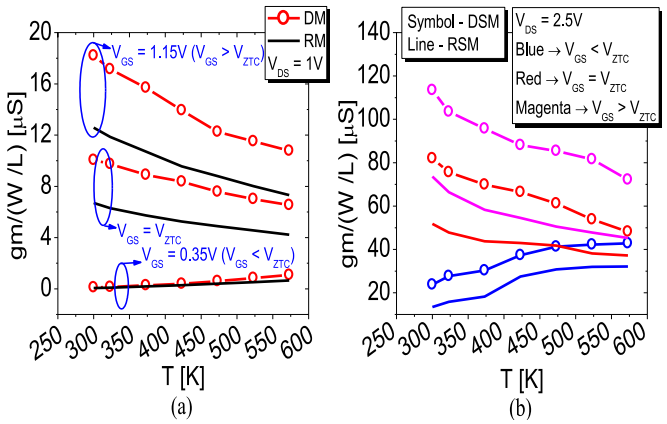

FIGURE 5. Experimental curves of $gm/(W/L)$ as a function of temperature for Diamond and Rectangular layout styles for MOSFETs implemented in Bulk (a) and SOI (b) technologies, respectively.

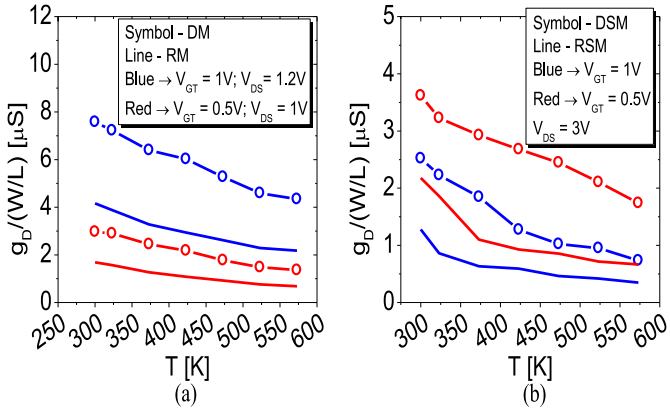

FIGURE 6. Experimental curves of $g_D/(W/L)$ as a function of temperature for Diamond and Rectangular layout styles for MOSFETs implemented in Bulk (a) and SOI (b) technologies, respectively.

pn junctions of DM ($0.1\mu m^2$) and DSM ($1.7\mu m^2$) that are 25% and 42% larger than the one of RM ($0.08\mu m^2$) and RSM ($1.2\mu m^2$) counterparts, respectively, and consequently, it increases their I_{LEAK} Besides, LCE effect also contributes to increasing I_{LEAK} in the Diamond structure, because this effect increases the thermal generation process of minority carriers in the depletion region (Shockley–Read–Hall generation). However, in any case, I_{LEAK} remains much smaller than I_{DS_SAT} in both devices and hence cannot perturbate the bias current of analog ICs.

For the analog figures of merit of relevance for amplifiers [15], [22], the experimental curves of $gm/(W/L)$, output conductance $[g_D/(W/L)]$ in saturation region, gm/I_{DS} ratio and intrinsic voltage gain (A_V) as a function of temperature for all devices are described below.

Based on Figs. 5a and 5b, we observed that DM and DSM $gm/(W/L)$ at all temperatures are always higher than those found in RM and RSM counterparts. To exemplify, considering $V_{GS} = V_{ZTC}$ and the temperatures of 300K, 473K and 573K, the values of DM $gm/(W/L)$ represent gains of 49%, 59% and 54%, respectively, in relation to those found in RM counterpart and DSM $gm/(W/L)$ is 58%, 55% and 49% higher than to those found in RSM counterpart at these temperatures. These gains are due the presence of LCE and PAMDLE in DLS MOSFET structure [8]. Consequently, the normalized amplifier transition frequencies f_T (frequency which corresponds to the transit frequency of the current gain when it is equal to 1), given by $gm/(2\pi C_L)$, where C_L is a given load capacitance, fixed at 1pF for this work, are hence always higher in DLS MOSFETs structure than those presented by the rectangular one for all temperatures.

Furthermore, observing the experimental curves of $gm/(W/L)$ from Fig. 5a, $gm/(W/L)$ reduces when the temperature increases in all devices when $V_{GS} \geq V_{ZTC}$, due to the reduction of the mobility of mobile charge carriers in the channel regions and the increase of the series resistances (composed by drain, channel and source resistance) of MOSFETs, as usual [13], [17], [20]. However, when $V_{GS} < V_{ZTC}$ the values of $gm/(W/L)$ increases as temperature also increases. This occurs because the reduction in V_{TH} with increasing temperature exerts a greater influence on I_{DS}, which increases its value, than the degradation of mobility at high temperatures when V_{GS} is smaller than V_{ZTC} [13].

Fig. 6 presents the experimental curves of $g_D/(W/L)$ ($g_D = \partial I_{DS}/\partial V_{DS}$) as a function of temperature for MOSFETs implemented with Bulk (Fig. 6a) and SOI (Fig. 6b) technologies, regarding that all devices are in saturation region ($V_{DS} > V_{GT}$).

Based on Fig. 6, we notice that DM and DSM $g_D/(W/L)$ present same trend in these high temperature conditions and $g_D/(W/L)$ reduces in all devices as the temperature increases due to degradation of mobility of the mobile charge carriers at high temperatures [13], [17], [20]. The increase of the temperature at which the MOSFET is exposed becomes a benefit for g_D of the devices, because as the MOSFET output conductance reduces, better its electrical behavior will be in saturation regime (e.g., highest intrinsic gain). In addition, as the temperature increases, the impact ionization effect decreases also, resulting in improved g_D [13], [21].

The g_D is linked to I_{DS}/V_{EA}, where both parameters influence the behavior of g_D at high temperatures [13]. As a result, DM $g_D/(W/L)$, for all studied temperatures, are always higher (82%, 104% and 94% for temperature equal to 300K, 473K and 573K, respectively, for V_{GT} equal to 1V) than those of RM counterpart, due to mainly LCE. This effect has the capability to influence impact ionization effect on DM more than the effect of the elevation of I_{DS_SAT} that LCE itself provides. Consequently, DM V_{EA} modulus ($|V_{EA}|$) is smaller than found one in RM counterpart in all temperatures considered in this study, as it is possible to observe through Fig. 7a, regarding I_{DS} and g_D are in saturation regime. With these results, DM g_D tends to be greater than those found in RM counterpart. DSM presents the same behavior described above for DM $g_D/(W/L)$ and $|V_{EA}|$, as Fig. 6b and Fig. 7b show, respectively.

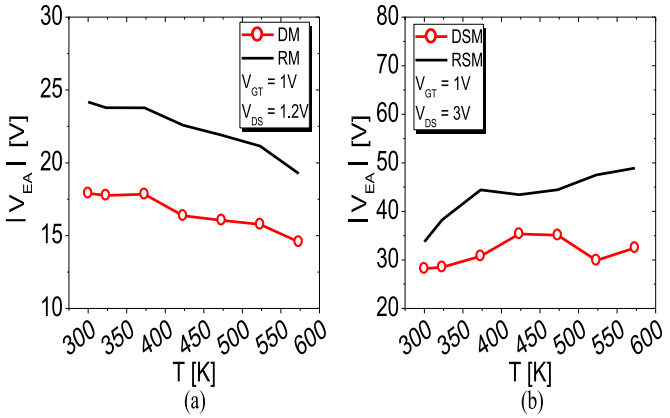

FIGURE 7. Experimental curves of $|V_{EA}|$ as a function of temperature for Diamond and Rectangular layout styles for MOSFETs implemented in Bulk (a) and SOI (b) technologies, respectively.

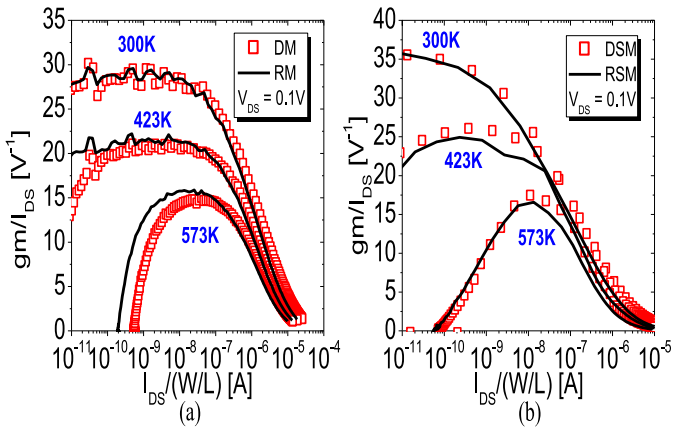

FIGURE 8. Measured gm/I_{DS} as a function of normalized drain current by the aspect ratio, considering three different temperatures (300K, 423K and 573K) for Diamond and Rectangular layout styles for MOSFETs, implemented in Bulk (a) and SOI (b) technologies, respectively.

Besides, analyzing Fig. 7b is possible to observe that $|V_{EA}|$ is increasing in the SOI MOSFETs as temperature increase, due to the reduction of the impact ionization effect that FD SOI MOSFET presents in relation to the Bulk MOSFET [23]. The reduction of this effect results in lower values of g_D in FD SOI MOSFET, as shown in Fig. 6, which has a greater influence on the $|V_{EA}|$ results than I_{DS_SAT} as the temperature increases. On the other hand, I_{DS_SAT} caused a greater influence on the $|V_{EA}|$ results in Bulk MOSFETs, reducing $|V_{EA}|$ as the temperature increase, as Fig. 7a shows.

Fig. 8 presents gm/I_{DS} ratio of Bulk (Fig. 8a) and SOI (Fig. 8b) MOSFETs as a function of $I_{DS}/(W/L)$, considering three different temperatures (300K, 423K and 573K) and V_{DS} equal to 0.1V. The gm/I_{DS} as a function of $I_{DS}/(W/L)$ plot is a very convenient representation for comparing different devices thanks to its independence on V_{TH} and, to the first order, it does not depend on the channel length either [22], [24].

It is seen from Fig. 8, that DM and DSM gm/I_{DS} in weak inversion regime (as for low-frequency base-band applications) are similar to RM and RSM gm/I_{DS}, suggesting that both have the same subthreshold slope, but in the moderate and strong (as for high-frequency applications) inversion regimes, DM and DSM gm/I_{DS} are, on average, 11% and 9% higher than those found in RM and RSM counterparts, respectively, thanks LCE and PAMDLE. Another interesting observation is that, below 573K the SOI devices are FD and gm/I_{DS} is higher than in Bulk devices, but in 573K, similar gm/I_{DS} between the technologies, i.e., the SOI devices probably became PD-SOI. Furthermore, as the temperature increases there is an expected degradation of gm/I_{DS} in all devices, because in weak inversion the maximum value of gm/I_{DS} is inversely proportional to temperature and in strong inversion the key temperature-dependent parameter for gm/I_{DS} is the mobility of the mobile charge carriers [21].

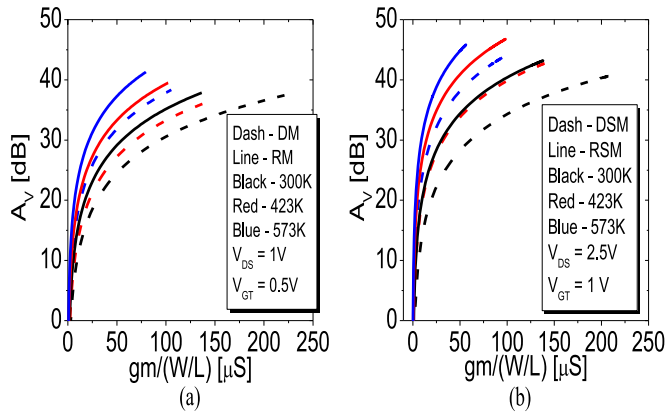

FIGURE 9. A_V versus gm normalized drain current in three different temperatures for Diamond and Rectangular layout styles for MOSFETs, implemented in Bulk (a) and SOI (b) technologies, respectively.

Finally, Fig. 9 plots A_V as a function of $gm/(W/L)$ (as an analog benchmark proposed in [15]), considering three different temperatures (300K, 423K and 573K) of Bulk (Fig. 9a) and SOI (Fig. 9b) MOSFETs, to compare the analog performance across all regions of inversion (saturation region).

Based on Fig. 9 and considering the same A_V for both CMOS technologies in different temperatures, we can observe that the DLS for MOSFETs is capable of providing $gm/(W/L)$ about two times higher as compared to those measured with the rectangular MOSFETs counterparts. Consequently, DLS MOSFETs structure has tremendous benefit concerning high-gain amplifiers that can double the $f_T/(W/L)$ in relation to those found in RMs counterparts (better frequency response performance) at high temperatures environment.

Table 3 summarizes the gains of some electrical parameters and figures of merit have studied of the Diamond layout style for MOSFETs in relation to the rectangular one for two different CMOS technological nodes [180nm-Bulk and 1μm-Silicon-On-Insulator and the same α angle (90°)] and a huge range of high temperatures.

TABLE 3. Gains of the diamond layout style for MOSFETs in relation to the rectangular one for different CMOS technologies.

	Gains of the Diamond layout style for MOSFETs in relation to rectangular one					
Temperature	*300K*		*423K*		*573K*	
Technology	*SOI*	*BULK*	*SOI*	*BULK*	*SOI*	*BULK*
$I_{DS\_SAT}/(W/L)@V_{GT}=1V$	+67%	+57%	+64%	+50%	+66%	+54%
I_{LEAK}	-20%	-24%	-37%	-30%	-50%	-51%
$gm/(W/L)@V_{GS}>V_{ZTC}$	+50%	+46%	+58%	+45%	+57%	+48%
$g_D/(W/L)@V_{GT}=1V$	-96%	-82%	-115%	-104%	-108%	-94%
gm/I_{DS}@*moderate regime*	+12%	+9%	+12%	+10%	+15%	+13%

The +/- sign: better/worst performance of DLS MOSFETs structure in relation to the one of RM counterpart.in Bulk and SOI MOSFETs.

Based on the results of Table 3, we conclude that the influence of LCE and PAMDLE effects tend to be similar for the two CMOS ICs technological nodes used in this study (180nm-Bulk and 1μm-Silicon-On-Insulator) and the high temperatures. Because the differences between gains that DLS MOSFET structure promotes in relation to standard MOSFET in CMOS ICs technological nodes used do not exceed the value of 15%. Therefore, we conclude, for the first time, that the gains the Diamond layout style for MOSFETs provides in relation to the rectangular one is independent of CMOS technology used and the temperature that it is exposed.

IV. CONCLUSION

We have performed an experimental comparative study between the Diamond and Rectangular (standard) layout style in two different CMOS ICs technological nodes (180nm-Bulk and 1μm SOI), regarding a huge range of high temperatures (from 300K to 573K), in order to analyze the influence of LCE and PAMDLE in these conditions, i.e., if the gains in electrical performance from DLS for MOSFETs in relation to Rectangular MOSFET one remains similar when different CMOS technology nodes and high temperatures are considered. The main results have shown that the gains of $I_{DS\_SAT}/(W/L)$ of DM and DSM, on average, were of 69% and 63%, respectively, in relation to RM and RSM counterpart; DM and DSM $gm/(W/L)$ presented on average gain of 54%. All results confirm previous studies that DLS can be considered an alternative strategy to boost the electrical performance of MOSFET to be used in, e.g., high-gain analog amplifier. Our results demonstrate that at identical low-frequency gain and capacitive load, DM amplifiers could reach a transition frequency two times higher than RM counterpart ones Besides, we concluded that LCE and PAMDLE effects are kept active independently of these two CMOS technology nodes and for different temperatures (difference between gains smaller than 15%), i.e., the gains presented by DLS for MOSFETs in the main electrical parameters are preserved and similar in both CMOS ICs technological nodes.

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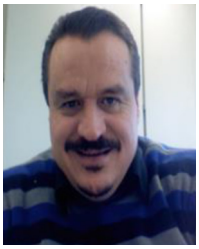

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