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Steep Switching Characteristics of L-Shaped Tunnel FET With Doping Engineering

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ABSTRACT In this work, a L-shaped tunnel FET (TFET), which has the dominant tunneling current in the normal direction to the gate, is introduced with the doping engineering and its electrical characteristics are analyzed using TCAD device simulations. The proposed L-shaped TFET has the pocket doping (p^+-doping for n-type operations) underlying the gate, which can suppress the corner tunneling generated near the source edge by the electric-field crowding. Thus, the on/off transition is significantly improved since the corner tunneling is the main cause of the degradation of the switching characteristics. To maximize the performance enhancement, the concentration of the pocket doping (N_{POC}) is optimized. As a result, the averaged subthreshold swing (SS_{AVE}) gets reduced from 60 to 26 mV/dec and the on-current (I_{ON}) becomes $\sim$ 2.0 times increased as compared to the conventional L-shaped TFETs. Moreover, it is confirmed that the pocket doping effectively suppresses the corner tunneling without the on-current reduction even in the extremely scaled gate length (L_G) device.

INDEX TERMS Band-to-band tunneling (BTBT), gate-normal tunnel FET (TFET), L-shaped TFET, corner tunneling, subthreshold swing (SS), hump phenomenon.

I. INTRODUCTION

For digital applications, the low power operation is one of the big concerns as Internet of Things (IoT) and wearable technology is quickly developing to improve our quality of life [1]–[3]. However, complementary MOS (CMOS) devices, which are utilized for microprocessor and static RAM (SRAM), have the fundamental limitation by their carrier injection mechanism (thermionic emission) and thereby subthreshold swing (*SS*) cannot be lower than 60 mV/dec at room temperature [4], [5]. Therefore, as a breakthrough, the steep switching devices such as tunnel FET (TFET) and negative capacitance FET (NCFET) have been widely studied [6]–[15]. Especially, the TFETs with tunneling in the normal direction to a gate by using the epi-channel region (gate-normal TFET) has been widely researched to be competitive with conventional CMOS performance [16]–[20]. It can have the sub-60 mV/dec steeper *SS* by using inter-band tunneling as a carrier injection mechanism as well as the larger tunneling current by extending the tunneling area compared to conventional TFETs. In spite of these advantages, it is hard to obtain the abrupt on/off transition in the gate-normal TFETs because the occurrence of the corner tunneling at the edge of the source region underneath the gate degrades *SS* and even causes the drain current hump [21].

The L-shaped TFET, which is based on the mesa structure with the epi-channel, has been also studied as one of the gate-normal TFETs [22], [23]. Recently, the stacked gate L-shaped TFET has been reported to suppress the electric-field crowding at the source corner by using additional high workfunction (WF) metal gate, which leads to the steep switching characteristics [24]. However, integrating two metals with different WFs is quite complicated in terms of process fabrications.

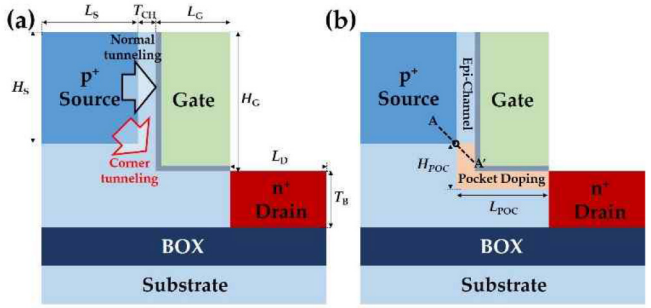

FIGURE 1. Schematic images of (a) the conventional n-type L-shaped tunnel FET (TFET) and (b) the proposed TFET. Both the L-shaped TFETs have the same device dimensions except for the pocket doping underlying the gate region.

In this study, the L-shaped TFET with the doping engineering is proposed to achieve steep switching characteristics. The proposed device can be easily implemented by introducing the pocket doping under the gate. Therefore, the effects of the pocket doping are rigorously investigated by using technology computer-aided design (TCAD) simulations and the various device parameters of the proposed device are optimized to maximize the device performances. Then, the process integration flow of the proposed L-shaped TFET is demonstrated in terms of the fabrication feasibility.

II. DEVICE PARAMETERS AND MODELS

Figs. 1(a) and (b) illustrate the n-type L-shaped TFETs for the conventional and the proposed structures used in this study. The proposed L-shaped TFET has the pocket doping region (p^+- doping for n-type operations) and the p^- epi-channel region underlying the gate, whereas the conventional one has only the p^- epi-channel region. To investigate the electrical characteristics of the proposed device, 20 nm gate length (L_G), 1.0 nm equivalent oxide thickness (EOT), and 4 nm epi-channel thickness (T_{CH}) are adapted. 4 nm T_{CH} is selected because the L-shaped TFET can have the maximum current drivability with $T_{CH} = 4$ nm as reported in the literature [22]. Additionally, 80 nm source height (H_S) and 10 nm body thickness (T_B) are applied. For the pocket doping, the length and height of the doping region are defined as $T_{CH} + 16$ nm and $T_{CH} + L_G$, respectively. To reduce the ambipolar current, the drain doping is set to 1×10^{18} cm^{-3} which may cause high contact resistances. Hence, the contact plug implantation is required before the contact formation. Other detailed parameters used in the TCAD simulations are listed in Table 1. All the device evaluations are performed by commercial TCAD tool (Synopsys Sentaurus^{TM}).

For accuracy analysis on tunneling current, the dynamic nonlocal band-to-band tunneling (BTBT) model (Kane's model) is used as follows [25].

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right) \quad (1)$$

which are $F_0 = 1$ V/m and $P = 2.5$ for indirect BTBT, $A_{Si} = 1.64 \times 10^{15}$ cm^{-3}·s^{-1} and $B_{Si} = 23.8 \times 10^6$ V·cm^{-1}

TABLE 1. Physical parameters of proposed device.

Symbol	Quantity	Value
L_G	Gate Length	20 nm
EOT	Equivalent Oxide Thickness	1.0 nm
L_S	Source Length	30 nm
L_D	Drain Length	30 nm
H_S	Source Height	80 nm
T_B	Body Thickness	10 nm
T_{CH}	Epi-Channel Thickness	4 nm
H_G	Gate Height	96 nm
H_{POC}	Pocket Height	T_{CH} + 16nm
L_{POC}	Pocket Length	$T_{CH} + L_G$
N_B	Body Doping	5×10^{17} cm^{-3}
N_S	Source Doping	1×10^{20} cm^{-3}
N_D	Drain Doping	1×10^{18} cm^{-3}
N_{POC}	Pocket Doping	$(0.05\text{-}2.5)\times10^{19}$ cm^{-3}
WF	Gate Workfunction	4.0 eV

TABLE 2. Slotboom and SRH recombination model parameters.

Model	Parameters	Unit	Value
Slotboom	*E*ref	cm^{-3}	1.3×10^{17}
	*N*ref	eV	0.00692
SRH Recombination	*tau*min (e, h)	s	0, 0
	*tau*max (e, h)	s	1.0×10^{-5}, 3.0×10^{-6}
	*N*ref (e, h)	cm^{-3}	10^{16}, 10^{16}
	γ (e, h)	-	1, 1
	*T*α (e, h)	-	-1.5, -1.5
	*T*coeff	-	2.55, 2.55
	*E*trap (e, h)	eV	0.0, 0.0

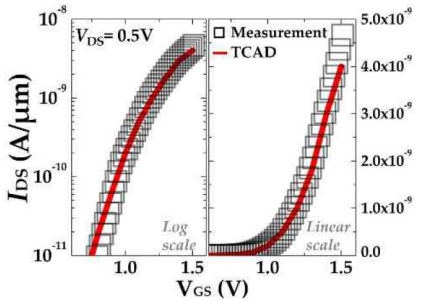

FIGURE 2. Transfer characteristics of the experimental L-shaped TFET and TCAD simulation results. (log/linear scales).

referred from [26]. Furthermore, Slotboom model is applied to consider the impact of doping concentrations on energy bandgap narrowing in the source/drain (S/D) regions. Also, Fermi statistics and Shockley-Read-Hall recombination models are used. The key model parameters are listed in Table 2. However, gate leakage current is ignored because this study is mainly focused on the effects of the pocket doping.

III. RESULTS AND DISCUSSION

A. POCKET DOPING OPTIMIZATION

First, the experimental transfer characteristics of the previously reported L-shaped TFET are reproduced with the BTBT model for the simulation accuracy as shown in Fig. 2 [23].

Fig. 3(a) shows the transfer characteristics of the conventional L-shaped TFET at $V_{DS} = 0.75$ V. It has the

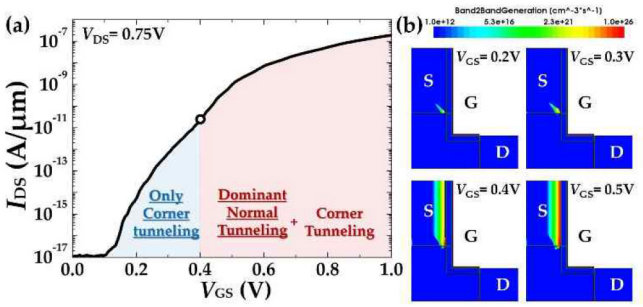

FIGURE 3. (a) Transfer characteristics of the conventional L-shaped TFET at V_{DS} = 0.75 V. It is separated into two regions: (1) corner tunneling; and (2) corner + normal tunneling regions. (b) 2D contour band-to-band tunneling (BTBT) rates at V_{GS} = 0.2 V, 0.3 V, 0.4 V, and 0.5 V. Until V_{GS} = 0.4 V, it is observed that the dominant current component consists of the corner tunneling, leading to poor switching characteristics.

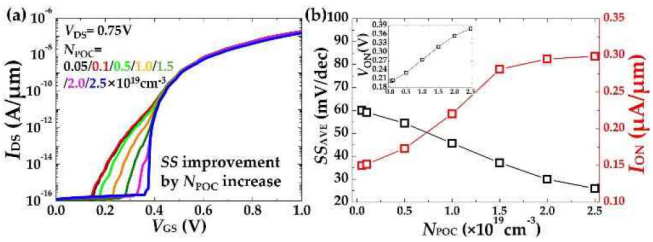

FIGURE 4. (a) Transfer characteristics of the proposed L-shaped TFET at V_{DS} = 0.75 V depending on the doping concentrations of the pocket doping region (N_{POC}). (b) Averaged subthreshold swing (SS_{AVE}) and on-current (I_{ON}) extracted at V_{GS} = 0.75V + V_{ON}.

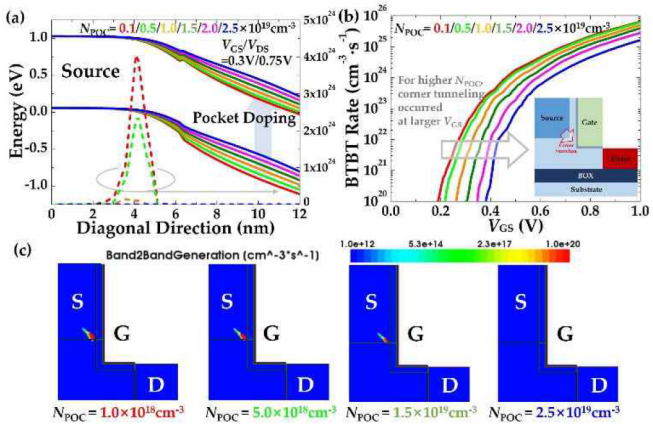

FIGURE 5. (a) Energy band diagrams along diagonal direction near source-edge region (A-A') and BTBT rates with various N_{POC}s at V_{DS}/V_{GS} = 0.75 V/0.3 V. (b) Corner BTBT rates with respect to V_{GS} with increasing N_{POC}s. (c) 2D BTBT rate contours with N_{POC} = 0.1, 0.5, 1.5, and 2.5 × 10^19 cm^-3 at V_{GS} = 0.3 V.

averaged SS (SS_{AVE}) of 60 mV/dec and the on-current (I_{ON}) of 0.15 uA/um, respectively. Here, SS_{AVE} is calculated by averaging SS in the drain current (I_{DS}) range from 1×10^{-14} to 1×10^{-9} A/um. A turn-on voltage (V_{ON}) is designated as V_{GS} at $I_{DS} = 1 \times 10^{-14}$ A/um and an I_{ON} is extracted at $V_{GS} = 0.75$ V + V_{ON} as an overdrive voltage. It is found that the I_{DS} hump occurs at $V_{GS} =\sim 0.4$ V because there exist two tunneling current paths: (1) tunneling at the corner edge of the source region (corner tunneling); and (2) tunneling in the normal direction to the vertical gate at the source overlap region (normal tunneling). To confirm the generation of the two different tunneling currents, the 2D BTBT rate contours are plotted from $V_{GS} = 0.2$ V to 0.5 V as shown in Fig. 3(b). It is clearly seen that the corner tunneling is generated first by the electric-field crowding at the corner edge of the source region and then the normal tunneling occurs when a sufficient V_{GS} (> 0.4 V) is applied. This V_{GS} difference between the generations of the two different tunneling currents induces the I_{DS} hump, which results in poor switching characteristics.

To mitigate the corner tunneling induced by the electric-field crowding, the pocket doping region (R_{POC}) is introduced under the gate region [Fig. 1(b)] since it can suppress the energy band bending between the source and R_{POC}. To optimize the concentration of the pocket doping (N_{POC}), the effects of the N_{POC} are evaluated with various N_{POC}s from 5×10^{17} cm^{-3} to 2.5×10^{19} cm^{-3} as shown in Fig. 4(a). As the N_{POC} increases, it is observed that the SS_{AVE} becomes steeper with the increasing V_{ON} [Inset of Fig. 4(b)] because the generation of the corner tunneling is reduced at $V_{GS} <$ 0.4 V. Fig. 4(b) shows the extracted SS_{AVE} and I_{ON} depending on the N_{POC}. It can be confirmed that the optimized N_{POC} is 2.5×10^{19}cm^{-3} with SS_{AVE} of 26 mV/dec and I_{ON} of 0.3 uA/um. Particularly, the SS_{AVE} is decreased to less than half as compared to $N_{POC} = 5 \times 10^{17}$cm^{-3} with the negligible I_{DS} change at $V_{GS} = 1.0$ V. It means that the proposed L-shaped TFET is very advantageous in terms of the supply voltage scaling.

The corner tunneling reduction by the increasing N_{POC} can be verified by the energy band diagrams along the diagonal direction [A-A' in Fig. 1(b)] near the source edge region at $V_{DS}/V_{GS} = 0.75$ V/0.3 V. Fig. 5(a) shows that the energy band of the R_{POC} goes up with the increasing N_{POC}, which results in the generation of the corner tunneling at the larger V_{GS}. Thus, it is found that BTBT rates gets dramatically reduced at $V_{GS} = 0.3$ V as the N_{POC} increases. Then, the corner tunneling rates are plotted with respect to V_{GS} as shown in Fig. 5(b). It is clearly observed that the corner tunneling becomes generated at the larger V_{GS} with the higher N_{POC}. Also, 2D BTBT rate contours are checked with $N_{POC} = 0.1$, 0.5, 1.5, and 2.5×10^{19}cm^{-3} at $V_{GS} = 0.3$ V [Fig. 5(c)]. It can be seen that the corner tunneling starts to disappear from $N_{POC} = 2.5 \times 10^{19}$cm^{-3}. Consequently, it is revealed that the proposed L-shaped TFET can have the much steeper switching characteristics and the better current drivability at the same overdrive voltage by suppressing the corner tunneling as compared to the conventional L-shaped TFET.

B. KEY PARAMETER VARIATIONS

As compared to the planar TFET, the L-shaped TFET have a strong advantage that tunneling area can be increased by vertically enlarging the source region without any dimension

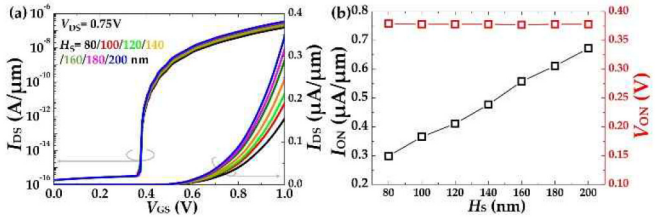

FIGURE 6. (a) Transfer characteristics with the increasing source height (H_S) at V_{DS} = 0.75 V and N_{POC} = 2.5 × 10^{19}cm^{-3}. (log/linear scales) (b) The extracted I_{ON} and V_{ON} with respect to H_S.

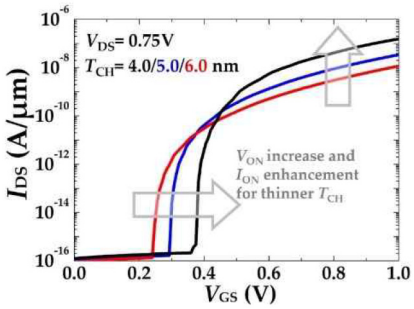

FIGURE 7. Transfer characteristics with various epi-channel thickness (T_{CH}) at V_{DS} = 0.75 V and N_{POC} = 2.5 × 10^{19}cm^{-3}.

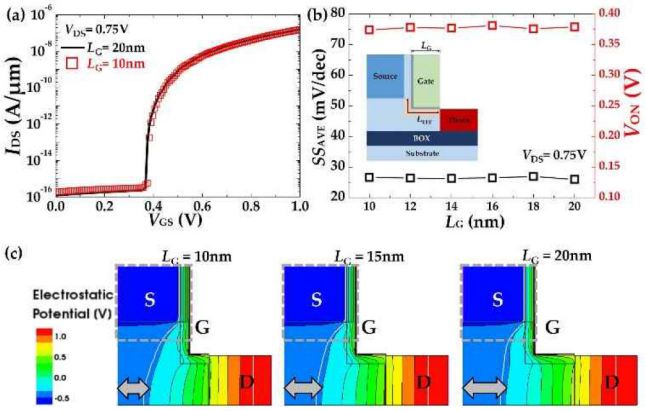

FIGURE 8. (a) Transfer characteristics of L_G = 10 and 20 nm at V_{DS} = 0.75 V. (b) The extracted SS_{AVE} and V_{ON} with respect to L_G from 10 nm to 20 nm. (c) The 2D contours of the electrostatics potential for L_G = 10, 15, and 20 nm at V_{DS}/V_{GS} = 0.75/0.3 V.

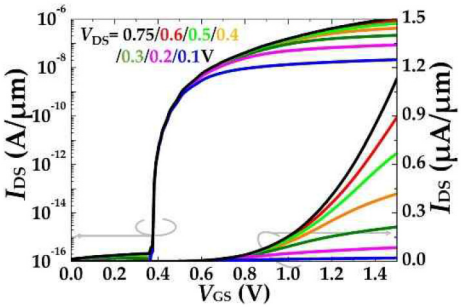

FIGURE 9. Transfer characteristics with V_{DS} of 0.1V to 0.75 V. (log/linear scales).

loss [22]. In terms of the pocket doping optimization, the effects of the key parameters such as H_S, T_{CH}, and L_G variations, which are directly related to the performance of the L-shaped TFET, needs to be evaluated. Also, the impact of the abrupt on/off transition by the pocket doping on the supply voltage (V_{DD}) scaling has to be confirmed.

Firstly, as shown in Fig. 6(a), the transfer characteristics are investigated as a function of H_S with the range from 80 nm to 200 nm at N_{POC} = 2.5 × 10^{19}cm^{-3}. As the H_S increases, the on-current gets continuously enhanced without the SS_{AVE} degradation, implying that the pocket doping has negligible impacts on the normal tunneling. This can be more clearly confirmed by the extracted V_{ON} and I_{ON} of Fig. 6(b) with respect to the H_S variation. The V_{ON} remains unchanged at V_{GS} =∼ 0.38 V regardless of the H_S, whereas the I_{ON} is linearly enhanced with the increasing H_S.

Then, the effects of T_{CH} variation from 4nm to 6nm are checked at the optimized N_{POC} [Fig. 7]. As the T_{CH} is decreased, it is found that V_{ON} gets larger and I_{ON} becomes increased. For the thinner T_{CH}, the tunneling width is reduced and the electric field across the channel is enhanced by the increasing channel capacitance [22]. Therefore, the tunneling start to be generated at the larger V_{GS} by the limited tunneling width and the driving current is improved by the better channel controllability. In this work, 4nm T_{CH} is selected to maximize the device performance.

The effects of the dimension scaling, which is considered as one of the critical factors for future technology nodes, are analyzed [27]. L_G is diminished from 20 nm to 10 nm with other parameters fixed. Then, the transfer characteristics are checked as depicted in Fig. 8(a). Interestingly, although L_G is shrunk to 10 nm, the transfer characteristics is almost the same as that of L_G = 20 nm. Fig. 8(b) shows the extracted SS_{AVE} and V_{ON} with respect to L_G. It is observed that the SS_{AVE} and V_{ON} are hardly degraded by the L_G scaling-down, meaning that the proposed L-shaped TFET is robust against short-channel effects (SCEs). This can be understood by noticing that the proposed device has the larger effective L_G (namely, L_{EFF} = defined $L_G + (H_G - H_S)$) than the defined L_G as illustrated in the inset of Fig. 8(b) and thereby it can have the strong immunities against SCEs. Moreover, based on the SS improvement at L_G = 10 nm, it can be confirmed that the pocket doping effectively suppresses the corner tunneling even in the extremely scaled L_G device. To clarify the SCE immunity of the proposed L-shaped TFET, the electrostatic potentials are simulated with L_G = 10, 15, and 20 nm at V_{DS}/V_{GS} = 0.75 V/0.3 V [Fig. 8(c)]. It is clearly seen that the change of the electrostatic potential induced by the drain voltage spreads out only in the lateral direction and thus the electrostatic potential near the source-to-channel junction (dashed gray square) is rarely modulated by V_{DS}.

Lastly, the transfer characteristics are investigated with respect to V_{DS} as shown in Fig. 9. As the V_{DS} decreases, the I_{ON} reduction is inevitable. This is because the channel inversion layer is formed by the electrons injected from the drain

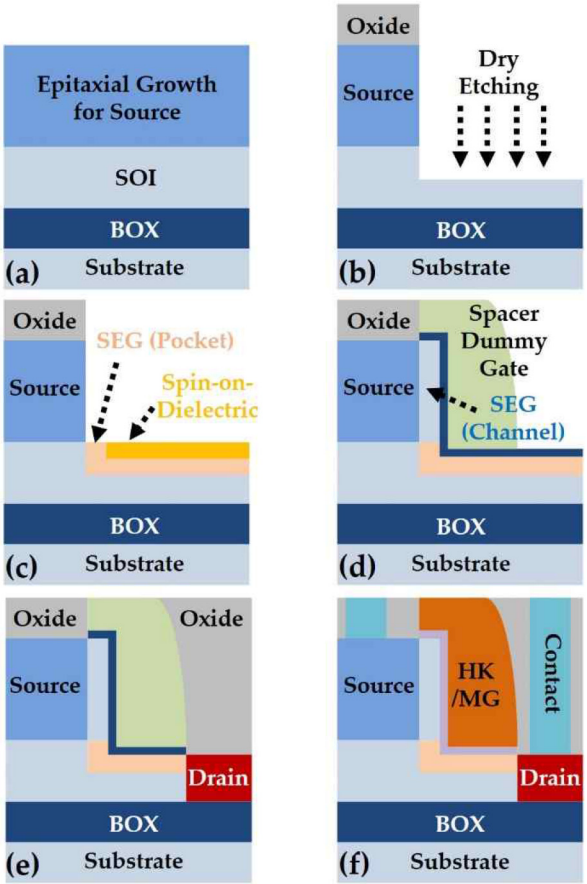

FIGURE 10. Summarized process integration for the proposed L-shaped TFET.

(that is, drain-side inversion) at the lower V_{GS}, resulting in I_{ON} saturation. Nevertheless, it is observed that the improved SS is still maintained regardless of V_{DS}. Consequently, the proposed L-shaped TFET can have the merits for the abrupt on/off transition, enhanced on-current, dimension, and V_{DD} scaling as compared to the conventional TFETs.

IV. PROCESS INTEGRATION

The proposed L-shaped TFET with doping engineering can be integrated as shown in Fig. 10. First, in-situ doped epitaxial growth on silicon-on-insulator (SOI) wafer is performed to make the source region [Fig. 10(a)]. Then, dry etching is carried out with the source region protected by an oxide hard-mask after photolithography process [Fig. 10(b)]. To form the pocket doping region, selective epitaxy growth (SEG) is conducted on the source and SOI regions. Then, spin-on-dielectric (SOD) is coated and etched back until the SOI region is exposed. By using the SOD layer, the pocket doping region is partially removed by wet chemical etchant [Fig. 10(c)]. On the exposed source region, the undoped silicon is grown by SEG to enhance tunneling current. Subsequently, sacrificial oxide and dummy gate are sequentially formed by spacer technique [Fig. 10(d)]. After that, drain implantation is performed and inter-layer dielectric (ILD) is deposited on the whole region. The ILD is planarized using chemical mechanical polishing (CMP) until dummy gate is exposed [Fig. 10(e)]. Then, dummy gate/sacrificial oxide are sequentially etched out and replaced with ALD interfacial oxide, high-k dielectric, and metal gate [Fig. 10(f)]. Back-end-of-line (BEOL) flows are skipped because it is the same as the conventional CMOS process.

V. CONCLUSION

In this study, the novel L-shaped TFET is proposed with the doping engineering underneath the gate and analyzed by the TCAD simulations with the calibrated nonlocal BTBT model. As contrast to the conventional L-shaped TFETs, the proposed device mitigates the corner tunneling, which causes poor on/off transition, and hence an abrupt switching can be successfully implemented. To optimize the N_{POC}, the device performances are evaluated in terms of SS and I_{ON}. As a result, at $N_{POC} = 2.5 \times 10^{19}\text{cm}^{-3}$, SS_{AVE} gets reduced from 60 to 26 mV/dec and I_{ON} becomes ~2.0 times increased as compared to the conventional one. Also, it is confirmed that the pocket doping effectively suppresses the corner tunneling even in the extremely scaled L_G device with the extended H_S. In addition, the process integration flow of the proposed L-shaped TFET is introduced in terms of the fabrication feasibility.

REFERENCES

[1] M. S. Lundstrom, "The MOSFET revisited: Device physics and modeling at the nanoscale," in *Proc. IEEE Int. SOI Conf.*, Niagara Falls, NY, USA, 2006, pp. 1–3, doi: 10.1109/SOI.2006.284404.
[2] T. Sakurai, "Perspectives of low-power VLSI's," *IEICE Trans. Electron.*, vol. E87-C, no. 4, pp. 429–437, 2004.
[3] M. White and Y. Chen, *Scaled CMOS Technology Reliability Users Guide*, JPL Publ., Pasadena, CA, USA, 2008, pp. 8–14. [Online]. Available: http://parts.jpl.nasa.gov/docs/NEPP07/NEPP 07~Scaled CMOS Technology Reliability Users Guide (Released CL#08-0939).pdf
[4] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–287, Mar. 2001, doi: 10.1109/5.915374.
[5] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011, doi: 10.1038/nature10679.
[6] K. K. Bhuwalka, S. Sedlmaier, A. K. Ludsteck, C. Tolksdorf, J. Schulze, and I. Eisele, "Vertical tunnel field-effect transistor," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 279–282, Feb. 2004, doi: 10.1109/TED.2003.821575.
[7] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp+ layer," *Jpn. J. Appl. Phys. I, Reg. Papers Short Notes Rev. Papers*, vol. 43, no. 7A, pp. 4073–4078, 2004, doi: 10.1143/JJAP.43.4073.
[8] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007, doi: 10.1109/LED.2007.901273.
[9] W. Y. Choi and W. Lee, "Hetero-gate-dielectric tunneling field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317–2319, Sep. 2010, doi: 10.1109/TED.2010.2052167.
[10] S. H. Kim, S. Agarwal, Z. A. Jacobson, P. Matheu, C. Hu, and T.-J. K. Liu, "Tunnel field effect transistor with raised germanium source," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1107–1109, Oct. 2010, doi: 10.1109/LED.2010.2061214.
[11] K. M. Choi and W. Y. Choi, "Work-function variation effects of tunneling field-effect transistors (TFETs)," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 942–944, Aug. 2013, doi: 10.1109/LED.2013.2264824.

[12] D. B. Abdi and M. J. Kumar, "In-built N^+ pocket p-n-p-n tunnel field-effect transistor," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1170–1172, Dec. 2014, doi: 10.1109/LED.2014.2362926.
[13] S. Guin, A. Chattopadhyay, A. Karmakar, and A. Mallik, "Impact of a pocket doping on the device performance of a schottky tunneling field-effect transistor," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2515–2522, Jul. 2014, doi: 10.1109/TED.2014.2325068.
[14] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008, doi: 10.1021/nl071804g.
[15] D. Kwon *et al.*, "Negative capacitance FET with 1.8-nm-thick Zr-doped HfO_2 oxide," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 993–996, Jun. 2019, doi: 10.1109/LED.2019.2912413.
[16] C. Hu, D. Chou, P. Patel, and A. Bowonder, "Green transistor—A VDD scaling path for future low power ICs," in *Proc. Int. Symp. VLSI Technol. Syst. Appl.*, Hsinchu, Taiwan, 2008, pp. 14–15, doi: 10.1109/VTSA.2008.4530776.
[17] K.-H. Kao *et al.*, "Optimization of gate-on-source-only tunnel FETs with counter-doped pockets," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2070–2077, Aug. 2012, doi: 10.1109/TED.2012.2200489.
[18] Ashita, S. A. Loan, and M. Rafat, "A high-performance inverted-C tunnel junction FET with source–channel overlap pockets," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 763–768, Feb. 2018, doi: 10.1109/TED.2017.2783764.
[19] G. Musalgaonkar, S. Sahay, R. S. Saxena, and M. J. Kumar, "Nanotube tunneling FET with a core source for ultrasteep subthreshold swing: A simulation study," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4425–4432, Oct. 2019, doi: 10.1109/TED.2019.2933756.
[20] G. Musalgaonkar, S. Sahay, R. S. Saxena, and M. J. Kumar, "A line tunneling field-effect transistor based on misaligned core–shell gate architecture in emerging nanotube fets," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2809–2816, Jun. 2019, doi: 10.1109/TED.2019.2910156.
[21] J. W. Lee and W. Y. Choi, "Design guidelines for gate-normal hetero-gate-dielectric (GHG) tunnel field-effect transistors (TFETs)," *IEEE Access*, vol. 8, pp. 67617–67624, 2020, doi: 10.1109/ACCESS.2020.2985125.
[22] S. W. Kim, W. Y. Choi, M.-C. Sun, H. W. Kim, and B.-G. Park, "Design guideline of Si-based L-shaped tunneling field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 51, no. 6S, 2012, Art. no. 06FE09, doi: 10.1143/JJAP.51.06FE09.
[23] S. W. Kim, J. H. Kim, T.-J. K. Liu, W. Y. Choi, and B.-G. Park, "Demonstration of L-shaped tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1774–1778, Apr. 2016, doi: 10.1109/TED.2015.2472496.
[24] S. S. Shin, J. H. Kim, and S. Kim, "L-shaped tunnel FET with stacked gates to suppress the corner effect," *Jpn. J. Appl. Phys.*, vol. 58, p. SDDE10, May 2019, doi: 10.7567/1347-4065/ab0ff1.
[25] *Sentaurus Process User Guide—V.P-2019.03*, Synopsys, Mountain View, CA, USA.
[26] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. De Meyer, "Direct and indirect band-to-band tunneling in germanium-based TFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 292–301, Feb. 2012, doi: 10.1109/TED.2011.2175228.
[27] A. Razavieh, P. Zeitzoff, and E. J. Nowak, "Challenges and limitations of CMOS scaling for FinFET and beyond architectures," *IEEE Trans. Nanotechnol.*, vol. 18, pp. 999–1004, Sep. 2019, doi: 10.1109/TNANO.2019.2942456.