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In-situ-SiN/AlN/$Al_{0.05}Ga_{0.95}N$ High Electron-Mobility Transistors on Si-Substrate Using Al_2O_3/SiO_2 Passivation

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ABSTRACT In this study, *in-situ* MOCVD-grown SiN/AlN/$Al_{0.05}Ga_{0.95}N$ HEMTs were fabricated using ALD-Al_2O_3/PECVD-SiO_2 passivation. A high on/off current ratio of 10^9 and a low subthreshold swing of 64 mV/dec are achieved. The interface traps in the SiN/AlN/$Al_{0.05}Ga_{0.95}N$ structure are investigated using frequency-dependent capacitance-voltage and conductance measurements. The shift in threshold voltage, under a gate-bias stress of 4 V for 1000 s, is less than 0.06 V for the devices with 3 nm *in-situ* SiN as gate dielectric. This indicates excellent bias-induced threshold-voltage stability. A saturated drain current of 6.4 A, a specific on-resistance of 5.37 m$\Omega\cdot cm^2$, and a high breakdown voltage of 1014 V are observed for the devices with a gate width of 20 mm. Baliga's figure of merit for the devices reaches 1.91×10^8 $V^2\Omega^{-1}cm^{-2}$, which confirms its potential for high-power-switching applications.

INDEX TERMS AlN/AlGaN heterostructure, in-situSiN, Al_2O_3/SiO_2 passivation, high-power application.

I. INTRODUCTION

AlGaN/GaN high electron-mobility transistors (HEMTs) are widely used in high-frequency and high-efficiency power converters [1]–[3]. In addition to the conventional AlGaN/GaN heterostructure in III-nitrides, many other heterostructures, such as AlN/GaN, AlGaN/GaN/AlGaN, $Al_xGa_{1-x}N/Al_yGa_{1-y}N$, AlN/AlGaN, were investigated for power switching applications [4]–[7]. Among these heterostructures, AlN/AlGaN is one of the most promising candidates because GaN-based heterostructures with a thin AlN barrier layer can be used to fabricate normally-on and normally-off devices on the same wafer, which enables monolithic integration [8], [9]. Moreover, the AlGaN channel instead of the GaN channel can improve the breakdown characteristics and shift the threshold voltage to a positive value for normally-off devices [6], [10]. Compared to GaN-channel HEMTs, AlGaN-channel HEMTs exhibit a superior thermal stability in the DC performance at elevated temperatures because of the weaker mobility degradation for the AlGaN channel heterostructure [6], [11], [12]. Until now, however, studies of AlN/AlGaN HEMTs, which are fabricated on commercial large-size Si substrates, have rarely been reported. Furthermore, studies of the passivation of AlN/AlGaN HEMTs with respect to high-voltage-and high-current - operation are also lacking.

In this paper, we fabricated *in-situ* metal organic chemical vapor deposition (MOCVD)-grown Si_3N_4/AlN/$Al_{0.05}Ga_{0.95}N$ HEMTs on 6-inch p-Si substrates for high-power applications. Atom layer deposition (ALD)-Al_2O_3 and plasma-enhanced chemical vapor deposition (PECVD)-SiO_2 were performed in sequence for passivation of Si_3N_4/AlN/$Al_{0.05}Ga_{0.95}N$ HEMTs. Compared to Si_3N_4/AlN/$Al_{0.05}Ga_{0.95}N$ HEMTs with SiO_2 passivation via PECVD, the devices, which used a passivation-process via ALD-Al_2O_3 and PECVD-SiO_2, show a much lower leakage-current of 3×10^{-7} mA/mm. Moreover, a low

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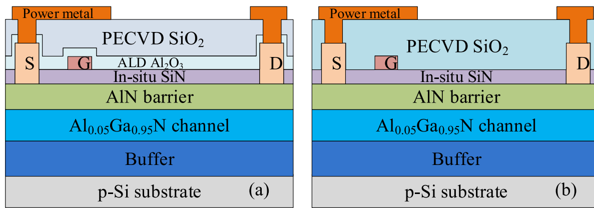

FIGURE 1. **Schematic of cross-sectional of (a) sample A with Al_2O_3/SiO_2 passivation layers and (b) sample B with a SiO_2 passivation layer.**

subthreshold swing (SS) and a high I_{ON}/I_{OFF} was attained. The performance of Si_3N_4/AlN/$Al_{0.05}Ga_{0.95}N$ HEMTs with ALD-Al_2O_3/PECVD-SiO_2 passivation layers, with a gate width of 20 mm, is also analyzed.

II. DEVICE STRUCTURE AND FABRICATION

The AlN/$Al_{0.05}Ga_{0.95}N$ epilayer, which was used in this study, was grown on a 6-inch p-type Si (111) substrate (resistivity $< 10\Omega\cdot$cm) using MOCVD. The epitaxy structure consists of (bottom to top): a 4.2 μm AlGaN buffer layer, a 300 nm $Al_{0.05}Ga_{0.95}N$ channel layer, a 5 nm AlN barrier layer, and a 3 nm *in-situ* SiN layer. The electron sheet density and electron mobility are 4.5×10^{12} cm^{-2} and 793 cm^2/Vs, respectively. The device fabrication process started with mesa isolation via inductive coupled plasma etching. *In-situ* SiN in source/drain region was removed via reactive ion etching. Subsequently, the source and drain ohmic metals Ti/Al/Ni/Au (20nm/140nm/45nm/55nm) were deposited using electron beam (EB) evaporation, followed by annealing at 865 °C for 45 s in N_2 ambient. The ohmic contact resistance of the device was 0.65 $\Omega\cdot$mm determined using the transfer length method. A Ni/Au (45nm/200nm) bilayer was deposited as gate electrode on the *in-situ* SiN to form a metal-insulator-semiconductor (MIS) gate structure. Then, the wafer was passivated with a 3 nm Al_2O_3, which was deposited using thermal ALD at 300 °C with trimethylaluminum and H_2O as precursors. An 800 nm SiO_2 was subsequently deposited using PECVD. The passivation layer above the contact pads was removed via ion-beam etching. Finally, the power metal Ni/Au (40nm/500nm) used for interconnection was deposited using EB evaporation. SiN/AlN/$Al_{0.05}Ga_{0.95}N$ HEMT with ALD-Al_2O_3/PECVD-SiO_2 passivation layers was denoted as sample A. SiN/AlN/$Al_{0.05}Ga_{0.95}N$ HEMT with an 800 nm SiO_2 passivation layer, which was deposited via PECVD, were fabricated as a reference (denoted as sample B). Fig. 1(a) and 1(b) show a cross-sectional view of sample A and sample B, respectively. The devices have a gate length (L_G) of 2 μm, a gate width (W_G) of 50 μm, and a gate-to-source (L_{GS}) distance 3 μm. The gate-to-drain distance (L_{GD}) varies from 6 μm to 32 μm.

III. RESULTS AND DISCUSSIONS

Fig. 2(a) shows the transfer and the gate leakage characteristics of both samples. Sample A showed a much lower gate

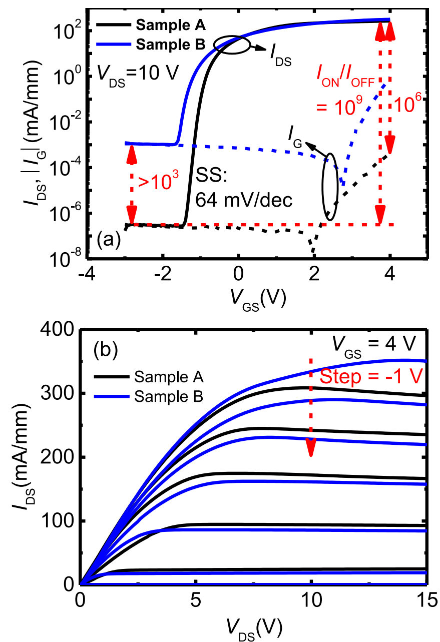

FIGURE 2. **(a) Transfer, gate leakage, and (b) output characteristics of both samples with L_{GD} = 6 μm.**

leakage than sample B, which led to a higher I_{ON}/I_{OFF} up to 10^9. In a conventional HEMT, the gate-leakage current consists of surface, bulk, and mesa edge leakages [13]. The high leakage current of sample B was caused by the surface damage that was induced by the active plasma sources during the PECVD [14], [15]. Tan *et al.* [16] proposed an electron hopping conduction involved for the gate leakage mechanism. The leakage current increased after SiO_2 passivation, as the effective barrier height for the hopping conduction process has been reduced [16]. Compared to PECVD-SiO_2, the amount of damage introduced by ALD-Al_2O_3 passivation could greatly be reduced. Moreover, ALD-Al_2O_3 passivation has shown significant advantages in suppressing current collapse [17], [18]. The low dielectric constant of SiO_2 is attractive for passivation layer applications because the parasitic capacitance of the devices can be significantly reduced. Therefore, an ALD-Al_2O_3/PECVD-SiO_2 bilayer was used instead of PECVD-SiO_2 as passivation layer. For sample A, the ratio of I_{DS} to I_G at V_{GS} = 4 V reached up to 10^6, which ensures good gate reliability. Moreover, a low SS of 64 mV/dec was obtained for sample A. Sample B showed a more negative threshold voltage and a high I_{ON} than sample A, which indicates that sample B has a higher carrier concentration in the channel. It is possible that the increase in carrier concentration may be Si-related. One explanation could be the incorporation of Si as a shallow donor at the AlGaN surface for sample B [19]. The incorporation of Si was blocked by Al_2O_3 layer for sample A. Therefore, sample B showed a higher saturated drain current (I_{ds-max}) than sample A, as shown in Fig. 2(b). The saturated drain current of both samples is lower than that of conventional

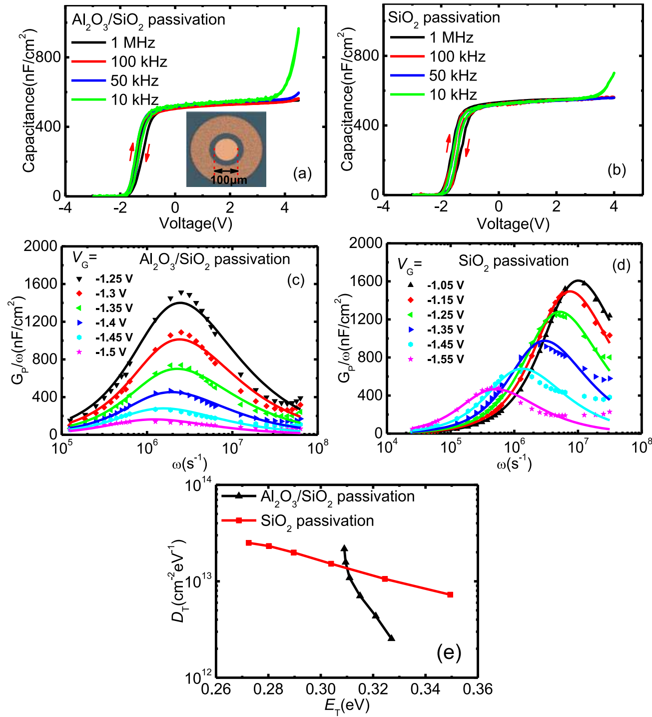

FIGURE 3. ***C-V*** **characteristics of the MIS capacitors with (a) Al_2O_3/SiO_2 passivation and (b) SiO_2 passivation at different frequencies with bidirectional sweeps. The inset shows the top view of SiN/AlN/$Al_{0.05}Ga_{0.95}N$ MIS capacitor with Al_2O_3/SiO_2 passivation. (c-d) Conductance as a function of radial frequency (full lines represent the fitted curves), and (e) trap state density as a function of the energy level below the conduction band for the MIS capacitors.**

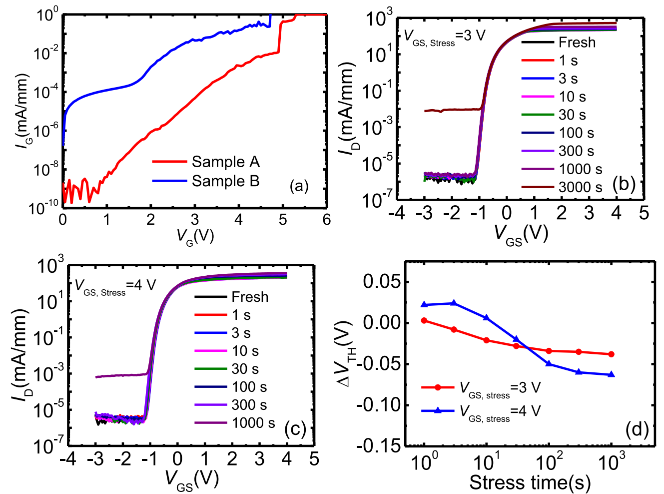

FIGURE 4. (a) Forward I_G-V_G measurement, on a semi-log scale, of both samples. I_D-V_{GS} curves of sample A with gate-bias stress of (b) 3 V for 3000 s and (c) 4 V for 1000 s at room temperature. (d) Threshold-voltage shift ΔV_{TH} induced by different gate-bias stresses for 1000 s.

AlGaN/GaN HEMTs due to the high sheet resistance for AlN/$Al_{0.05}Ga_{0.95}N$ heterostructure. It can be improved further by optimizing material growth process in subsequent studies.

Frequency-dependent capacitance and conductance measurements were performed to investigate trap states in the SiN/AlN/$Al_{0.05}Ga_{0.95}N$ structures. Circular-shaped Ni-Au/SiN/AlN/$Al_{0.05}Ga_{0.95}N$ MIS capacitors with Al_2O_3/SiO_2 passivation and SiO_2 passivation was used for these measurements. The diameter of the circular area is 100 μm. A hysteresis and frequency dispersion near the threshold voltage can be seen in the capacitance-voltage curves in Figs. 3(a-b), which is induced by the trap states in AlN/$Al_{0.05}Ga_{0.95}N$ structure. The conductance, as a function of radial frequency for the MIS capacitors near the threshold voltage, is shown in Figs. 3(c-d). Furthermore, the trap state density and energy levels were extracted, see Fig. 3(e), using the method in Ref. 20. In the AlN/$Al_{0.05}Ga_{0.95}N$ heterostructure with Al_2O_3/SiO_2 passivation, the trap state density ranged from 2.17×10^{13} $cm^{-2}eV^{-1}$ to 2.54×10^{12} $cm^{-2}eV^{-1}$ was located at energy level between 0.309 eV and 0.327 eV below the conduction band. This is a similar range as the trap state density and energy levels in the AlGaN/GaN heterostructure [20], [21]. In the AlN/$Al_{0.05}Ga_{0.95}N$ heterostructure with SiO_2 passivation, the trap state density ranged from 2.50×10^{13} $cm^{-2}eV^{-1}$ to 7.26×10^{12} $cm^{-2}eV^{-1}$ was located at energy level between 0.273 eV and 0.349 eV below the conduction band. The AlN/$Al_{0.05}Ga_{0.95}N$ heterostructure with SiO_2 passivation showed a higher trap state density and a broader energy level than that with Al_2O_3/SiO_2 passivation. Shallow trap levels dominate the gate leakage current [20]. Therefore, sample B showed a higher gate leakage than sample A.

It is noteworthy that the strong frequency dispersion near 4 V, as shown in Figs. 3(a-b), means that a high density of traps is present at the SiN/AlN interface. These interface traps have a significant impact on device reliability, especially the threshold-voltage stability [22], [23]. To evaluate the gate reliability and the threshold-voltage stability of both samples, both the forward gate breakdown characteristics and the bias-induced threshold voltage-instability were investigated. Fig. 4(a) shows forward $I_G - V_G$ curves, on a semi-log scale, for both samples. The gate breakdown-voltage was about 5 V and 4.7 V for sample A and sample B, respectively, with 3 nm *in-situ* Si_3N_4 insulator. Figs. 4(b) and 4(c) show the I_D-V_{GS} curves of sample A, with a gate-bias stress of 3 V for 3000 s and 4 V for 1000 s, respectively. The threshold voltage was defined as the gate voltage at $|I_D| = 10^{-3}$ mA/mm. As the time of gate bias stress increased, shifts in the threshold voltage occurred - see Fig. 4(d). The threshold voltage shifting for the forward gate bias stresses was caused by the traps existing in the AlN barrier layer or SiN dielectric layer [24]. The shifts in threshold voltage under gate-bias stresses of 3 V and 4 V for 1000 s were below 0.04 V and 0.06 V, respectively. Sample A exhibits excellent bias-induced threshold-voltage stability. The shift in threshold voltage increased in absolute value with increasing gate-bias stress and stress time.

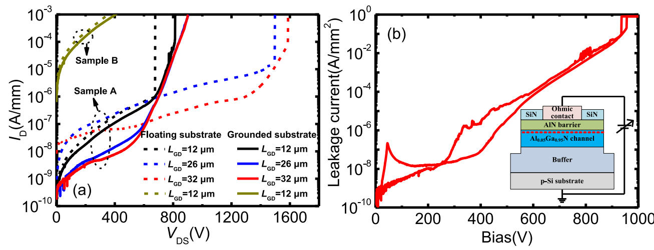

FIGURE 5. (a) Breakdown characteristics of both samples with different values for L_{GD}. (b) Vertical breakdown characteristics of SiN/AlN/$Al_{0.05}Ga_{0.95}$N on Si. Top mesa area was 100 × 100 μm².

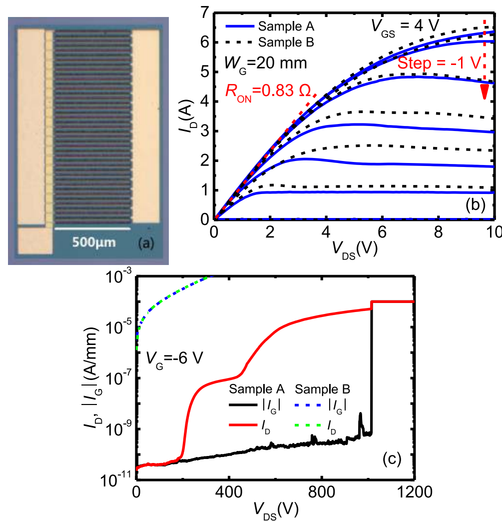

FIGURE 6. (a) Top view of the SiN/AlN/$Al_{0.05}Ga_{0.95}$N HEMTs with Al_2O_3/SiO_2 passivation and W_G = 20 mm. (b) Pulsed I_D-V_{DS} curves of both samples. A pulse width and period of 500 μs and 500ms were used, respectively. (c) Breakdown characteristics of both samples.

Moreover, the device failed more likely, when the gate-bias stress increased.

The breakdown characteristics of both samples with different values for L_{GD} are shown in Fig. 5. The V_{BR} is defined for an off-state current of 10 μA/mm. For sample A with a floating substrate, the V_{BR} of the devices with L_{GD} = 12 μm, 26 μm, and 32 μm were 675 V, 1428 V, and 1488 V, respectively. For sample A with grounded substrate, V_{BR} of 756 V, 772 V, and 772 V were obtained for devices with L_{GD} of 12 μm, 26 μm, and 32 μm, respectively. The V_{BR} with the grounded substrate hardly increased with increasing L_{GD} due to the vertical breakdown of SiN/AlN/$Al_{0.05}Ga_{0.95}$N on Si. Sample B showed a much lower V_{BR} than sample A due to its higher leakage current. Fig. 5(b) shows the vertical breakdown characteristics of SiN/AlN/$Al_{0.05}Ga_{0.95}$N on Si. The measurement setup is shown in the inset of Fig. 5(b). A hard breakdown voltage around 940 V was obtained for the epilayer. Therefore, the V_{BR}, with a grounded substrate for the sample A, could be increased by increasing the thickness of the epilayer or improving the crystalline quality of the epilayer in a future study.

TABLE 1. Comparison of AlN/AlGaN HEMTs.

Ref.	I_{ON}/I_{OFF}	SS (mV/dec)	$R_{on,sp}$ (mΩ·cm²)	V_{BR} (V)	FOM ($V^2Ω^{-1}cm^{-2}$)
[7]	10^7	75	643*	810	$1.02×10^6$
[25]	/	/	37.9*	/	/
This work	10^9	64	14.4*	1428	$1.42×10^8$
	/	/	5.37**	1014	$1.91×10^8$

Note: *Calculated by using $R_{on,sp} = R_{on} × (L_{SD} + (1.5 × 2)$ μm), considering a 1.5 μm transfer length for the source/drain ohmic contacts for small area devices. **Calculated by using $R_{on,sp} = R_{on}$ × A, where A is the active device area for large area devices.

To further evaluate their potential in high-power applications, SiN/AlN/$Al_{0.05}Ga_{0.95}$N HEMTs, with W_G = 20 mm, were fabricated with Al_2O_3/SiO_2 passivation and SiO_2 passivation. They had a L_G of 2 μm, a L_{GS} of 3 μm, a L_{GD} of 17 μm, a source field plate of 4 μm, a drain field plate of 1 μm, and a gate-finger width of 500 μm. The top view of the device is shown in Fig. 6(a). Fig. 6(b) exhibits pulsed I_D-V_{DS} tests for both samples. The quiescent drain bias was set to 0 V, and a pulse width and period of 500 μs and 500 ms were used, respectively. A saturated drain current of 6.4 A and an on-resistance of 0.83 Ω were obtained for sample A with Al_2O_3/SiO_2 passivation. The specific on-resistance ($R_{on,sp}$) of sample A was 5.37 mΩ·cm², considering the active area. Sample B showed a slightly higher saturated drain current than sample A due to its higher carrier concentration. Fig. 6(c) shows the off-state breakdown characteristics for both samples. For sample A, a hard breakdown voltage of 1014 V was observed resulting from the surge in gate current. The gate current of sample B is almost equal to the drain current, which indicates that the breakdown of sample B is caused by gate leakage. Baliga's Figure of merit (FOM = $V_{BR}^2/R_{on,sp}$) for sample A reached 1.91×10^8 $V^2Ω^{-1}cm^{-2}$, the highest among the reported values for AlN/AlGaN HEMTs. Table 1 shows the comparison of AlN/AlGaN HEMTs. The devices in this work show an excellent performance in terms of I_{ON}/I_{OFF}, SS, $R_{on,sp}$, V_{BR}, and FOM. These results indicate its potential for high power applications.

IV. CONCLUSION

We fabricated SiN/AlN/$Al_{0.05}Ga_{0.95}$N HEMTs with *in-situ* SiN as gate dielectric using ALD-Al_2O_3/PECVD-SiO_2 passivation. The devices showed an extremely low reverse gate leakage of 3×10^{-7} mA/mm, a high I_{ON}/I_{OFF} of 10^9, and a low SS of 64 mV/dec. The gate reliability, which was induced by the interface traps, was investigated via gate-breakdown and bias-induced threshold voltage-instability measurements. The shift in threshold voltage increased with increasing gate-bias stress and stress time. Furthermore, the threshold-voltage shift, under gate-bias stress of 4 V for 1000 s, was below 0.06 V. The devices with a W_G of 20 mm showed a saturated drain current of 6.4 A, a specific on-resistance of 5.37 mΩ·cm², a high breakdown voltage of 1014 V, and a Baliga's FOM of 1.91×10^8 $V^2Ω^{-1}cm^{-2}$. These results indicate that *in-situ*-SiN/AlN/$Al_{0.05}Ga_{0.95}$N

HEMTs, with ALD-Al_2O_3/PECVD-SiO_2 passivation, are promising devices for high-power applications.

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