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Etched-and-Regrown GaN *pn*-Diodes With 1600 V Blocking Voltage

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ABSTRACT Etched-and-regrown GaN pn-diodes capable of high breakdown voltage (1610 V), low reverse current leakage (1 nA = 6 μA/cm^2 at 1250 V), excellent forward characteristics (ideality factor $\sim$ 1.6), and low specific on-resistance (1.1 mΩ.cm^2) were realized by mitigating plasma etch-related defects at the regrown interface. Epitaxial *n*-GaN layers grown by metal-organic chemical vapor deposition on free-standing GaN substrates were etched using inductively coupled plasma etching (ICP), and we demonstrate that a slow reactive ion etch (RIE) prior to *p*-GaN regrowth dramatically increases diode electrical performance compared to wet chemical surface treatments. Etched-and-regrown diodes without a junction termination extension (JTE) were characterized to compare diode performance using the post-ICP RIE method with prior studies of other post-ICP treatments. Then, etched-and-regrown diodes using the post-ICP RIE etch steps prior to regrowth were fabricated with a multi-step JTE to demonstrate kV-class operation.

INDEX TERMS Gallium nitride, p-n junctions, power semiconductor devices, epitaxial growth.

I. INTRODUCTION

GaN offers increased power density for power electronics due to its larger band gap energy (E_g) compared to Si [1]–[9]. The critical electric field scales as $\sim E_g^{2.5}$ [10] to enable greater than 100x higher maximum voltage (V_{max}) at a given doping level than Si can achieve. However, selective area doping has been difficult to achieve in GaN, and this has limited the development GaN vertical power devices including metal-oxide semiconductor field effect transistors and junction barrier Schottky diodes. Ion implantation of Mg to selectively form *p*-type GaN regions has been demonstrated [11], but kV operation with low leakage remains elusive. Selective-area epitaxy can also form *p*-regions in *n*-GaN by using plasma-based etching followed by *p*-GaN regrowth, but etch-induced defects cause severe junction leakage [12]. Etched-and-regrown diodes with $V_{max} > 1.2$ kV have been reported using low power plasma etching to minimize etch damage, however, the forward current density was low (0.2 kA/cm^2 at 5 V) compared to continuously-grown GaN diodes [13]. Use of wet chemical treatments for defect mitigation following plasma-based etching has produced pn-diodes with $V_{max} > 600$ V, but the reverse leakage was still orders-of-magnitude higher than is observed in continuously-grown diodes [14].

In this work, we show that a combination of reactive ion etching (RIE) and AZ400K chemical treatment can achieve low leakage and high voltage operation of etched-and regrown GaN pn-diodes while preserving good forward characteristics. Initial experiments were performed with diodes lacking a junction termination extension (JTE) to compare with our prior studies of post-ICP methods of mitigating plasma etched-induced defects. Upon demonstrating superior performance of the RIE treatment, we fabricated etched-and-regrown diodes using the RIE treatment combined with a multi-step JTE to demonstrate 1.6 kV breakdown.

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II. DEVICE GROWTH AND FABRICATION

GaN pn-diodes were grown by metal-organic chemical vapor deposition (MOCVD) on two-inch diameter, free-standing n-GaN substrates with a nominal threading dislocation density $< 10^6$ cm^{-2} and resistivity $\sim 10^{-2}$ Ω-cm. The *n*-GaN drift region was 10 μm thick with a net donor density $\sim 2.7 \times 10^{16}$ cm^{-3} measured by capacitance-voltage assuming a relative permittivity value of 9 for GaN. Following n-GaN growth, 400 nm was etched from the entire surface using a $Cl_2/BCl_3/Ar$ inductively-coupled plasma (ICP) etch with 125 W for the ICP power and 10 W for the radio frequency (RF) power. The entire wafer was then etched to a depth of 270 nm by reactive ion etching (RIE) using 45 sccm CF_4 + 5 sccm O_2 gas chemistry with 25 W RF power, resulting in a 0.3 Å/s etch rate to remove defective material left by the ICP step. The RIE etch depth was chosen to be as deep as was practical given time and tool constraints for a slow etch (150 minutes) to attempt to remove as much ICP-induced damage as possible. Shorter etch times were not attempted. Following RIE, residual fluorine was removed from the surface using an HF dip, rinse, and anneal at 400 °C for 10 minutes in a nitrogen environment. The surface was then treated with AZ400K (2% KOH and 5-15% potassium borates in water by weight) at 80 °C for 10 minutes to remove remnant surface damage [14].

The first round of diodes was fabricated without JTE. A 0.4 μm thick *p*-type GaN epilayer with a Mg concentration of 3×10^{19} cm^{-3} was then regrown via MOCVD. The anode was formed by e-beam deposition of 150 μm diameter Pd/Au p-type ohmic contacts on the *p*-GaN. Isolation trenches were ICP-etched around the *p*-contacts down into the *n*-GaN drift region but were not deep enough to provide significant electric field control [8]. No surface passivation was used. The ohmic *n*-contact was formed on the back of the substrate using a blanket Ti/Al layer.

The second round of diodes used the same fabrication steps as above with the addition of a multi-step JTE [15]. A 0.3 μm thick *p*-type GaN epilayer with a Mg concentration of 10^{18} cm^{-3} capped with a 0.1 μm thick layer with Mg concentration of 3×10^{19} cm^{-3} was then regrown via MOCVD. Etch depths of 200, 260, and 300 nm in the *p*-GaN were patterned using multiple photolithography steps and ICP etch conditions described above. The etch depth increased with increasing distance from the anode. The step widths were 50 μm starting from the edge of the anode. A fourth ICP etch through the junction was performed to provide electrical isolation. No surface passivation was used. The ohmic *n*-contact was formed on the back of the substrate using a blanket Ti/Al layer.

III. IMPACT OF POST-ICP RIE TREATMENT ON DIODE PERFORMANCE

This section describes the diode electrical performance achieved with the RIE treatment following ICP etch. No JTE was used with this first study to make consistent comparison to previously studied etched-and-regrown diodes with different post-etch treatments. The reverse characteristics are compared to prior studies, including continuously-grown, regrown without etch, etched-and-regrown without post-ICP treatment, and etched-and-regrown using only a wet chemical post-ICP treatment. It is demonstrated that the RIE treatment greatly improves the reverse bias leakage compared to these other cases.

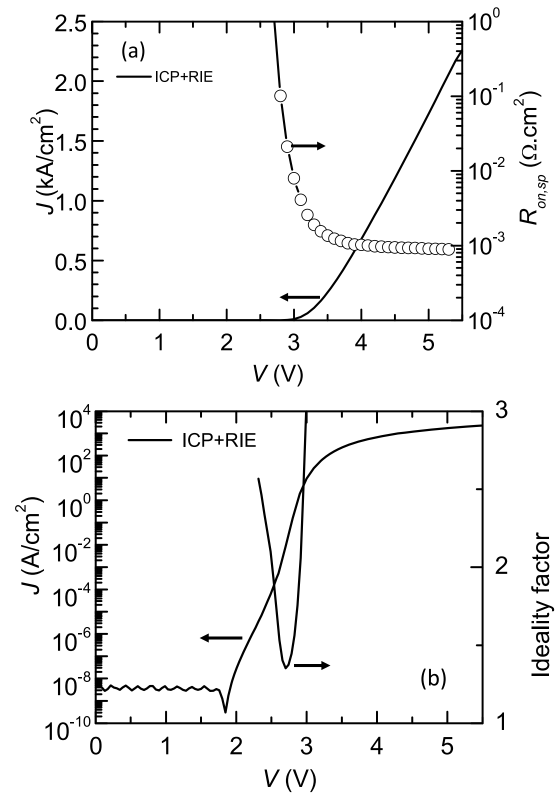

FIGURE 1. Forward *I-V* characteristics of the RIE+ICP diode (a) plotted on a linear scale with calculated differential on-resistance and (b) plotted on a logarithmic scale with calculated ideality factor.

Figure 1(a) shows the forward DC current-voltage (*I-V*) characteristics on a linear scale for the etched-and-regrown diode (termed ICP+RIE). The ICP+RIE diode showed a sharp turn-on at 3 V. The differential specific on-resistance ($R_{on,sp}$) plotted in Fig. 1(a) achieved $R_{on,sp} = 0.9$ mΩ.cm^2 and a current density of 2.0 kA/cm^2 at 5.2 V. The diode area was defined as the anode size. Figure 1(b) displays the same forward *I-V* data on a logarithmic scale to show the low forward leakage prior to diode turn-on. Between 2.6 – 2.9 V, the diode began to conduct, and the extracted ideality factor (n) in this bias range was 1.3. This n value is close to the ideal $n = 1$ case for a diode whose current is dominated by recombination in the quasi-neutral regions rather than recombination at defects in the depletion region. Thus, the $n \sim 1$ regime observed for the etched-and-regrown diode indicates a high-quality regrown junction. Forward characteristics of a continuously-grown diode (CT) grown in the same reactor under nominally the same conditions, grown on substrates from the same vendor, and fabricated in the

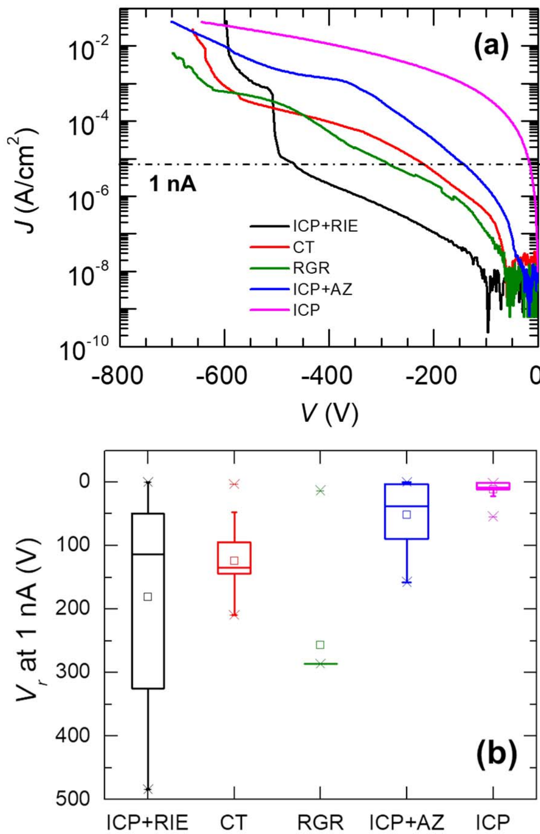

FIGURE 2. (a) Reverse I-V data for diodes formed by etch-and-regrowth with post-ICP RIE treatment (ICP+RIE), continuous growth (CT), regrowth without and etch (RGR), etch-and-regrowth with a post-ICP AZ400K treatment (ICP+AZ) and etch-and-regrowth with not post-ICP treatment and (b) box plots of the reverse voltage at 1 nA leakage.

same fashion as the ICP+RIE diode have been described previously [14] up to $J = 50$ A/cm^2. The forward leakage and specific on-resistance of the CT diodes were similar to ICP+RIE, however, the CT diodes had an ideality factor = 2.0.

The reverse *I-V* data for the ICP+RIE diode are shown in Fig. 2(a). For comparison, *I-V* data [14], [16] for the CT diode, a regrown diode that was removed from the growth reactor but not etched prior to regrowth (RGR), an etched-and-regrown diode without any post-etch defect mitigation (ICP), and an etched-and-regrown with AZ400K treatment following ICP (ICP+AZ) are also shown in Fig. 2(a). The RGR, ICP and ICP+AZ diodes were grown in the same reactor under nominally the same conditions, grown on substrates from the same vendor, and fabricated in the same fashion as the ICP+RIE diode described in this study.

The CT, RGR, ICP and ICP+AZ diodes were discussed previously [14], [16] and the results are summarized here. The CT and RGR reverse characteristics are similar, which demonstrates that regrowth without a plasma etch did not introduce significant defectivity. However, the ICP diode exhibited ∼ 500x higher leakage compared to the CT and RGR diodes. This excess leakage was attributed to band-to-band tunneling through a near-mid-band gap deep level in *n*-GaN at $E_c - 1.9$ eV, where E_c is the conduction band minimum energy. A strong increase in the concentration of the $E_c - 1.9$ eV deep level was measured by steady-state photocapacitance and was quantitatively correlated with increased leakage [14]. Treating the ICP-etched surface with AZ400K prior to regrowth reduced the leakage by >10x compared the ICP diode but did not recover the lower leakage seen for CT and RGR diodes [14]. The $E_c - 1.9$ eV deep level was only partially mitigated by AZ400K surface treatment, which is consistent with reduced leakage and suggests that the defect also incorporates below the surface due to ion channeling during ICP etching.

The RIE step was added to remove sub-surface damage from the ICP etch. The etch conditions were used previously to form recessed gates with low leakage in AlGaN high electron mobility transistors [17], which suggests that the etch causes little damage to the remaining crystal. Indeed, the RIE treatment reduced reverse leakage for the ICP+RIE diode by >1000x compared to the ICP diode and by >100x compared to just AZ400K alone [14]. The ICP+RIE diode attained reverse voltage (V_r) of 450 V at 1 nA (6 μA/cm^2), and V_{max} (defined as voltage at 1 A/cm^2) of 600 V. Reduction of reverse leakage, i.e., increase in V_r achieved at 1 nA, rather than increase in V_{max} was taken as the key indicator of defect mitigation because the electric field distribution that dictates breakdown was not well controlled due to lack of a JTE. Figure 2(b) shows box plots of V_r at 1 nA for the various diodes to demonstrate the statistical significance of the improved performance of the ICP+RIE compared to the ICP+AZ. Over one hundred diodes were tested for each of the ICP+RIE and ICP+AZ device types, and 25 – 30 diodes were tested for the other samples. The upper quartile of the ICP+RIE population achieved more negative V_r compared to the ICP+AZ diodes. The effect of an RIE etch without subsequent AZ400K treatment was not studied, but the modest reduction of leakage with just AZ400K compared to RIE and AZ400K suggests that the RIE step was more effective in reducing leakage.

Sidewall leakage is not expected to be a significant contribution to the reverse leakage. Sidewall leakage manifested as a sharp increase in reverse leakage at low V_r (∼ 20 V) that scaled with perimeter in previous work on etched-and-regrown diodes using selective area regrowth of *p*-GaN in *n*-GaN wells using the same substrate vendor, growth reactor, and diode fabrication method. This hallmark of sidewall leakage was not observed in the planar regrowth diodes discussed here.

Given the previous correlation of excess leakage and plasma etch-induced defects [14], the significant reduction in leakage with the RIE treatment likely resulted from removal of defective material. Thus, the combination of RIE and AZ400K for the ICP+RIE diode sufficiently mitigated ICP-induced damage such that diode performance was not limited by the ICP etch. However, quantitative evidence of deep

level defect reduction near the etched-and-regrown interface using RIE has not been established yet, and this subject is under further investigation. Indeed, the act of regrowth itself could form defects after the RIE etch that impact device performance. Exposing the n-GaN surface to growth temperatures could cause thermal decomposition, leading to the formation of nitrogen vacancies (V_N). Prior studies have associated V_N created by plasma etching of sidewalls to increased reverse leakage at low V_r (~50 V) in GaN pn-diodes [18]. Removal of the damaged material using ozone oxidation and wet etching of the oxide reduced the reverse leakage [18]. For the ICP+RIE diode, V_N incorporation at the junction during regrowth could also contribute to reverse leakage.

It is notable that the ICP+RIE diode achieved a higher V_r at 1 nA compared to the CT and RGR diodes. The box plots in Fig. 2(b) show that this trend is statistically significant, in that the top quartile of the IVP+RIE diodes achieve larger V_r at 1 nA compared to the CT and RGR diodes. If diode reverse bias performance was mainly dictated by etch-induced defects, the CT, RGR, and ICP+RIE diode should have similar leakage. The ~10x lower reverse leakage for ICP+RIE diode (up to $V_r = 450$ V where leakage is likely influenced more by junction material quality rather than control of peak electric field) could result from dopant compensation by impurities near the regrown junction. Conversely, the RGR diode did not have elevated Si at its regrowth interface [16]. Intentional low doping on the *n*-side of the junction has been used previously to produce record V_{max} in continuously-grown [4], [5] and regrown [9] GaN diodes, and reduce leakage in etched-and-regrown GaN diodes [13]. It is possible that ICP+RIE diodes reported here enjoy a similar benefit due to compensation of Mg on the *p*-side of the regrown junction by unintentionally incorporated impurities.

Figure 3 presents secondary ion mass spectroscopy (SIMS) data for the ICP+RIE diode that show significant compensation on the *p*-side of the junction. The regrowth interface is marked by a spike in the Si concentration that is often observed with GaN regrowth [19]. Spikes in C and O concentrations were also evident at the regrowth interface, but their areal densities were < 10x than that of Si. The Si, O, and C spikes are attributed to surface contamination from ambient exposure because our previous work showed that regrowth without removing the wafer from the growth reactor produces no measurable increase in these impurities [16]. The difference in acceptor and donor concentration ($N_a - N_d$) near the regrowth interface is also shown in Fig. 3, where Si is the donor and it is assumed that 75% of the Mg-H complexes were dissociated by thermal annealing [20]. Thus, SIMS data confirm that effective doping on the *p*-side near the junction was significantly reduced by the Si spike for the RIE+ICP diode. It is possible that the effective reduction in *p*-type doping at the regrown junction acts as an unintentional JTE, similar to a bi-layer JTE achieved by reducing p-type doping near the junction by ion implantation [21].

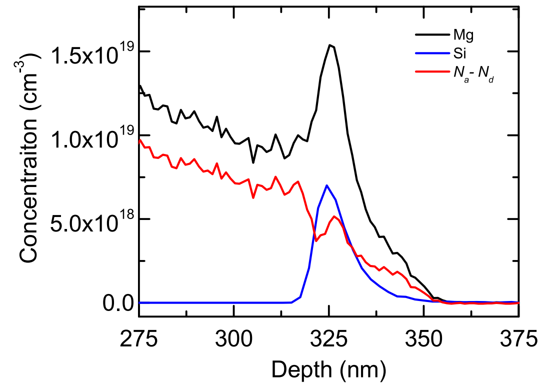

FIGURE 3. SIMS data of the RIE+ICP diode showing high Si concentration at the regrown interface. The effective p-doping density is also shown.

Nitrogen vacancies (V_N) at the regrowth interface could also contribute to an unintentional JTE by compensating Mg. As discussed above, it is possible that a large density of V_N exist at regrowth interface of ICP+RIE diode. Since V_N is donor-like, this defect would cause additional compensation of the Mg on the p-side of the ICP+RIE diode beyond that measured by SIMS. The presence of donor-like defect that forms an unintentional JTE would explain why the RGR diode exhibited improved reverse leakage compared to the CT diodes, despite the RGR diode having no significant interfacial Si [16]. In such a case, V_N would play a complex role in regrown junctions by increasing leakage at low V_r but improving electric field management at high V_r.

Determining how reduced *p*-side doping near the regrowth interface could reduce reverse leakage by 10x is beyond the scope of this work, as the present focus is the mitigation of the 100,000x increase in reverse leakage in etched-and-regrown GaN diodes.

IV. ETCHED-AND-REGROWN DIODE WITH ETCH DAMAGE MITIGATION AND JUNCTION TERMINATION EXTENSION

A new set of etched-and-regrown diodes using the ICP+RIE method for etch damage mitigation were grown and fabricated with a JTE to demonstrate that the ICP+RIE method described here achieves kV-class devices. These devices are termed ICP+RIE (JTE). The epitaxial structure was altered slightly, where a lighter-doped *p*-GaN region (Mg = 10^{18} cm^{-3}) was included at the regrowth interface. This layer with reduced Mg concentration was included to ensure a region of low *p*-type doping near the regrowth interface without relying on uncontrolled impurity incorporation during regrowth. The substrate, growth conditions, and ICP and RIE etch conditions were nominally the same as the diodes in Section III.

The forward characteristics for the ICP+RIE (JTE) diode are shown in Figure 4. The ICP+RIE (JTE) diodes had low leakage and regions of $n = 2.1$ and $n = 1.5$, as expected for high quality diodes. The $R_{on,sp}$ values were slightly higher for the ICP+RIE (JTE) samples at 1.1 mΩ.cm^2. The excellent forward bias behavior of the ICP+RIE (JTE) devices

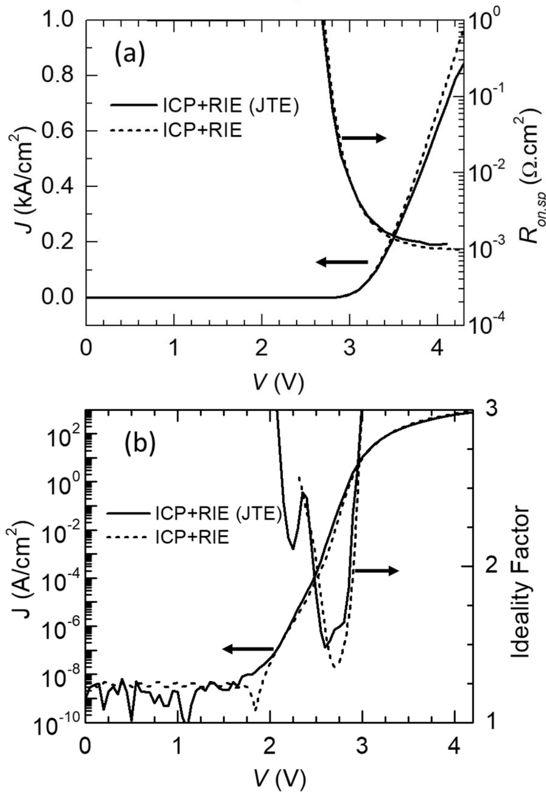

FIGURE 4. Forward *I-V* characteristics of the RIE+ICP (JTE) diode (a) plotted on a linear scale with calculated differential on-resistance and (b) plotted on a logarithmic scale with calculated ideality factor. The ICP+RIE data from Fig. 1 have been replotted for comparison.

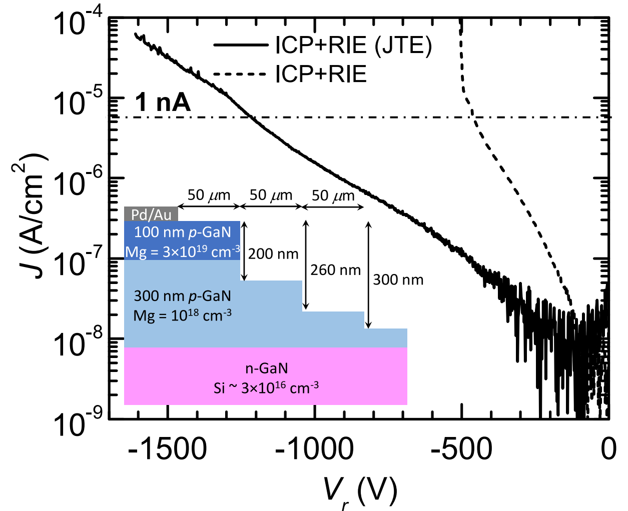

FIGURE 5. Reverse I-V data for RIE+ICP (JTE) diode compared to continuously-grown didoes and didoes regrown without and etch. The ICP+RIE data from Fig. 2(a) have been replotted for comparison. The inset is a cross-section of the ICP+RIE (JTE) structure (not to scale).

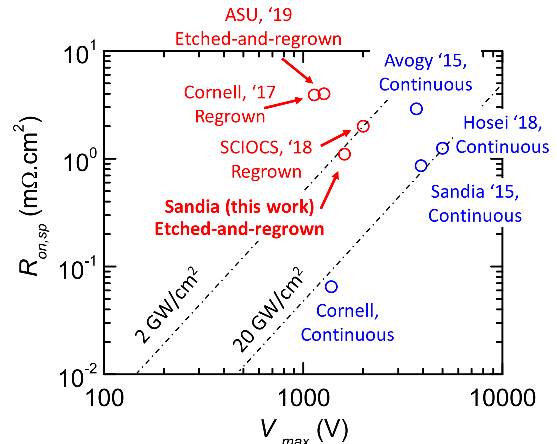

FIGURE 6. Figure-of-merit comparison of continuously-grown [1, 2, 5, 7], regrown [6, 9], and etched-and-regrown diodes [13]. $R_{on,sp}$ datum from [13] is reported at 5 V for comparison to the diodes under study.

reaffirms the efficacy of etch damage mitigation using the ICP+RIE process.

Figure 5 shows the reverse bias electrical data for the ICP+RIE (JTE) device. Reverse leakage of the ICP+RIE (JTE) diode did not exceed 1 nA until V_r = 1250 V, and the device went into breakdown at 1610 V. Greatly reduced leakage with the three-step JTE confirms that etched sidewall leakage contributes less than 1 nA of current at < 1 kV. The relative importance of the JTE versus the low *p*-GaN doping to achieve reduced leakage and increased V_r is the subject of future study in continuously-grown diodes where impurity spikes and etch damage are not convolving factors. Comparison of the reverse bias data in Fig. 2 without JTE and Fig. 5 with JTE shows that useful trends in reverse leakage and etch damage mitigation can be observed in GaN diodes without the added complexity of a JTE, however, a JTE is required to assess a breakdown voltage and reverse leakage for a realistic power device.

Figure 6 plots $R_{on,sp}$ *vs.* V_{max} for the ICP+RIE (JTE) diode compared to previously reported regrown and continuously-grown diodes. The ICP+RIE (JTE) diode compares well against reports for GaN diodes regrown without etch by MBE [6] and hybrid hydride vapor phase-MOCVD methods [9] and etched-and-regrown diodes by MOCVD [13]. The Cl-based ICP etching method in [13] used a low RF power (2 W) to reduce the physical component of the etch and therefore reduce damage to the crystal. In contrast, this work used an F-based RIE etch with 25 W RF power and a likely lower plasma density to remove damage caused by a Cl-based ICP etch. The higher RF power of the RIE method used here might suggest a more physical etch that creates more damage and reverse leakage compared to ICP in [13], however, the former resulted in a lower leakage diode. This observation suggests that, in addition to RF power, etch chemistry and plasma density are important factors that impact plasma etch-induced defects contributing to leakage in GaN diodes. The etch process in [13] was slow (0.3 nm/s), and the RIE process here was 10x slower, so the common element of slowly removing material via dry etch might be key to avoiding damage to the crystal.

The ICP+RIE(JTE) diode has a $V_{max}{}^2/R_{on,sp}$ figure-of-merit of 2.4 GW/cm^2, which is well below that reported for continuously-grown GaN diodes. Indeed, the best continuously-grown GaN diodes have reached the theoretical limit of 20 GW/cm^2 figure-of-merit, assuming an electron mobility of 1500 cm^2/Vs and a critical electric field of 4 MV/cm. Thus, despite the mitigation of etch damage, etched-and-regrown GaN diodes require further improvements to reach equivalence to continuously-grown diodes. The discrepancy could be due to 1) accelerated breakdown due to remnant etch-related defects, 2) excess resistance due to the drift region being thicker than necessary for the realized V_{max}, 3) non-optimized JTE, or a combination thereof.

Finally, scalability to larger device size for the etch-and-regrowth and JTE methods described here is considered. Devices large than 150 μm diameter were not fabricated. Nonetheless, the etch tools used for the ICP+RIE and JTE processes are typical for compound semiconductor fabrication and could accommodate devices with areas larger than 1 mm^2. Device size will likely be limited by the uniformity of the GaN substrate itself. Factors like miscut and resultant variability in epitaxial surface morphology can strongly influence device leakage and hence practical device size [22]. Thus, the uniformity and microstructure of the substrate are expected to dictate epitaxial uniformity and thus maximum device size and yield.

V. SUMMARY

Plasma etched-and-regrown GaN diodes grown by MOCVD achieving $R_{on,sp} = 1.1$ mΩ.cm^2, ideality factor of 1.5, and 1610 V breakdown were demonstrated. An RIE step in addition to AZ400K surface treatment greatly reduced reverse leakage of the etched-and-regrown diodes compared to wet chemical treatments alone. It is likely that the RIE step reduced leakage by removing sub-surface defects caused by ICP etching. The etched-and-regrown diodes presented here compare well against the best regrown GaN diodes without etch, which demonstrates that etch-and-regrowth is a viable path for selective area doping for high power GaN electronics.

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