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A Common Drain Operational Amplifier Using Positive Feedback Integrated by Metal-Oxide TFTs

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ABSTRACT This paper presents a common-drain-based operational amplifier (OPAMP) fabricated by mono n-type indium-zinc-oxide (IZO) thin-film transistors (TFTs). Positive feedback technology is employed to the load TFTs by cross-coupled connection in order to boost the voltage gain of the common-drain differential pair. The OPAMP exhibits an open-loop voltage gain (A_v) of 27 dB over a −3 dB bandwidth (BW) of 8.4 kHz at a DC supply voltage of 10 V. The measured unity-gain frequency (UGF), phase margin (PM) and DC power consumption are 119.4 kHz, 36° and 0.96 mW, respectively. Moreover, the chip area of the proposed OPAMP is as small as 0.37 mm × 0.3 mm since this concise topology needs only 10 TFTs.

INDEX TERMS Cross-coupled, common-drain, indium-zinc-oxide (IZO) thin-film transistors (TFTs), positive feedback, operational amplifier (OPAMP).

I. INTRODUCTION

In large-area and flexible electronics, thin-film transistors (TFTs) technology plays an important role in the integration for analog and digital building blocks. Among them, metal-oxide TFTs possess the superiority of decent field-effect mobility, good uniformity coupled with low production cost over other TFT counterparts [1]–[3]. Researchers are pursuing high performance of integrated circuits using metal-oxide TFTs, such as shift register, ring oscillator and amplifier [4]–[6]. The operational amplifiers (OPAMPs) are key fundamental components for many analog and mixed-signal systems, such as DC-DC converter and ADC [7], [8].

Common-source topology is widely adopted to construct the gain stage in operational amplifiers using TFT technologies [7]–[19]. The small signal voltage gain of a common-source amplifier is the product of the equivalent driver transconductance (G_m) and load resistance (R_L). It is worthy to mention that, combining both merits of low temperature polycrystalline silicon (LTPS) TFTs with high on-current and oxide TFTs with low off-current, a CMOS OPAMP with excellent performance is successfully realized by low temperature polycrystalline silicon oxide (LTPO) technology in [19]. Nevertheless, NMOS-only OPAMP design using metal-oxide TFTs is constrained by the absence of available PMOS transistors for integration, thereby a current source load with high output resistance due to poor device mobility [20]. Moreover, the device transconductance is also limited, leading to insufficient intrinsic gain compared with crystalline silicon [21].

Taking frequency response into consideration, it is unreasonable to cascade multiple stages for high gain. Relative works on TFT-based OPAMPs using positive feedback

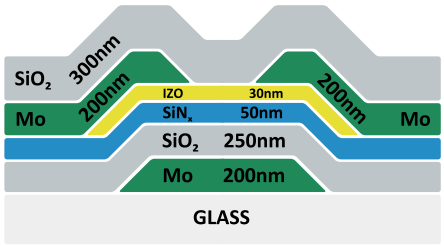

FIGURE 1. Cross-sectional structure of the IZO TFTs.

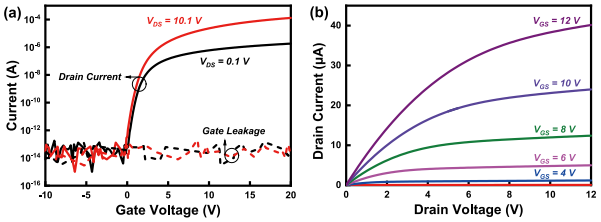

FIGURE 2. Measured (a) transfer characteristics and (b) output characteristics of the fabricated IZO TFT with W/L = 35 μm/7 μm.

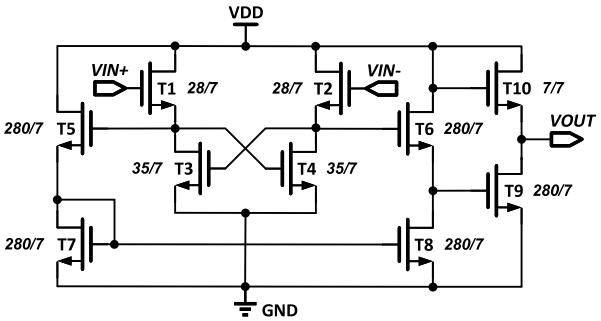

FIGURE 3. Circuit schematic of the proposed OPAMP with positive feedback.

techniques to increase G_m and R_L in common-source amplifiers have been reported [10], [13], [14], [16], [17]. On the one hand, VOUT is proportionally fed back to the gate of the load device, where an active network with a feedback coefficient approaching unity ($A_f \approx 1$) is employed to increase R_L to the order of r_o (the output resistance of a transistor) as well as maintain stability [10], [13]. Besides, a RC high-pass filter can be constructed as an alternative for positive feedback in the amplifier [21]. Cascode structure is implemented to further boost R_L to the order of $g_m r_o^2$ [22]. On the other hand, positive feedback has also been introduced to an operational amplifier with dual-gate-TFTs for transconductance enhancement [14]. In our previous work [17], higher gain exceeds $g_m r_o$ (the intrinsic gain of a transistor) is attained by incorporating both techniques to simultaneously increase G_m and R_L. Although feedback loops are usually added to the common-source differential pair for gain boosting, it will inevitably increase the complexity of circuitry. Considerable chip area is occupied especially when passive RC network with large capacitor is employed. Moreover, multiple stacked devices structure leads to higher supply voltage as well as a loss in voltage headroom of the amplifier.

This paper proposes a new operational amplifier circuit integrated by IZO TFTs. Different from the conventional common-source topology, the amplifier is constructed based on common-drain stage incorporating positive feedback. Negative resistance is introduced to the load of the common-drain differential pair by cross-coupled-connected TFTs. In this way, with a simple topology of 10 TFTs, the open-loop voltage gain of the OPAMP is boosted to the order of the intrinsic gain of a transistor.

II. DEVICE FABRICATION AND CHARACTERISTICS

Fig. 1 shows the back-channel-etch (BCE) structure of the bottom-gate indium-zinc-oxide (IZO) TFTs employed for the proposed OPAMP. A 200-nm layer of molybdenum (Mo) is deposited onto the glass substrate through DC sputtering and patterned by wet etching to form the gate electrode. Successively, 250-nm SiO_2 and 50-nm SiN_x are deposited by plasma-enhanced chemical vapor deposition (PECVD) and patterned as stacked gate insulator (GI) by dry etching. Subsequently, radio frequency (RF) magnetron sputtering and patterning are employed to form a 30-nm IZO active layer. Then the source and drain electrodes are sputtered with Mo and patterned. Finally, a 300-nm SiO_2 layer is fabricated and patterned as the passivation (PV) for device protection under ambient condition.

The transfer characteristics of the IZO TFT with a channel aspect ratio of 35 μm / 7 μm are shown in Fig. 2(a), in which the solid line and the dashed line represent the drain current I_d and the gate leakage current I_g, respectively, while Fig. 2(b) shows the corresponding output characteristics. The field-effect mobility (μ_{FE}) is extracted as 11.2 $cm^2/(V \cdot s)$, while the extracted threshold voltage (V_{TH}) and the subthreshold swing (SS) are 1.9 V and 0.33 V/dec, respectively.

III. CIRCUIT DESIGN AND SIMULATIONS

Fig. 3 reveals the overall schematic of the proposed operational amplifier which comprises only NMOS device. The circuit can be divided into three stages. In the first stage, a common-drain differential pair (T1 and T2) with cross-coupled connected loads (T3 and T4) is adopted to obtain high input impedance and high gain. The second stage composed of T5-T8 is a differential-to-single-ended converter with current mirror as tail current source. In addition, T9 and T10 constitute a common-source amplifier with a diode-connected load and realize a weaker small-signal voltage gain. Meanwhile, the third stage acts as an output buffer with sufficient output voltage swing and lower output impedance for driving loads.

Supposing that all the transistors in the first stage operate in the saturation region and their DC currents are same, the half-circuit of the first stage and its corresponding small-signal model are depicted in Fig. 4(a) and Fig. 4(b), respectively. Fig. 4(c) and Fig. 4(d) provide the transformation of small signal equivalent circuits. Applying Kirchhoff's

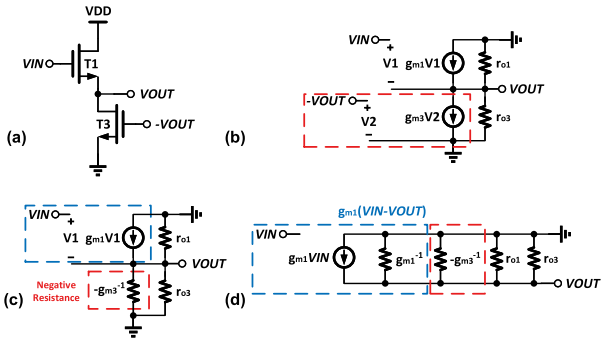

FIGURE 4. (a) Half-circuit of the common-drain stage with cross-coupled-connected load, (b) its small-signal model, (c) the transformation of equivalent negative resistance ($-g_{m3}^{-1}$), and (d) the two components of g_{m1}(VIN-VOUT) in the simplified circuit.

current law (KCL) at VOUT in Fig. 4(b), the small-signal voltage gain of the first stage can be derived as

$$A_{v1} = \frac{g_{m1}}{g_{m1} - g_{m3} + {r_{o1}}^{-1} + {r_{o3}}^{-1}} \tag{1}$$

Corresponding to Fig. 4(d), the gain A_{v1} can be expressed as

$$A_{v1} = g_{m1}\Big[(g_{m1} - g_{m3})^{-1} \| r_{o1} \| r_{o3}\Big] \tag{2}$$

where g_{m1} and g_{m3} represent the transconductances of T1 and T3 while r_{o1} and r_{o3} are their output resistances, respectively. Due to the cross-coupled connection of the load transistor T3 shown in Fig. 4(a), the conductance of T3 ($g_{m3}V2$) in Fig. 4(b) can be replaced by a resistor with negative resistance ($-{g_{m3}}^{-1}$) depicted in Fig. 4(c). And the relationship between $V1$, VIN and $VOUT$ in Fig. 4(c) is

$$V1 = VIN - VOUT \tag{3}$$

As shown in Fig. 4(d), the transconductance term of T1 ($g_{m1}V1$) in Fig. 4(c) can be decomposed into a parallel connection of a current source ($g_{m1}VIN$) and a resistor connected between VOUT and GND ($-g_{m1}VOUT$). Since the opposite direction of the current flow through positive resistor ${g_{m1}}^{-1}$ and negative resistor $-{g_{m3}}^{-1}$, a certain portion of current that flows through ${g_{m1}}^{-1}$ can be equivalently absorbed by the current path of $-{g_{m3}}^{-1}$ by tuning the physical size of T1 and T3. As the transconductance ratio of T3 to T1 (g_{m3}/g_{m1}) approaches unity, the gain in Eq. (1) can be further simplified as

$$A_{v1} = g_{m1}\big(r_{o1} \| r_{o3}\big) \tag{4}$$

It can be found that the transconductance term (g_{m1}) is eliminated by the negative conductance term ($-g_{m3}$) so that the voltage gain is enhanced to the order of the intrinsic gain $g_m r_o$. As there exists a trade-off between sufficient gain and stability, the feedback coefficient g_{m3}/g_{m1} should approach unity for the positive feedback loop.

To convert the differential output signal to a single one, source followers with current mirror loads are employed as the second stage. The duplication of the current through T5 and T7 is reproduced by T8 and summed up with the current from T6. The voltage gain of the second stage is expressed as

$$A_{v2} = g_{m5}\Big({g_{m5}}^{-1} \| r_{o5} \| r_{o7}\Big) \le 1 \tag{5}$$

Due to the finite value of r_o, there exists slight gain attenuation even though a relatively large channel aspect ratio of TFTs is implemented in the second stage. The output stage is a common-source amplifier with diode-connected load. Neglecting the channel length modulation, the voltage gain is dependent on the size ratio of the driver T9 to the load T10, which is given as

$$A_{v3} = g_{m9}\Big({g_{m10}}^{-1} \| r_{o10} \| r_{o9}\Big) \approx \frac{g_{m9}}{g_{m10}} \tag{6}$$

Assuming no gain reduction caused by A_{v2}, the overall small-signal voltage gain of the proposed OPAMP is approximate to

$$A_{v,tot} \approx g_{m1}\Big[(g_{m1} - g_{m3})^{-1} \| r_{o1} \| r_{o3}\Big]\frac{g_{m9}}{g_{m10}} \tag{7}$$

It is hard to obtain abundant gain via the third stage since large area is required for the scaling of device geometries. The total voltage gain is dominated by the first stage. Maximum open-loop voltage gain can be achieved by carefully tuning the channel aspect ratio of T1 and T3. In addition, it can be further improved by employing TFTs with larger channel length attributed to the higher intrinsic gain. Multiple poles exist in the overall OPAMP circuit with one of the dominant poles ω_{p1} located at the output of the first stage. The resistance seen from the output node of the first stage is increased due to the negative resistance. Meanwhile, more equivalent parasitic capacitances are attached in parallel due to the cross-coupled connection, resulting in a relatively large time constant τ. Within the unity-gain frequency, the other dominant pole ω_{p2} at the output terminal of the third stage dramatically moves towards the origin and contributes significant phase lag as it is loaded by large capacitance C_L of ~15 pF. Owing to the total phase lag introduced by these two poles, the potential stability issue of the proposed design must be taken into consideration. For an abundant phase margin, transistors with large channel aspect ratio are applied to move the secondary pole ω_{p3} contributed by the output of differential-to-single-ended converter to a higher frequency [10]. In addition, the right-half-plane (RHP) zero ω_{z1} introduced by the parasitic capacitance of the third stage is located at the order of 10 MHz far beyond the unity-gain frequency.

SPICE simulation is performed to verify and optimize the proposed OPAMP. The optimal dimensions of TFTs are marked in Fig. 3. Fig. 5 displays the simulated frequency response of the proposed OPAMP with the DC supply voltage VDD of 10 V and the load of 15 pF. The low-frequency voltage gain, −3 dB bandwidth, unity-gain frequency and phase margin are simulated as 26.1 dB, 8 kHz, 89.1 kHz and 21°, respectively.

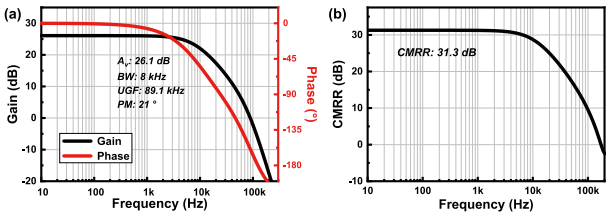

FIGURE 5. Simulated (a) frequency response of the proposed OPAMP with VDD of 10 V and load of 15 pF and (b) common-mode rejection ratio.

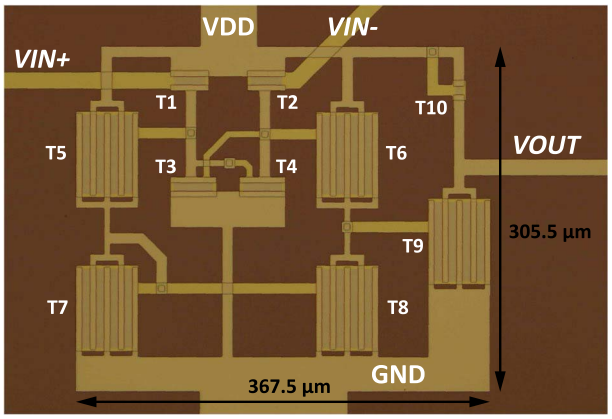

FIGURE 6. Microphotograph of the fabricated operational amplifier.

The theoretical common-mode rejection ratio (CMRR) of the proposed amplifier assuming perfect matching can be derived as

$$\mathrm{CMRR} = \left|\frac{A_{v,\mathrm{DM}}}{A_{v,\mathrm{CM}}}\right| = \frac{A_{v1}\cdot A_{v2}}{\frac{g_{m1}}{g_{m1}+g_{m3}}\cdot\frac{g_{m5}}{g_{m5}+g_{m7}}} \tag{8}$$

where $A_{v,\mathrm{DM}}$ is the differential-mode voltage gain of the proposed OPAMP, and the common-mode voltage gain ($A_{v,\mathrm{CM}}$) of the amplifier is dependent on the transconductances of the driver TFTs (T1 and T5) and the load TFTs (T3 and T7) when neglecting channel length modulation. As shown in Fig. 5(b), the simulated low-frequency CMRR of the proposed OPAMP is 31.3 dB. The common-mode rejection can be improved by employing a tail current source incorporating common-mode feedback (CMFB) technology in the input differential pair of a fully differential OPAMP.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

From the perspective of uniformity and field effect mobility, IZO TFT process with channel length of 7 µm is chosen for circuit integration. And the proposed operational amplifier design has been implemented on glass substrate instead of plastic due to the simpler process as well as lower cost. The optical image of the fabricated OPAMP with TFTs and terminals of the circuit labeled are shown in Fig. 6. The area is measured as 367.5 µm × 305.5 µm. Fingered layout of TFT with large channel aspect ratio is employed to avoid drain current degradation owing to the series resistances [22]. Besides, in a fingered layout TFT, the parasitic capacitance due to the overlap between source / drain and gate electrode

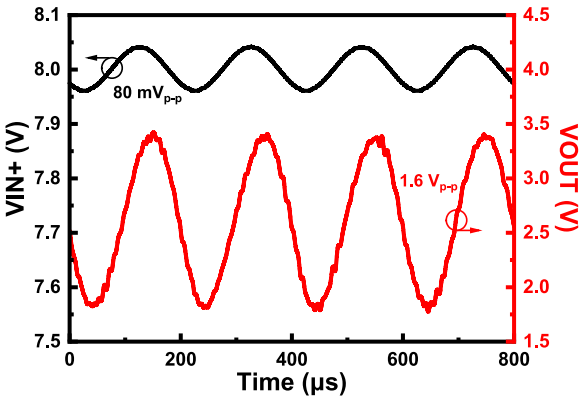

FIGURE 7. Measured transient waveforms of the proposed OPAMP with a 5 kHz sinusoid input (VIN+) of 80 mV_{p-p}.

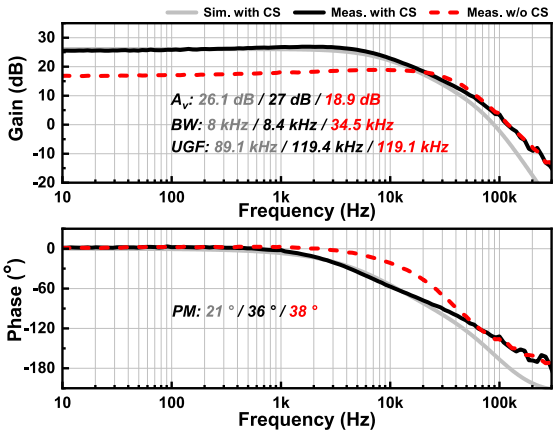

FIGURE 8. Frequency response of the proposed OPAMP and the amplifier (including T1-T8) without common-source (CS) stage (T9 and T10) with 10 V DC supply voltage.

is effectively reduced when compared to direct layout transistor with identical channel aspect ratio. Keeping both design parameters and measurement setup the same, an amplifier without the common-source (CS) output stage has also been fabricated and tested for comparison. The measurement is conducted using an oscilloscope (Agilent DSO-X 4014A), a network analyzer (Keysight E5061B), a signal generator (NF WF1948) and a semiconductor parameter analyzer (Agilent B1500A). Note that, the load introduced by the passive probe can be approximately equivalent to 15 pF‖10 MΩ. The measured time-domain output waveform is plotted in Fig. 7. The supply voltage is 10 V and VIN– is biased at 8 V, while VIN+ is a 5 kHz sinusoidal input of 8 V DC offset and 80 mV_{p-p} (peak to peak voltage). The output voltage is 1.6 V_{p-p} with the corresponding DC power consumption measured as 0.96 mW.

As shown in Fig. 8, the black solid line presents the measured frequency response of the fabricated OPAMP with the corresponding simulation result (the gray solid line) for comparison, while the red dashed line represents the measurement result of the 2-stage amplifier (including T1-T8) without the common-source output stage (T9 and T10).

TABLE 1. Comparison with state-of-the-art operational amplifiers integrated by thin film transistors.

Circuit Design	[11]	[7]	[18]	[12]	[13]	[14]	[17]	This Work	[10]	[19]
TFT Tech.	Metal-Oxide								a-Si	LTPO
	IGZO						IZO			
Topology	Diode-connected NMOS			Pseudo-CMOS	Positive Feedback					CMOS
No. of TFTs	16	18	19	13	16	22	16	**10**	14	13
VDD (V)	5	±15	±10	5	6	±10	15	**10**	25	±20
A_v (dB)	18.7	24.5	19.6	22.5	19	30	29.54	**27**	42.5	50.7
BW (kHz)	108	6	350	5.6	25	0.15	9.33	**8.4**	2	200
GBWP (kHz)	930	101.9	3342	74.7	223	4.74	279.9	**188**	267	68500
UGF (kHz)	472	32	1600	31	330	5.5	180.2	**119.4**	30	7000
PM (°)	≈ -10*	≈ -10*	102	≈ 20*	70	NA	21.5	**36**	NA	92
P_{DC} (mW)	0.9	NA	51	0.16	6.78	0.19	5.07	**0.96**	3.55	0.6
Area (mm^2)	2.6 × 0.8	1.35 × 0.95	0.5 × 1.4	2.52 × 3.9	4.2 × 6	≈ 1.1 × 1*	1.3 × 0.85	**0.37 × 0.3**	3.4 × 1.5	0.25 × 0.27

* Extracted from measured results

Compared with the 2-stage amplifier, the open-loop voltage gain of the proposed OPAMP is increased by 8.1 dB at the expense of −3 dB bandwidth. The gain-bandwidth product (GBWP) of the proposed OPAMP is calculated as 188 kHz. The measured phase margin is 36° without frequency compensation. It is obvious that the unity-gain frequencies and phase margins of both amplifiers remain approximately the same. The measured gain and –3 dB bandwidth are relatively consistent with the simulated results. However, the unity-gain frequency and phase margin of the measured results are higher, which is perhaps owing to the deviation of the parasitic parameters between the layout and the simulation.

Table 1 summarizes the performance of the proposed OPAMP and provides a comparison with state-of-the-art counterparts using different TFT technologies. IGZO TFTs are considered to be a popular choice for metal oxide TFT OPAMP circuit integration while IZO TFTs are employed in [17]. The open-loop gain of the proposed OPAMP is higher than those of the designs based on NMOS diode and pseudo-CMOS topologies while comparable to those reported in [14] and [17]. Higher gain of the differential-ended OPAMP is achieved without gain attenuation caused by a differential-to-single-ended converter in [14]. Compared with [17], lower power consumption as well as better stability attributed to higher phase margin are achieved in the proposed design, whereas the gain and bandwidth are slightly smaller. Nonetheless, the phase margin is smaller compared with the designs in [13] and [18]. In closed-loop applications, a minimum phase margin of 45° is appropriate for an OPAMP to compromise between stability and transient response. Compensation techniques should be introduced for sufficient PM. Miller compensation is a promising method to separate poles and thus increase PM at the cost of −3 dB bandwidth. Moreover, optimizing parasitic parameters in the layout and compensating threshold voltage variations of the TFTs are beneficial to the frequency response of OPAMP [13].

It is noteworthy that, unlike those common-source-based designs in the previous works, the proposed OPAMP is mainly constructed by a common-drain stage for amplification. Thus only 10 TFTs are used which is almost half of those in [14] and [18], resulting in the smallest area among mono-NMOS designs. As consequence, positive feedback is successfully introduced to the common-drain-based operational amplifier by cross-coupled-connected loads of the first stage.

V. CONCLUSION

An operational amplifier based on common-drain topology with positive feedback is designed and implemented by IZO TFTs. In particular, the proposed OPAMP consists of a differential common-drain stage as the dominant gain stage, a differential-to-single-ended converter and a common-source stage. Negative resistance is obtained by cross-coupled connection of load TFTs, and thus boost the gain of the common-drain input stage. The measured open-loop voltage gain of the proposed OPAMP is 27 dB. The −3 dB bandwidth, unity-gain frequency and DC power consumption are measured as 8.4 kHz, 119.4 kHz and 0.96 mW, respectively. The new design requires only 10 transistors with a minimum area among all the designs using metal-oxide TFTs as far as we know. As a result, the proposed design provides a promising solution to low-cost OPAMP with open-loop voltage gain that approaches the intrinsic gain of metal-oxide TFTs.

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