Received 30 December 2020; revised 3 February 2021; accepted 8 February 2021. Date of publication 17 February 2021; date of current version 4 March 2021.
The review of this article was arranged by Editor M. Chan.

Digital Object Identifier 10.1109/JEDS.2021.3059854

A Zero-Cost Technique to Improve ON-State Performance and Reliability of Power LDMOS Transistors

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This work was supported in part by the Department of Science and Technology (Government of India) through their Technology Development Program and in part by the Indian Space Research Organization through their RESPOND program. The work of Nihar R. Mohapatra was supported by the Visvesvaraya Ph.D. Scheme, MeitY, Government of India.

ABSTRACT In this paper, we have proposed a simple and zero-cost technique to improve ON-state and reliability performance of LDMOS transistors. We introduced doping gradient in the channel by optimizing position of the P-Well mask during test structure design/layout. Through proper device design, fabrication and measurement on different test structures, we have shown that the graded channel significantly improves the drive capability (upto ~30%), analog FoMs and hot-carrier reliability of LDMOS transistors without any penalty on the OFF-state performance. The performance improvement is independent of drift region design (breakdown voltage). The device physics behind different observations is also discussed with detailed TCAD simulations.

INDEX TERMS PMIC, LDMOS, doping gradient, breakdown voltage, specific on-resistance, trans-conductance, output conductance, electron velocity, hot carrier reliability.

I. INTRODUCTION

The Power Management Integrated circuits (PMICs) have witnessed a tremendous growth in recent years because of growing interest in Internet of Things (IoTs), System-on-Chips (SoCs), Electric Vehicles (EVs) and green energy solutions. The BCDMOS (Bipolar-CMOS-DMOS) process is typically used for fabricating these PMICs [1]–[4]. The Lateral Diffused MOS (LDMOS) transistor is heart of any BCDMOS process. These LDMOS transistors can withstand high voltage while at OFF state and can provide low drain to source resistance (R_{on}) during ON state. In many cases, the PMICs are required to deliver power to a load efficiently. A key factor in improving the power efficiency of PMICs is to deliver current with lowest possible ON-resistance [5], [6]. Further, drive strength of the LDMOS transistors need to be higher to reduce its size (overall chip area), associated capacitance, switching losses and to increase robustness of PMICs to load/line transients. The LDMOS transistors in PMICs should also have optimum trans-conductance (g_m) and output conductance (g_{ds}) in order to have proper regulation and faster analog control. Further, the high operating voltage of LDMOS transistors make them susceptible to hot carrier degradation. The carriers flowing inside the device get accelerated by high internal electric field, undergo impact ionization, get injected onto the oxide, generate defects by breaking bonds and change the device electrical behavior [7], [8]. The LDMOS transistors in PMICs should be immune to this phenomena. So, in a nutshell, the LDMOS transistors are expected to provide high off-state breakdown voltage ($BV_{DS,off}$, 1.5-2X of the operating voltage) at low specific on-resistance ($R_{sp} = R_{on}$ x device pitch), optimum g_m, g_{ds} and stronger hot carrier immunity.

Typically, drift region doping (N_{drift}), length (L_D) and thickness (t_D) are engineered to set ON- and OFF-state breakdown voltages ($BV_{DS,on}$ and $BV_{DS,off}$) and R_{on}. Note that, the simultaneous optimization of $BV_{DS,off}$ and R_{on} is always tricky. A range of techniques have been proposed/discussed in literature and used by industries to improve the $BV_{DS,off} - R_{on}$ performance of LDMOS transistors. The reduced surface field (ReSURF) [9]–[13] and field plate techniques [14]–[16] have focused on R_{sp} reduction without varying the $BV_{DS,off}$, whereas the gate engineering

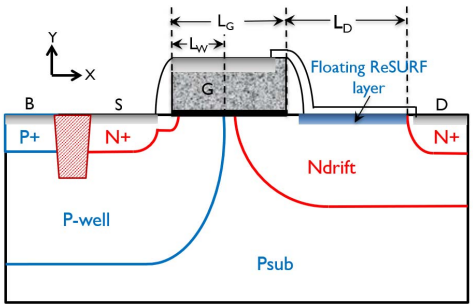

FIGURE 1. Schematic representation of the nLDMOS transistor used in this study. The overlap between gate and P-Well mask (L_W) is varied from 0.2 to 0.4 μm to have transistors with different channel doping profiles. The other processing steps are same. The thickness, doping of the drift region and the ReSURF implant are optimized to set the $BV_{DS,\,on}$ and $BV_{DS,\,off}$ of the transistor.

techniques (split gate architecture, gate work-function engineering etc.) have mainly focused on improving the on-state performance of LDMOS transistors [17]–[19]. However, most of these techniques involve extra process steps and complex device architectures thereby increasing process integration complexity and cost.

The graded channel concept (with a doping gradient from source to drain) has been tried in MOS transistors to improve device performance (ON current, switching speed) and hot-carrier reliability [20], [21]. The channel doping gradient is realised by tilted ion implantation (an additional process step) from the source side. This makes the device asymmetric, thus forcing all the transistors to be aligned during circuit layout (all Sources in one side and Drains in other side). This is a major bottleneck in designing high performance area efficient circuits. However, the LDMOS transistors are inherently asymmetric. Therefore, graded channel technique could be used to improve the device performance without any issue. Few research groups have demonstrated improved LDMOS transistors with graded channel doping [22]. But, most of these works have used additional process steps.

In this work, the P-Well mask is used to introduce graded channel in LDMOS transistors (done without any cost addition). The position of the P-Well mask with respect to Gate mask is varied to introduce different levels of doping gradient, which helped to improve R_{on}, I_{on} and g_m without degrading device OFF-state performance and device hot carrier reliability. The effect of doping gradient on device performance is systematically investigated through measurements on properly designed test structures and on multiple dies. It is shown that the transistor ON-state performance can be improved by ~30% by proper optimization of doping gradient. The device physics behind this observation is discussed in detail using TCAD simulations. Although this manuscript has focused on nLDMOS transistors, similar improvement has also been observed for pLDMOS transistors. However, the pLDMOS transistor data is not included in this paper because of lack of space.

This paper is organized as follows. The device and measurement details are discussed in Section II. The DC performance and analog/RF performance improvement with channel doping gradient is discussed in Sections III-A and III-B respectively. The hot carrier reliability with channel doping gradient is discussed in Section III-C. The device physics behind different observations is also discussed in Section III followed by conclusion in Section IV.

TABLE 1. Device dimensions used in this work.

Devices	L_G(μm)	L_D(μm)	L_W(μm)	Ndrift
D1	0.6	0.7	0.4	N_{drift1}, N_{drift2}, N_{drift3}
D2	0.6	0.7	0.3	N_{drift1}, N_{drift2}, N_{drift3}
D3	0.6	0.7	0.2	N_{drift1}, N_{drift2}, N_{drift3}
D4	0.45	0.7	0.2	N_{drift1}, N_{drift2}, N_{drift3}

II. DEVICE DETAILS

The transistors used in this work are fabricated using a well qualified CMOS process. The nLDMOS transistors are integrated into the CMOS process by adding one (non-critical) mask and few implants to form the Ndrift region. Fig. 1 shows schematic cross-section of the nLDMOS transistor. The channel region is implanted before gate stack formation using the P-Well mask. The test structures with different channel doping gradients are created by varying the overlap between the P-well mask and gate mask (L_W). Table 1 summarizes the device dimensions used in the study. The transistors D1, D2 and D3 have gate/drift-region length (L_G/L_D) of 0.6/0.7 μm but different L_W (different channel doping gradient). Note that the minimum L_W is limited by P-Well mask overlay error. L_W very close to the mask overlay specification results in device variability issues. In this work, the L_W is limited to 0.2μm. The transistors D3 and D4 have same L_D/L_W but different L_G. All these devices are fabricated with 3 different drift dopings (N_{drift1}, N_{drift2} and N_{drift3}). All transistors have an oxide thickness of ~7nm and support a maximum gate voltage (V_{GS}) of 3.3V.

The TCAD process suite Sentaurus [23] comprising of process and device simulation capabilities is used in this work to verify the device physics behind different observations. Several improved diffusion models are implemented in the process simulator to have the correct doping profiles. Fig. 2 shows 1D cut-line from 2D simulated doping profile along the channel for D1, D2 and D3. As shown, the channel doping gradient increases with decrease in L_W. Note that the doping gradient could be further increased by increasing channel doping for a particular L_W. For electrical simulations, hydrodynamic carrier transport model is used. Electron and hole impact ionization (II) are modeled using van Overstraeten-de Man model. ShockleyReadHall and Auger recombination models are included to account for carrier generation recombination. In addition, the bandgap narrowing model for silicon, doping-dependent Masetti mobility model, Lombardi surface mobility degradation model at silicon-oxide interfaces and high-field mobility saturation models are switched ON. Fig. 3 shows the measured and simulated transfer and output characteristics for LDMOS transistors D1, D2 and D3. As shown, the simulated characteristics are

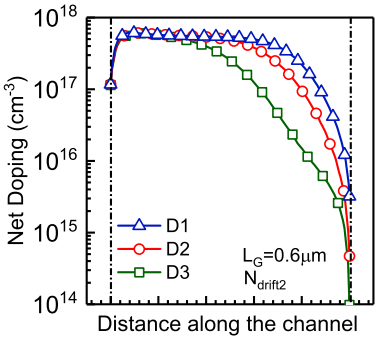

FIGURE 2. 1D cut-line from simulated 2D doping profile along the channel for transistors with different L_W. The doping profile is taken 10nm below the Si-SiO_2 interface. The higher channel doping gradient is clearly observed for transistors with lower L_W (D3).

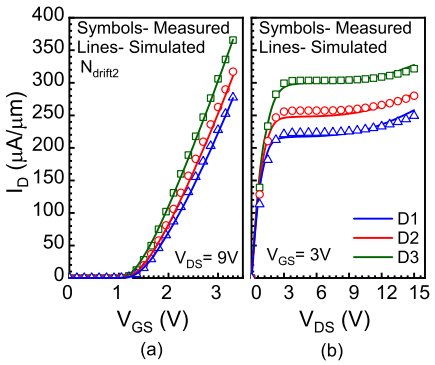

FIGURE 3. Measured (symbols) and simulated (lines) (a) transfer characteristics at V_{DS} = 9V and (b) output characteristics at V_{GS} = 3V for transistors D1, D2, and D3. TCAD simulations are accurately calibrated with experimentally measured data.

in good agreement with the measured data. This calibrated deck is used to extract parameters like electric field and electron velocity in the channel.

III. RESULTS AND DISCUSSION

The results presented in this section are from the devices fabricated with the same process flow. The transistors from same die and same wafer are used to study the effect of doping gradient on device performance and hot carrier reliability. The transistors from different wafers are used to study the effect of drift region doping (N_{drift}) on relative device performance improvement due to doping gradient. Note that the transistors with N_{drift2} are used throughout the analysis unless specified. All measurements are performed on 13 different dies across the wafer. The $V_{th,lin}$ and $V_{th,sat}$ are extracted using constant current method at drain to source voltages (V_{DS}) of 100mV and 15V respectively. The I_{on} is measured at V_{GS} of 3.3V and V_{DS} of 15V. The R_{on} is extracted at V_{GS} of 3.3V and V_{DS} of 100mV. The $BV_{DS,off}$ is extracted at V_{GS}/I_D of 0V/100pA/μm. The Keysight's B1500 is used to perform DC and reliability measurements, while accurately calibrated TCAD simulations are used to understand the device physics behind the observations.

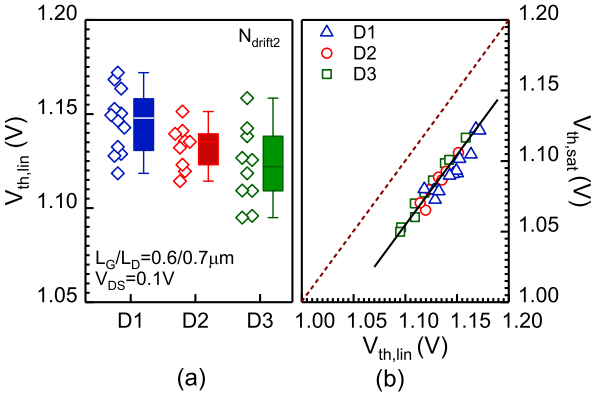

FIGURE 4. Experimentally measured (a) $V_{th,\ lin}$ and (b) $V_{th,\ lin}$-$V_{th,\ sat}$ characteristics for a 0.6μm long nLDMOS transistor with different channel doping gradients. The data is extracted from 13 different dies across the wafer. $V_{th,\ lin}$ and $V_{th,\ sat}$ reduces slightly with decrease in L_W because of reduction in average channel doping.

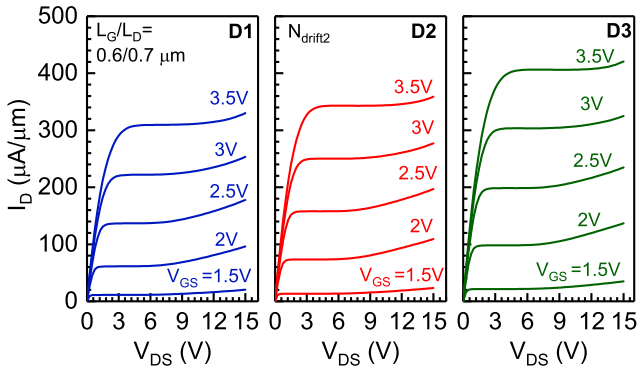

FIGURE 5. Experimentally measured output characteristics for devices D1, D2 and D3. Improvement in current with reduction in L_W (increase in channel doping gradient) can be clearly observed.

A. DC PERFORMANCE

Figs. 4(a) and 4(b) show the measured $V_{th,lin}$ and $V_{th,lin}$-$V_{th,sat}$ characteristics for D1, D2 and D3. As shown, $V_{th,lin}$ decreases with increase in the doping gradient because of reduction in average channel doping (refer Fig. 2). However, the $V_{th,lin}$ difference is very less (D3 has ~25mV less $V_{th,lin}$ compared to D1). The $V_{th,sat}$ is ~50mV lower than $V_{th,lin}$ for all the transistors thus implying that the doping gradient does not have any effect on the DIBL of transistors.

Fig. 5 shows the output characteristics of D1, D2 and D3. The characteristics clearly show the absence of quasi-saturation, velocity saturation (in channel and drift regions) and high output impedance for all the transistors. Fig. 6a shows the extracted R_{on} as a function $V_{th,lin}$ for D1, D2 and D3. Fig. 6b shows the extracted I_{on} as a function $V_{th,sat}$ for D1, D2 and D3. As shown, R_{on} reduces by ~11% (at same $V_{th,lin}$) and I_{on} improves by ~30% (at same $V_{th,sat}$) with increase in the doping gradient. This is a significant improvement and is achieved without any changes to the drift region.

Moreover, the LDMOS transistors are used as switches in PMICs like voltage regulators and DC-DC converters. The

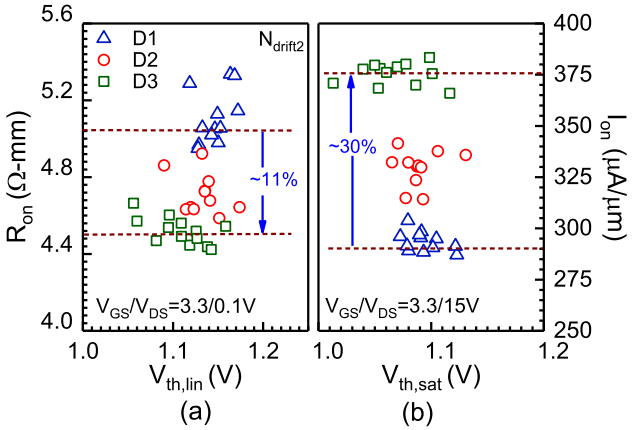

FIGURE 6. Experimentally measured, (a) R_{on} as a function of $V_{th,\,lin}$ and (b) I_{on} as a function of $V_{th,\,sat}$ for D1, D2 and D3. Significant improvement in R_{on} and I_{on} is observed for transistors with higher doping gradient.

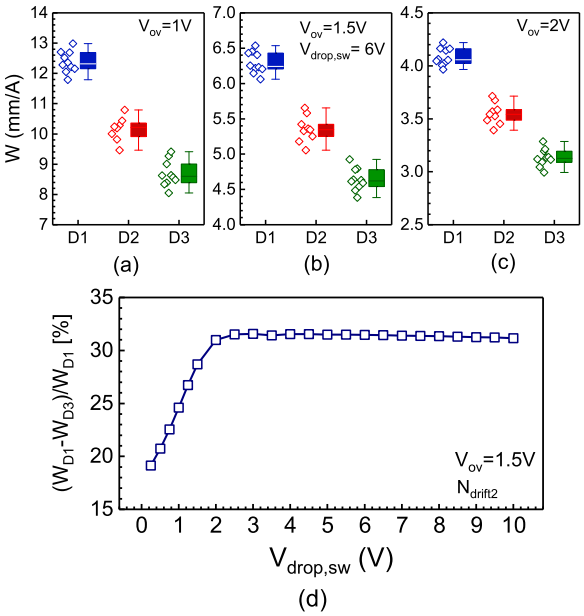

FIGURE 7. (a)-(c) Width required to deliver 1A load current for transistors D1, D2, D3 at different gate overdrive voltages (V_{ov}). The voltage drop across the transistor is set at 6V during this measurement. (d) Percentage reduction in width for delivering a particular load current as a function of voltage drop across the transistor. The transistors with higher doping gradient could deliver a particular load current at ~20-30% lower area.

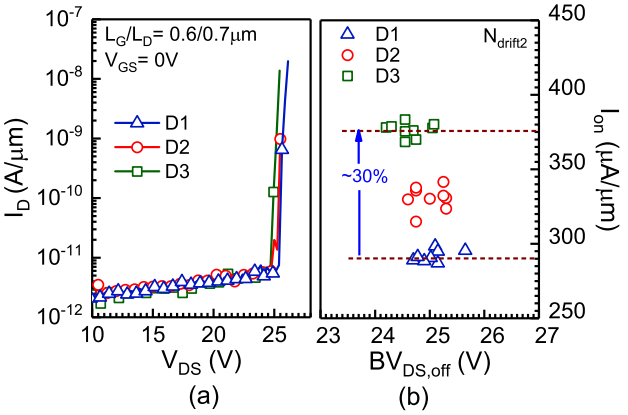

FIGURE 8. (a) Breakdown characteristics of transistors D1, D2 and D3. The $BV_{DS,\,off}$ is extracted at I_D of 100pA/μm. (b) Measured I_{on} as a function of $BV_{DS,\,off}$ for D1, D2 and D3. Significant improvement in I_{on} at same $BV_{DS,\,off}$ is observed for transistors with higher doping gradient.

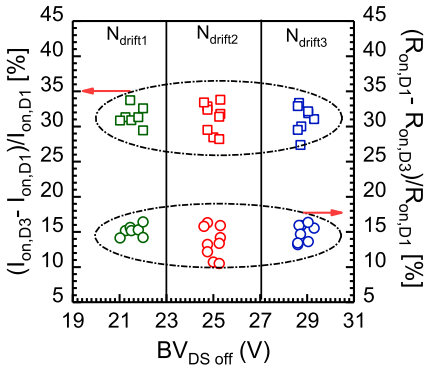

FIGURE 9. Improvement in I_{on} and R_{on} due to doping gradient for transistors with different Ndrift (N_{drift1} > N_{drift2} > N_{drift3}). The $BV_{DS,\,off}$ varies with the drift region doping but the relative improvement in I_{on} and R_{on} due to doping gradient is same.

area of the switches depends on the maximum load current rating of these circuits. These switches are always expected to deliver more current per unit width in order to facilitate lower input capacitance, lower switching losses, low switch mode spikes/ringing and lower circuit area. Figs. 7a–c plot the width required per ampere current for D1, D2 and D3 at different overdrive voltages ($V_{ov} = V_{GS} - V_{th}$). The voltage drop across the switch ($V_{drop,sw}$) is set at 6V. As shown, the transistor D3 is able to deliver 1A current at ~30% lower width compared to D1 at all V_{ov}s. This improvement reduces to ~20% for lower $V_{drop,sw}$ (Fig. 7d). So, the transistors with higher doping gradient can service the same load at 20-30% lower width. This will improve the transient behavior of the circuits significantly. Further, since the blocking voltage of the switch ($BV_{DS,off}$) is mainly limited by the impact ionization at the gate edge and depends solely on the drift region doping/drift length, it is independent of doping gradient as shown in Fig. 8a. Fig. 8b shows I_{on} as a function of $BV_{DS,off}$ for D1, D2 and D3. As shown, the LDMOS transistors (power switches) with high drive capability and higher SOA can be designed without degrading their voltage blocking capability.

As mentioned in Section II, the doping gradient in the channel is created by selective implantation of the channel region (using the P-Well mask) and dopant diffusion during subsequent annealing steps. Therefore, with change in the channel doping profile, there will be some changes in the drift region doping profile. To examine the effect of this change (mainly at the channel-drift region junction) on the device performance, we have measured transistors with different drift region doping (N_{drift1}, N_{drift2} and N_{drift3}). Fig. 9 shows the improvement in I_{on} and R_{on} due to doping gradient for transistors with different N_{drift}

TABLE 2. Performance of LDMOS transistors for different channel doping gradient and drift region doping.

Devices	Ndrift	$BV_{DS,off}$(V)	R_{on}(Ω-mm)	R_{sp} (mΩ-mm^2)
D1	N_{drift1}	21.53	4.9	10.192
	N_{drift2}	25.06	5.06	10.525
	N_{drift3}	28.80	5.22	10.858
D2	N_{drift1}	21.50	4.53	9.422
	N_{drift2}	25.00	4.68	9.734
	N_{drift3}	28.70	4.82	10.026
D3	N_{drift1}	21.42	4.39	9.131
	N_{drift2}	24.55	4.53	9.422
	N_{drift3}	28.65	4.67	9.714
D4	N_{drift1}	21.70	4.08	7.797
	N_{drift2}	25.00	4.21	8.125
	N_{drift3}	29.10	4.35	8.396

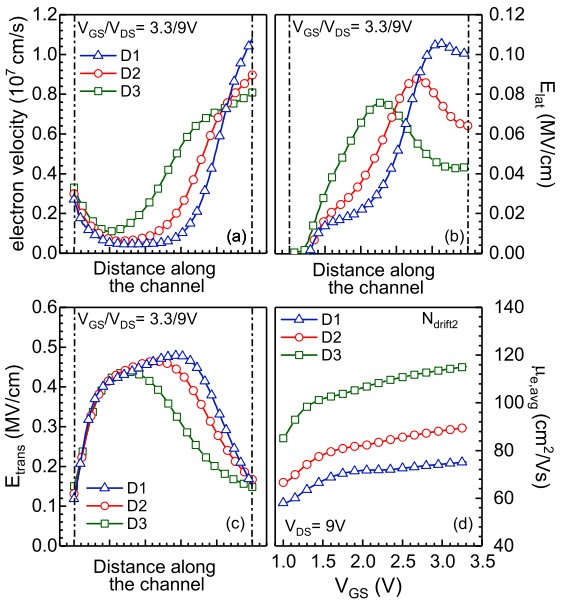

FIGURE 10. Simulated (a) electron velocity, (b) lateral electric field (E_{lat}), (c) transverse electric field (E_{trans}) along the channel for transistors D1, D2 and D3. The cross-section is taken 10nm below the Si-SiO_2 interface. (d) Average electron mobility ($\mu_{e,avg}$) in the channel as a function of V_{GS}. The improved I_D for D3 can be attributed to higher electron velocity in most part of the channel.

(N_{drift1}>N_{drift2}>N_{drift3}). Table 2 summarizes $BV_{DS,off}$, R_{on} and R_{sp} (R_{on} X Device pitch) for different N_{drift} for D1, D2, D3 and D4. As expected, the $BV_{DS,off}$ varies with change in drift region doping. However, the relative improvement in I_{on}, R_{on} and R_{sp} with the doping gradient is still the same. This confirms that the improvement in device performance is solely due to the channel doping gradient.

Detailed TCAD simulations are then carried out to find the exact physics behind the improvement in device performance with doping gradient. Figs. 10a, 10b, and 10c show the simulated electron velocity, lateral electric field (E_{lat}) and transverse electric field (E_{trans}) along the channel for D1, D2 and D3. As shown, for transistors with higher gradient (i.e., D3), E_{lat} is higher at source side of the channel whereas E_{trans} is lower at drain side of the channel. The higher E_{lat} (at source side) results in faster acceleration of injected electrons leading to higher electron velocity in the channel. The lower

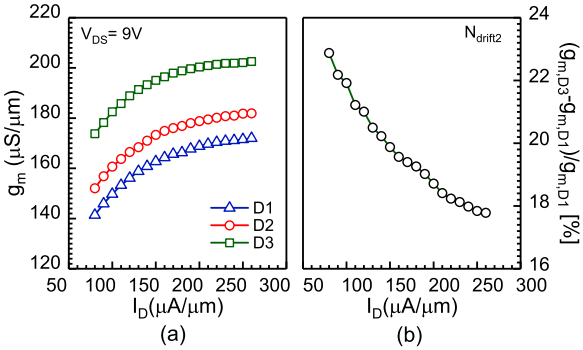

FIGURE 11. (a) g_m as a function of I_D for transistors D1, D2 and D3. (b) the relative improvement in g_m of D3 compared to D1 as a function of I_D. The g_m improves with doping gradient because of higher carrier velocity and this improvement reduces with increase in I_D.

E_{trans} in most part of the channel for D3 reduces scattering thus resulting in improved device characteristics. Overall, the increased E_{lat} at the source end and lower average E_{trans} in the channel is responsible for higher mobility of electrons in the channel as shown in Fig. 10d and higher current.

B. ANALOG/RF PERFORMANCE

The device parameters such as g_m, trans-conductance generation efficiency (g_m/I_D) and transit frequency (g_m/C_{gs}) are very important for overall transient performance and stability of voltage regulators and DC-DC converters. All these parameters are extracted from the transfer and output characteristics measured at different drive current (I_D) on transistors operating in the saturation region (V_{DS} = 9V).

Fig. 11a shows g_m as a function of I_D for D1, D2 and D3. Note that at same I_D, the V_{ov} for D3 is less compared to that of D1 (refer Fig. 5). This means the source to channel barrier (ϕ_{sc}) for D3 is higher than D1 (at same I_D). But still, the g_m for D3 is ~20% higher (at I_D of 150μA/μm) compared to D1 and this is primarily due to increase in the electron mobility because of the channel doping gradient. Since the V_{ov} difference (between D1 and D3) increases with increase in I_D, the improvement in g_m reduces with increase in the drive current as shown in Fig. 11b.

Fig. 12 shows g_m/I_D as a function of I_D for D1 and D3. As expected, D3 shows ~20% improvement in g_m/I_D (at I_D = 150μA/μm) compared to D1. The higher trans-conductance generation efficiency in D3 can be exploited to build high performance PMICs.

We have also measured the gate-source capacitance (C_{gs}) as function of I_D to predict the RF performance of transistors with doping gradient. The transit frequency indicator (g_m/C_{gs}) is plotted as a function of I_D in Fig. 13. As shown, D3 has higher transit frequency at all I_Ds.

C. HOT CARRIER RELIABILITY

The LDMOS transistors are more sensitive to hot carrier (HC) degradation because of higher operating V_{DS}. Fig. 14 shows the E_{lat}, II and E_{trans} along the horizontal cut-line

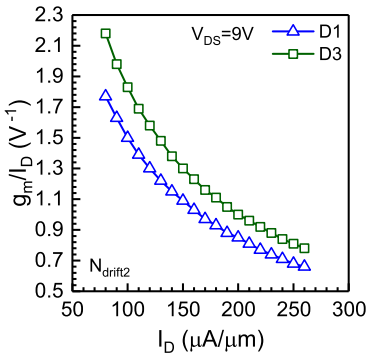

FIGURE 12. g_m/I_D as a function of I_D for transistors D1 and D3. The transistor with higher doping gradient has higher g_m/I_D.

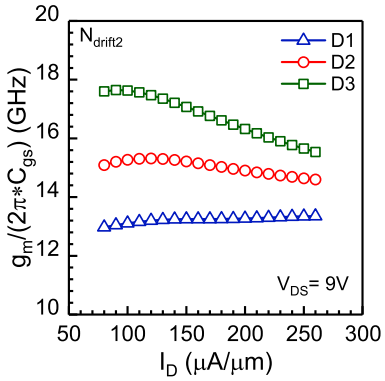

FIGURE 13. g_m/C_{gs} as a function of I_D for transistors D1, D2 and D3. Higher g_m for transistor with higher channel doping gradient improves g_m/C_{gs} (cutoff frequency) at all drive currents.

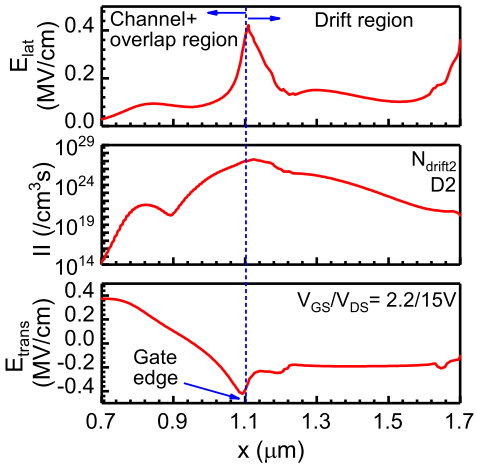

FIGURE 14. Simulated E_{lat}, impact ionization rate (II) and E_{trans} along the channel for transistor D2. The cross-section is taken 10nm below the Si-SiO_2 interface. The E_{lat} and II peaks at the drain side gate edge. The negative E_{trans} near the drain side gate edge favours hot hole injection into the drift region spacer creating acceptor type traps thus degrading the device parameters.

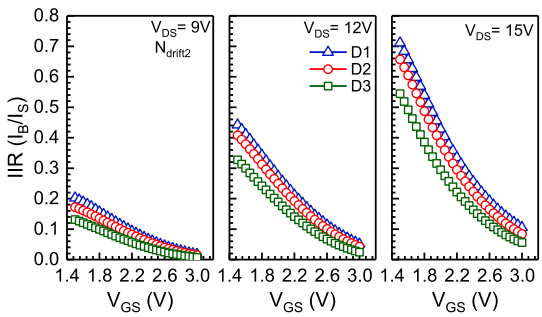

FIGURE 15. The impact ionization rate (IIR) as a function of V_{GS} for D1, D2 and D3. The data is presented for 3 different V_{DS}. The transistor with higher channel doping gradient have less IIR.

near Si-SiO_2 interface (along the channel and drift region) of a LDMOS transistor. The hot carriers are generated due to acceleration of injected carriers (from source) by E_{lat}. These carriers undergo impact ionization (II) and generate electron-hole pairs. As shown in Fig. 14, the E_{lat} and II is maximum at drain side gate edge. The II generated holes are collected by the substrate contact (substrate current, I_B). The II generated electrons are collected at drain contact along with the injected electrons from source. Further, with a negative E_{trans} (bottom to top) near the drain side gate edge, some of these II generated holes are injected into the drift region spacer creating acceptor type traps [24]. These created traps are later filled by electrons. These negatively charged traps (after being filled by electrons) deplete the drift region below spacer, which results in degradation of the R_{on} and g_m.

The hot carrier reliability of LDMOS transistors with different channel doping gradient is evaluated by performing constant bias stress experiments at room temperature. During this hot carrier stress, the device parameters such as R_{on} and $g_{m,max}$ (maximum g_m at $V_{DS} = 0.1V$) are monitored at logarithmic stress intervals (four times per decade). Fig. 15 shows the impact ionization rate, IIR (number of holes generated per one injected electron, I_B/I_S) as a function of V_{GS} for D1, D2 and D3. The data is presented for V_{DS} of 9V, 12V and 15V. Note that the drift region-channel junction is more graded for transistors with higher channel doping gradient. Therefore, the IIR (at constant V_{GS} and V_{DS}) is less for D3. Figs. 16a and 16b shows the time evolution of HC induced R_{on} and $g_{m,max}$ degradation for D1, D2 and D3. The HC stress was performed at a bias condition corresponding to maximum II ($V_{GS,stress} = 2.2V$, $V_{DS,stress} = 15V$). The transistor D3 exhibits less HC degradation due to lower IIR and the same is observed for different stress bias conditions (as shown in Fig. 17). The HC degradation in LDMOS transistors also follows a simple power law and can be fitted into straight line (refer Fig. 16).

Note that at the same stress bias, the transistors with higher channel doping gradient (i.e., D3) have higher drive current because of higher carrier velocity. Therefore, the HC induced degradation for different channel doping gradient should be done at the same stress current. Fig. 18 shows R_{on} and $g_{m,max}$ degradation as a function of stress current ($I_{D,stress}$) for D1, D2 and D3. As shown, the HC induced degradation increases with reduction in $I_{D,stress}$. This is due to higher E_{lat} at drain side gate edge because of lower V_{GS}.

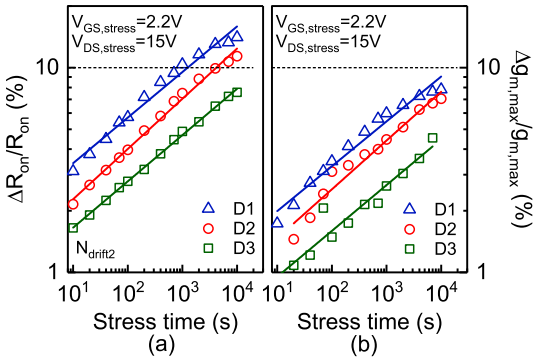

FIGURE 16. Time evolution of (a) R_{on} and (b) $g_{m,max}$ degradation under hot carrier stress for D1, D2 and D3. The transistors with higher channel doping gradient exhibits lower HC degradation.

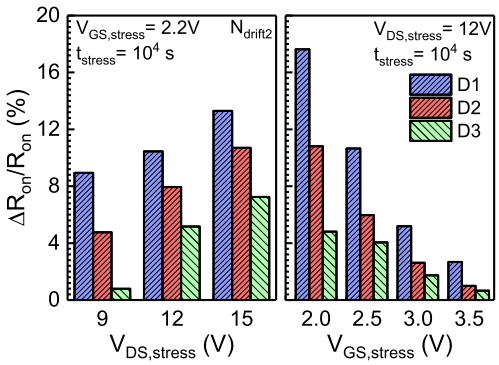

FIGURE 17. HC induced R_{on} degradation for different stress bias conditions for D1, D2 and D3. The transistors with higher channel doping gradient exhibits lower HC degradation for all stress biases.

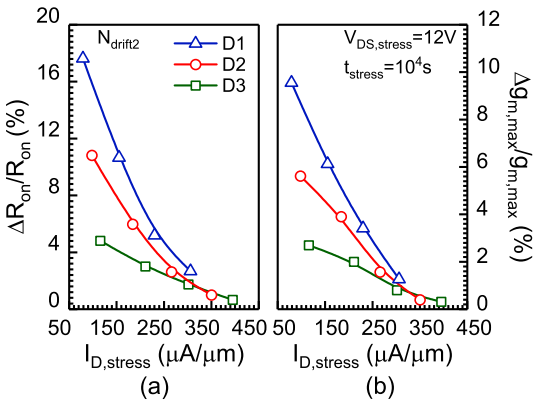

FIGURE 18. HC induced (a) R_{on} and (b) $g_{m,max}$ degradation as a function of stress current for D1, D2 and D3. At same stress current, the transistors with higher channel doping gradient exhibits lesser HC degradation.

The HC induced degradation is lower for D3 compared to D1, D2. For example, at 150μA/μm $I_{D,stress}$, D3 has ~3X lower degradation compared to D1.

Overall, it is observed that the channel doping gradient improves important device FoMs like R_{on}, I_{on}, g_m, g_m/I_D and also improves the HC reliability. Fig. 19 plots the HC induced R_{on} degradation as a function of R_{sp} for different transistors. Both of these parameters are very important in

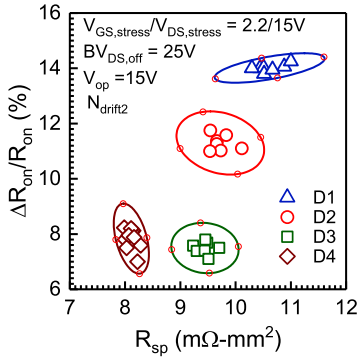

FIGURE 19. The HC induced R_{on} degradation as a function of specific on-resistance (R_{sp}) for different transistors. The device with $L_G/L_W/L_D$ of 0.45/0.2/0.7μm exhibits record R_{sp} with much improved HC reliability.

PMICs. The increase in I_D with increase in channel doping gradient results in reduction of R_{sp}. The lower IIR with increase in channel doping gradient results in reduction of HC induced degradation. The reduction of L_G further reduces R_{sp} (due to pitch reduction) without affecting the device reliability. Note that the R_{sp} value of 8.2mΩ-mm^2 (at $BV_{DS,off}$ of 25V) for the transistor with $L_G/L_W/L_D$ of 0.45/0.2/0.7μm is successfully demonstrated. The R_{sp} is measured at a V_{GS} of 3.3V. This is according to our knowledge, one of the best figures published till date.

IV. CONCLUSION

In this work, we proposed a zero-cost technique to improve the critical parameters of LDMOS transistors. We introduced channel doping gradient by optimizing the P-Well mask position during layout. Through elaborate measurement on multiple transistors across multiple dies, we showed that the LDMOS transistor drive strength could be significantly increased by this method. We demonstrated R_{sp} value of 8.2mΩ-mm^2 at a $BV_{DS,off}$ value of 25V. Through long term reliability measurements, we also demonstrated that the process to improve the device performance also improves long term reliability thus SOA. The device physics behind these observations were discussed through detailed TCAD simulations. The results presented in this work indicates the potential of channel doping gradient in power LDMOS devices for efficient PMICs.

ACKNOWLEDGMENT

The authors would like to thank Semiconductor Laboratory (SCL, Department of Space, Government of India) for their support in device fabrication.

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