Received November 30, 2020; revised January 28, 2021 and February 4, 2021; accepted February 8, 2021. Date of publication 11 February 2021; date of current version 3 March 2021. The review of this article was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2021.3058662

2.3 kV 4H-SiC Planar-Gate Accumulation Channel Power JBSFETs: Analysis of Experimental Data

ADITI AGARWAL (Graduate Student Member, IEEE), AND B. J. BALIGA (Life Fellow, IEEE)

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA

CORRESPONDING AUTHOR: A. AGARWAL (e-mail: aagarw12@ncsu.edu)

ABSTRACT Experimental results obtained for 2.3 kV SiC planar-gate power JBSFETs with different cell topologies are analyzed in this article using analytical models and numerical simulations. All the accumulation-channel devices were simultaneously manufactured in a 6-inch commercial foundry with channel length of 0.5 μm and gate oxide thickness of 55 nm. The Schottky contact width was chosen to achieve an on-state voltage drop of below 2.8 V in the 3rd quadrant for the integrated JBS diodes. Lower specific on-resistance of the Hexagonal and higher values for the Octagonal cell topologies compared with the conventional Linear cell design were experimentally observed. New analytical models developed for the various cell topologies reveal that these differences arise from changes in the relative contributions from the N^+ source contact, channel, and accumulation region resistances. The analysis reported in this article provides new insight on the importance of the accumulation layer resistance to the Octagonal cell topology. Numerical simulation reveal that the measured leakage current behavior correlates with the electric field observed at the Schottky contact within the 2.3 kV JBSFET cell structures. The leakage current begins to rise rapidly when the electric field exceeds 1.5 MV/cm due to Schottky barrier lowering and enhanced tunneling. The reverse transfer capacitance and gate charge were found to correlate with the JFET region density within the different cell topologies. The measured on-state voltage drop in the third quadrant was found to correlate with the JBS diode density in the cell topologies. A new high-frequency figure-of-merit [$V_{f3Q} * Q_{gd,sp}$] is proposed for SiC JBSFETs. The Octagonal cell designs are found to be the most suitable for high frequency applications of 2.3 kV JBSFETs based on the HF-FOMs [$R_{on} * Q_{gd}$] and [$V_{f3Q} * Q_{gd,sp}$].

INDEX TERMS 4H-SiC, accumulation-channel, analytical models, JBSFET, cell topology, linear, hexagonal, octagonal, figure-of-merit, numerical simulations, silicon carbide.

I. INTRODUCTION

Commercialization of silicon carbide (SiC) power MOSFETs has been evolving over a broad range of voltage ratings [1]. Most of the effort was initially focused on replacing 1.2 kV silicon IGBTs [2]–[4]. Subsequently, devices with voltage ratings of 1.7-3.3 kV were pursued [5]–[9]. The commercially available planar-gate SiC power MOSFETs utilize the conventional Linear cell topology. Other cell topologies have been studied for 1.2 kV rated SiC planar-gate power MOSFETs without an integrated JBS diode [10], [11]. The impact of cell topology was extended to 600 V SiC MOSFETs [12] without integrated JBS diodes.

Putting an anti-parallel SiC JBS diode with the SiC power MOSFET has been demonstrated to reduce power losses in applications [13]. An additional separately packaged component adds space and cost to the power electronics. Integration of the SiC JBS diode inside the 1.2 kV SiC planar-gate linear-cell MOSFET chip created the first JBSFET structure [14]. The net SiC chip area and manufacturing cost was reduced with this approach because the space taken by the edge termination for the separate JBS diode is eliminated [15]. The reverse-recovery current was shown to reduce with integration of the JBS diode within the 1.2 kV planar-gate SiC MOSFET.

Avalanche ruggedness of the JBS diode, not integrated into the 650 V SiC power MOSFET cell structure, with a hexagonal layout was reported in 2018 [16], [17]. The impact of various cell topologies on 1.2 kV SiC planar-gate

accumulation-channel JBSFETs was reported in 2019 [18]. In 2020, 600 V JBSFETs were reported with a specific on-resistance of 5.6 mΩ-cm^2 at a gate bias of 20 V using the linear cell topology [19]. The performance of 650 V SiC planar-gate inversion-channel JBSFETs with 27 nm gate oxide thickness was recently published [20].

Photovoltaic (PV) inverters utilize commercially available 1.2 kV devices in complex multi-level converters. Availability of 2.3 kV SiC devices can reduce the complexity of the converter and lead to better efficiency [21]. Other applications for 2.3 kV SiC power MOSFET are electric ships [22], fly-back auxiliary power supplies [23], and electric lighting [24]. SiC power MOSFETs have been reported with blocking voltages of 1.7 to 2.4 kV [5]–[9]. None of these higher breakdown voltage devices contained an integrated JBS diode.

Identification of the cell topology to achieve the best performance for 2.3 kV SiC planar-gate JBSFETs is valuable for the applications mentioned above. The reduced drift region doping concentration for 2.3 kV devices coupled with a thicker drift region to support the larger voltage [25], [26] alters the characteristics of JBSFETs when compared with 600 and 1.2 kV devices. The larger blocking voltage can increase the electric field at the Schottky contact within JBSFETs producing enhanced leakage current. The larger drift region resistance can increase the on-state voltage drop of the JBS diode within the JBSFET until it may not clamp conduction of the body diode. It is therefore necessary to evaluate the impact of the cell topology on 2.3 kV SiC JBSFETs even if this has been previously done for lower breakdown voltage devices.

Experimentally measured data on accumulation-channel, planar-gate, 2.3 kV 4H-SiC power JBSFETs for three (linear, hexagonal and octagonal) cell topologies was recently provided in a brief 2-page abstract [27]. Detailed description of the electrical characteristics and analysis of the cell designs could not be included in this abstract due to limited space. In this article: (a) more experimental data regarding these structures is provided; (b) new analytical models for the specific on-resistance of various cell structures are given that provide insight into the relative contribution of various components; and (c) the results of numerical simulations are shown that reveal the origin of leakage current in the integrated JBS diodes. The N$^+$ source contact resistance is found to be significant for the 2.3 kV JBSFETs with the Linear cell topology, while the accumulation layer resistance is shown to significantly increase the specific on-resistance for the Octagonal cell topology. A new high frequency figure-of-merit is also proposed in this article pertinent for evaluation of the relative performance of JBSFETs. This work allows identifying the best cell topology for 2.3 kV SiC planar-gate JBSFETs for the first time.

II. DEVICE STRUCTURE AND CELL LAYOUT

All the fabricated 2.3 kV JBSFET structures utilized JBS diodes that were integrated within the MOSFET cell. An accumulation-mode channel was employed for the MOSFET portion to reduce the resistance [10]. A cross-section of the basic unit-cell for the JBSFETs is illustrated in Fig. 1 with all the relevant dimensions. A gap in the P$^+$ shielding region is formed to accommodate the JBS diode. The P$^+$ contact region in the power MOSFET cells serves as the P$^+$ region used to suppress leakage current at large blocking voltage in the JBS diode [25], [26]. The doping of the JFET region was increased to 3.0 x 10^{16} cm^{-3} for improving the MOSFET on-resistance [28]. The series resistance of the JBS diode was also reduced by utilizing the same enhanced doping below the Schottky contact. Breakdown voltage close (over 95 %) to the ideal parallel-plane case was achieved at the edges of the devices by employing the hybrid-JTE edge termination [29]. As a consequence, the leakage current and breakdown voltage of the JBSFETs was determined by the cell topology.

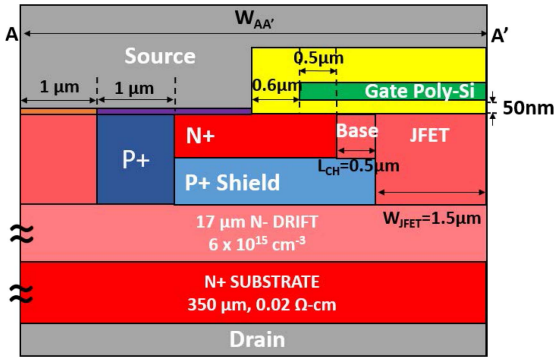

FIGURE 1. Half-cell cross-section of the 2.3 kV, accumulation-channel, JBSFET structure.

Three cell topologies (Linear, Hexagonal, and Octagonal) were examined for the 2.3 kV SiC JBSFETs. A top view of the cell layouts is provided in Fig. 2. Two designs for the Octagonal case were used with different size for the JBS diode area to examine impact on third quadrant voltage drop for this relatively new cell topology. The cross-section shown in Fig. 1 applies along the line A-A' marked in Fig. 2 for each topology. A channel length of 0.5 µm was designed for all the devices by choosing the boundaries for the P$^+$ shield and N$^+$ source regions.

The conventional Linear cell topology shown in Fig. 2(a) contains the Schottky contact along its entire length with a half-width (W_{SCH}) of 1.0 µm. A Schottky contact with a half-width (W_{SCH}) of 1.5 µm was placed in the middle of the Hexagonal polysilicon gate electrode opening for the Hexagonal topology as shown in Fig. 2(b). For the Octagonal cell designs, the Schottky contact was located inside the polysilicon window between the Octagonal shaped polysilicon gates. A larger Schottky contact half-width W_{SCH} of 2.8 µm was used in the Oct_B cell design compared with 1.1 µm for the Oct_A design.

The Schottky contact half-width (W_{SCH}) within the JBSFET cell design must be chosen to achieve an on-state voltage drop below 3.0 V for the integrated JBS diode to

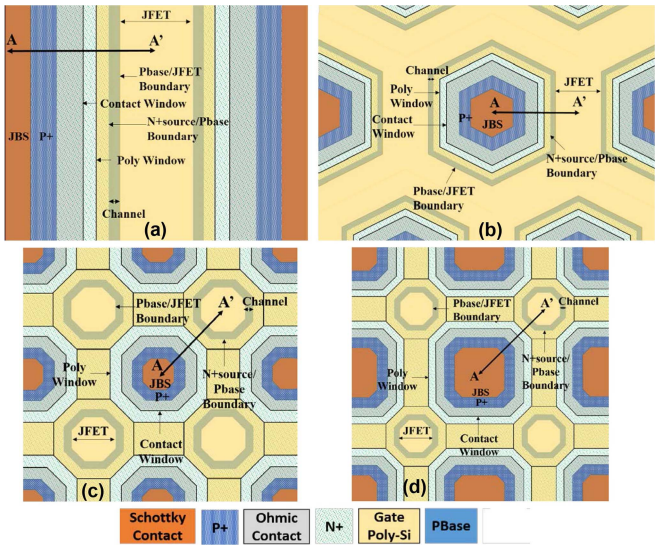

FIGURE 2. Cell layouts for the four 2.3 kV JBSFET designs: (a) Linear with $W_{SCH} = 1g\mu m$; (b) Hexagonal with $W_{SCH} = 1.5g\mu m$; (c) Octagonal A with $W_{SCH} = 1.1g\mu m$; (d) Octagonal B with $W_{SCH} = 2.8g\mu m$. The channel regions are shown as a greenish-grey regions. The Schottky contact regions are shown as the orange regions.

ensure clamping-off the P-N junction body-diode within the MOSFET portion. The Schottky contact half-width (W_{SCH}) also impacts the specific on-resistance, the specific gate-drain capacitance and specific gate-charge for the MOSFET portion within the JBSFETs because it alters the cell pitch ($W_{A-A'}$).

The JBS diode density is defined as the ratio of the Schottky contact area to the cell area. The JBS diode occupies between 5 and 17 % of the total area as documented in Table 1 for the different cell designs. The channel density is defined as the width of channel within a cell to the cell area. The JFET density is defined as the ratio of JFET region area to cell area. These design parameters, whose values are provided in Table 1 for each cell design, will be shown to be useful for understanding the JBSFET electrical characteristics.

The gate poly-Si overlap area given in Table 1 for the cell designs determines the input capacitance for the devices [25]. It is defined as the area where the gate poly-Si overlaps the N^+ source or P-base regions. This area includes the polysilicon bars used to connect the Octagonal polysilicon islands in the Octagonal cell designs. The parameters provided in Table 1 will be used in Section IV to analyze the measured electrical characteristics for the different cell topologies.

III. DEVICE FABRICATION

The 2.3 kV planar-gate accumulation-channel 4H-SiC JBSFETs were manufactured in a 6-inch foundry (X-Fab, TX) using the 11-mask PRESiCE^{TM} process engineered by NCSU [30]. N-type epitaxial layers grown on 4H-SiC 6-inch N^+ substrates with 17 μm thickness and doping concentration of 6×10^{15} cm^{-3} were used as the starting material.

TABLE 1. 2.3 kV JBSFET cell design information.

	Linear	Hexagonal	Oct_A	Oct_B
$W_{A-A'}$ [μm]	6.1	6.6	5.9	7.6
W_{SCH} [μm]	1.0	1.5	1.1	2.8
Channel Density [μm^{-1}]	0.164	0.211	0.193	0.116
JFET Density	0.246	0.403	0.109	0.065
JBS Diode Density	0.164	0.052	0.054	0.167
Schottky Area [cm^2]	7.38×10^{-3}	2.34×10^{-3}	2.43×10^{-3}	7.51×10^{-3}
Gate Overlap Area [cm^2]	7.40×10^{-3}	1.10×10^{-2}	1.77×10^{-2}	1.45×10^{-2}

The ideal specific on-resistance of the epitaxial layer is 1.7 mΩ-cm^2. The parallel-plan breakdown voltage of the layer is 2700 V. The N-base surface concentration was optimized to obtain a threshold voltage of 2.5 V for the case of a gate oxide thickness of 55 nm [10]. The 55 nm gate oxide was thermally grown followed by NO annealing to obtain an accumulation channel mobility of 25 cm^2/V-s at an on-state gate bias of 20 V. This conventional value of 55 nm for the gate oxide thickness was chosen compared with 27 nm used for the 650 V JBSFETs [20] because the channel component comprises a smaller fraction for the 2.3 kV JBSFET due to an increase in the drift region contribution. The oxide thickness was verified using an MOS capacitor test element located on the wafers. The Ni contacts were annealed at 900 ^{o}C to simultaneously obtain ohmic contacts to the N^+ and P^+ regions while achieving a good Schottky contact to the N-drift region with the enhanced JFET doping [14], [19].

IV. ANALYSIS OF MEASURED DEVICE CHARACTERISTICS

The device characteristics measured for the different cell topologies of the 2.3 kV 4H-SiC JBSFETs were: (a) breakdown voltage; (b) leakage current; (c) on-resistance; (d) threshold voltage; (e) transconductance; (f) input capacitance; (g) output capacitance; (h) reverse transfer capacitance; and (i) gate charge. Sixty devices with each cell design were measured to obtain the statistical distributions. Typical characteristics are shown in the paper together with average values for various parameters used for the device comparison. The best values for the on-resistance are provided because they are often reported in previous papers.

A. BREAKDOWN VOLTAGE AND LEAKAGE CURRENT

Zero gate bias blocking characteristics were obtained using a Keysight B1505A curve tracer. The typical characteristics for the four SiC JBSFET cell designs are shown in Fig. 3 using representative devices from a chip array located in the middle of the wafer. The breakdown voltage was defined using the typical 100 μA current level used in datasheets for SiC power MOSFETs with similar active area. This corresponds to a leakage current density of 2.2 mA/cm^2. The breakdown voltage varied by less than 50 V for each cell design across the wafer. It can be seen that the conventional Linear cell design has a breakdown voltage of

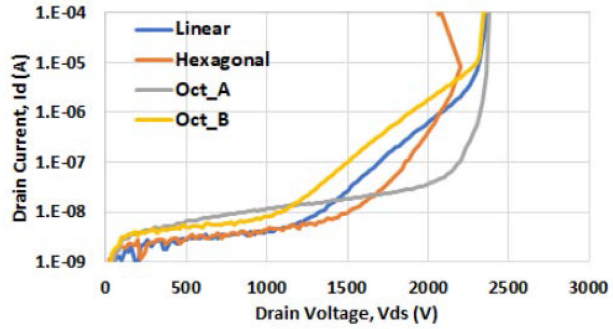

FIGURE 3. The blocking characteristics measured for the four JBSFET cell designs with zero gate bias.

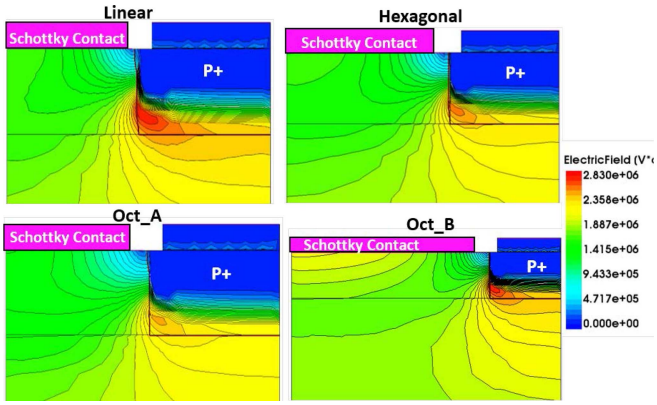

FIGURE 4. Electric field contours for the JBS diodes within the four cell designs at a drain bias of 2000 V.

2324 V, while the Hexagonal cell has a reduced breakdown voltage of 2079 V due to a snap back in its blocking characteristics. This snap-back in the blocking characteristics for the Hexagonal cell design has been consistently observed in the case of both MOSFETs and JBSFETs with other blocking voltages [10], [12], [18], [20], [32]. It is caused by high electric fields produced at the sharp edges of the hexagonal shaped P^+ shielding regions. All the fabricated devices with Hexagonal cells exhibit this behavior. The snap-back did not cause catastrophic failure of the devices during testing.

The Octagonal cell designs have the highest breakdown voltage of 2377 V for the Oct_A case and 2340 V for the Oct_B case. The breakdown voltages for the Octagonal cell designs exceed that of the Linear cell case because the electric field at the P-N junction is reduced due to the saddle junction formed under the octagonal polysilicon gate regions compared with a cylindrical junction formed in the Linear cell. The reduction of electric field by forming a saddle junction was first reported for the atomic-lattice-layout [31].

The behavior of the leakage current is unique for each of the four cell designs in Fig. 3. The leakage currents observed for all four cell designs are low ($<$ 10 nA) at drain bias values up to 1000 V. The leakage current for the Linear and Hexagonal cell designs begins to increase rapidly at about 1500 V. This effect occurs for the Octagonal Oct_B cell design at a drain bias of 1000 V, and is not evident for the Oct_A cell design.

Numerical simulations of the JBS diode portion within the four 2.3 kV JBSFET cell designs were performed to understand the observed trends in the leakage currents. The JBS diode portion in the Linear cell design was modelled with 2D simulations. From the layouts shown in Fig. 2, the JBS diode portion in the Hexagonal and Octagonal cell designs can be approximated using circular symmetry around the center of the Schottky contact. These JBS diodes were modelled using the 2D cylindrical geometry in Sentaurus TCAD with a 3D device specified by rotation of a 2D mesh. The center of the Schottky contact was used for rotation in these cases.

Electric field contours are shown in Fig. 4 at a drain bias of 2000 V for the integrated JBS diodes within the four cell designs. A high electric field occurs at the corner of the P-N junction for all cases as expected due its rectangular shape in SiC devices. The electric field at the corner of the P-N junction is also determined by the proximity of the adjacent P-N junction in the JBS diode structure. A smaller distance between the P-N junctions, corresponding to a reduced Schottky contact width in the JBS diode structure, lessens the electric field at the corner of the P-N junction by relaxing the curvature of the potential contours around the P-N junctions. The largest electric field is observed at the P-N junction in the case of the Linear cell design with W_{SCH} of 1.0 μm due to the formation of a cylindrical junction. The electric field at the P-N junction for the Hexagonal and Oct_A cases are smaller than for the linear case in spite of their larger values of W_{SCH} of 1.5 and 1.1 μm, respectively, because a saddle junction is formed by the rotation which diminishes electric field crowding. The electric field at the P-N junction for the Octagonal case Oct_B design is found to be larger than the Oct_A design because of its larger W_{SCH} of 2.8 μm.

The electric field has the highest value at the center of the Schottky contact in JBS diode structures [26]. This electric field produces enhanced leakage current due to Schottky barrier lowering and tunneling currents [25]. The color contours in Fig. 4 clearly show a larger electric field at the middle of the Schottky contact for the case of the Octagonal Oct_B design due to the relatively large W_{SCH} of 2.8 μm than the Oct_A design.

The electric field profile below the center of the Schottky contact in the JBS diodes is shown in Fig. 5 at a drain bias of 2000 V for the four cell designs. The Hexagonal case has very similar profile as the Linear case with suppression of the electric field at the Schottky contact to 1.6 MV/cm compared with a peak value of 1.9 MV/cm below the contact. The electric field at the Schottky contact for the Octagonal Oct_A design is reduced to 1.4 MV/cm. In contrast, the electric field at the Schottky contact for the Octagonal Oct_B design is larger than the Linear case with a value of 2.1 MV/cm.

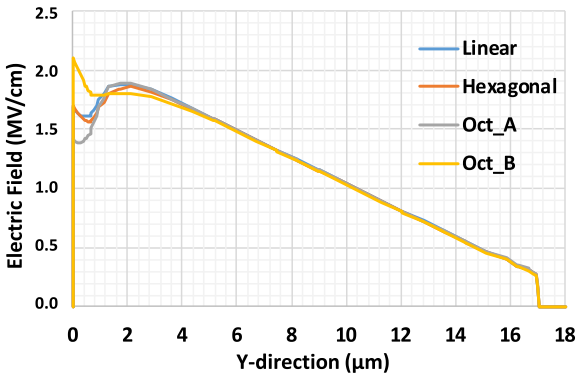

FIGURE 5. Electric field profile with depth at a drain bias of 2000 V below the center of the Schottky contact in the JBS diodes within the four cell designs.

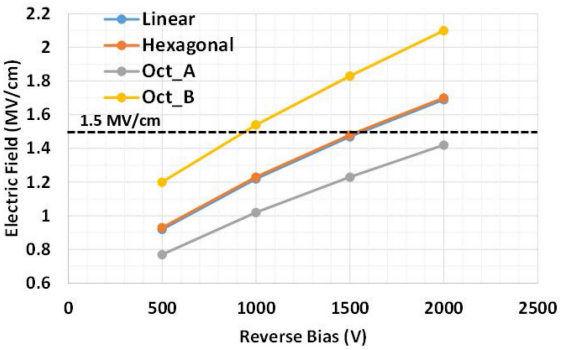

FIGURE 6. Increase in Electric field at the middle of the Schottky contact for the four cell designs with increasing drain bias.

In order to understand the on-set of leakage current associated with the Schottky contact in the integrated JBS diodes, it is necessary to examine the rise in electric field at the middle of the Schottky contact with increasing drain bias for each cell design. This electric field is shown in Fig. 6 for the four cell designs up to a drain bias of 2000 V. It can be seen that the smallest electric field occurs for the Octagonal Oct_A case because the shielding by the P^+ region is strong due to the saddle junction and a small Schottky contact half-width W_{SCH} of 1.1 μm. The largest electric field is observed for the Oct_B cell design due to its large Schottky contact half-width W_{SCH} of 2.8 μm. The same magnitude of 1.5 MV/cm for the electric field at the Schottky contact occurs when the drain voltage reaches 1000 V for the Octagonal Oct_B cell design, and 1500 V for the Hexagonal and Linear cases. The leakage currents for these structures begins to increase rapidly in Fig. 3 at these voltages. It can be concluded that an electric field of 1.5 MV/cm is needed for the observation of rapidly increasing leakage current in 2.3 kV JBSFETs. The same value for the electric field of 1.5 MV/cm for the on-set of rapid increase in leakage current was previously observed for 650 V SiC JBSFETs [20]. Since the electric field determines the Schottky barrier lowering and tunneling induced enhancements in leakage current [25], it is reasonable that the same value of 1.5 MV/cm applies to

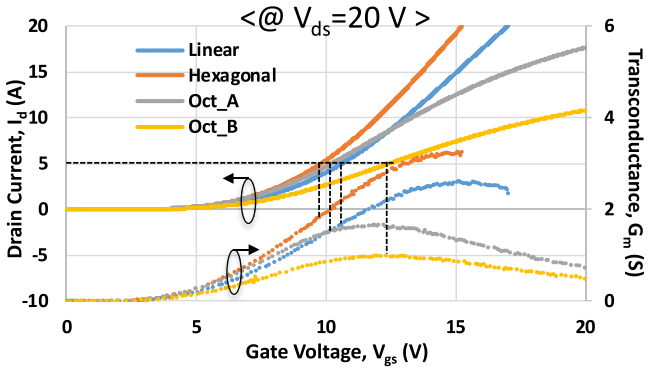

FIGURE 7. Transfer characteristics at V_{ds} = 20 V of the four cell designs of 2.3 kV SiC JBSFETs with the extracted transconductance.

TABLE 2. Specific on-resistance of 2.3 kV JBSFETs.

	Linear	Hexagonal	Oct_A	Oct_B
$R_{on,sp}$[avg] @ 5A (mΩ-cm^2)	10.5	8.4	13.7	24.6
$R_{on,sp}$[avg] @ 1A (mΩ-cm^2)	9.8	8.1	12.3	19.4
$R_{on,sp}$[best] @ 1A (mΩ-cm^2)	9.2	7.6	11.1	16.9

all SiC JBSFETs independent of voltage rating. It is worth noting that a rapid increase in the leakage current does not occur for the Octagonal Oct_A case because the electric field remains below 1.5 MV/cm up to 2000 V due to its smaller Schottky contact half-width W_{SCH} of 1.1 μm and better shielding by the saddle junction formed for its JBS diode.

The electric fields obtained from the numerical simulations reveal the reason for the Octagonal Oct_A cell design producing the highest measured breakdown voltage and smallest leakage current for 2.3 kV planar-gate JBSFETs.

B. THRESHOLD VOLTAGE AND TRANSCONDUCTANCE

Transfer characteristics were measured in the linear region for the four cell designs using the Keysight B1505A curve tracer with a drain bias of 0.1 V (not shown). They were very similar for all cases due to the same accumulation-mode channel design [32]. The threshold voltages at 1 mA for all four cases were found to have the same value of 2.5 V.

The transfer characteristics were also measured in the saturation region for the four cell designs by using a drain bias of 20 V as shown in Fig. 7. The tranconductance was extracted at a drain current of 5 A as indicated in the figure. The transconductance values were 1.7, 1.9, 1.5 and 1.0 S for the Linear, Hexagonal, Octagonal Oct_A and Octagonal Oct_B cases, respectively. These values are proportional to channel densities provided in Table 1 as expected.

C. ON-RESISTANCE

The on-state i-v characteristics were measured using the Keysight B1505A curve tracer with a gate bias of 20 V. They are shown in Fig. 8 for the four cell designs. The average value of the specific on-resistances previously reported [27]

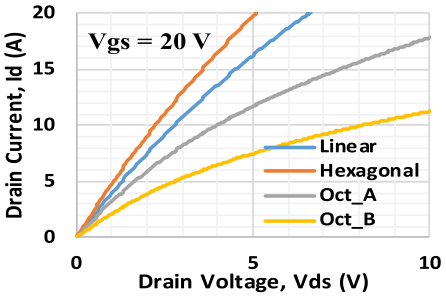

FIGURE 8. On-state characteristics measured for the 2.3 kV JBSFETs with four cell designs.

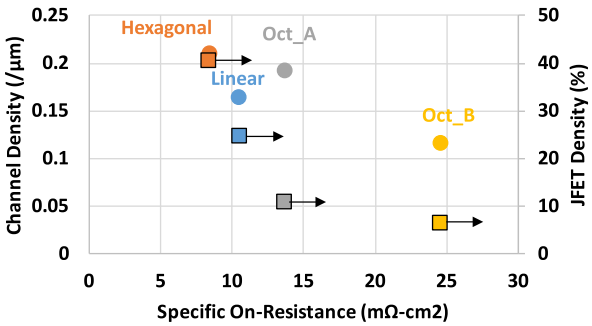

FIGURE 9. Correlation between measured specific on-resistance for the four cell designs of 2.3 kV JBSFETs with channel and JFET density. The circular and square symbols correspond to channel density and JFET density.

for the four cell designs extracted from the data at a drain current 5 A are provided in Table 2. The Hexagonal cell design has a specific on-resistance value lower than the bench mark Linear design while the Octagonal cells have much larger values. This is partially due to on-set of quasi-saturation in Fig. 8 for the Octagonal cell cases. The specific on-resistance extracted in the linear region at a drain current of 1 A is also provided in Table 2 in this article in order to compare them to values obtained by analytical modelling without quasi-saturation discussed below. In addition, the best values are included in Table 2 because they are often quoted in publications.

The specific on-resistance of a power MOSFET is expected to be smaller when the channel and JFET density are increased [25]. This behavior is observed for the 2.3 kV JBSFETs as shown in Fig. 9. The smallest specific on-resistance for the Hexagonal cell design is observed to be due to its large channel and JFET densities (see Table 1). The larger specific on-resistances for the Octagonal cell design Oct_A is seen to be mainly due to its low JFET density. The even larger specific on-resistances for the Octagonal cell design Oct_B is seen to be due to its low channel and JFET densities.

Analytical models for the specific on-resistance of Linear cell SiC power MOSFETs that are previously available [25] can be easily extended to JBSFETs. They have been derived using two-dimensional analysis of current flow in the cells [25]. New analytical models are however needed for the specific on-resistance of the Hexagonal and Octagonal JBSFET cases because the current is three-dimensional in shape. They were derived for this article using circular co-ordinates to represent the Hexagonal and Octagonal polysilicon gate structures. The new models account for a reduction of current density for current flow into the JFET region for the Hexagonal case, and increase in current density for the Octagonal case as current flows into the JFET region. The current crowding effect is similar to that discussed in detail with illustrations for the Hexagonal and ALL cell topologies for IGBTs with regard to latch-up [25].

Analytical solutions for the specific on-resistances were derived using a circular geometry as approximations for the Hexagonal and Octagonal cells. The source specific contact resistance was derived by dividing the specific contact resistance by the source contact area and multiplying with the cell area. The specific channel resistance was derived by accounting for the circular shape of the channel width in these cells. Similarly, the specific accumulation layer resistance was derived by accounting for the circular shape of its width in these cells. The JFET region has a rectangular cross-section in the previously analyzed Linear cell geometry [25]. In contrast, the specific on-resistance for the JFET region of the Hexagonal and Octagonal cells was derived by accounting for the cylindrical shape of the JFET region with a circular cross-section. The cross-section for current flow in the drift region for the previously analyzed Linear cell geometry has a trapezoidal shape. In contrast, the specific drift region resistance of the Hexagonal and Octagonal cells was derived by accounting for current spreading in a conical geometry from the cylindrical JFET regions. These derivations automatically account for changes in current density along the current flow path as holds true for the previously derived models for the Linear cell case.

The analytical solutions for the specific on-resistances derived for the Hexagonal cell based up on a circular geometry are:

$$R_{CS,sp} = \rho_C \frac{(W_{AA'})^2}{2r_C W_{N+}} \tag{1}$$

$$R_{CH,sp} = \frac{L_{CH}(W_{AA'})^2}{2r_{CH}\mu_{NA}C_{OX}(V_G - V_{TH})} \tag{2}$$

$$R_{A,sp} = \frac{(W_{AA'})^2}{2\mu_{NA}C_{OX}(V_G - V_{TH})} \ln\left[\frac{r_{CH} + K_A W_{JFET}}{r_{CH}}\right] \tag{3}$$

$$R_{JFET,sp} = \frac{\rho_{JFET} x_{JP+}(W_{AA'})^2}{\left[(W_{AA'})^2 - (r_{P+})^2\right]} \tag{4}$$

$$R_{D,sp} = \frac{\rho_D W_{AA'}}{2} \ln\left[\left(\frac{W_{AA'}}{W_{JFET} - W_{D,JFET}}\right) \times \left(\frac{2W_{AA'} - W_{JFET} - W_{D,JFET}}{W_{AA'}}\right)\right] + \rho_D(t_{EPI} - x_{JP+} - r_{P+}) \tag{5}$$

The analytical solutions for the specific on-resistances derived for the Octagonal cell based up on a circular

geometry are:

$$R_{CS,sp} = \rho_C \frac{(W_{AA'})^2}{\pi r_C W_{N+}} \quad (6)$$

$$R_{CH,sp} = \frac{(W_{AA'})^2}{\pi \mu_{NA} C_{OX}(V_G - V_{TH})} \ln\left[\frac{L_{CH} + W_{JFET}}{W_{JFET}}\right] \quad (7)$$

$$R_{A,sp} = \frac{(W_{AA'})^2}{\pi \mu_{NA} C_{OX}(V_G - V_{TH})} \ln\left[\frac{W_{JFET} - W_{D,JFET}}{K_A W_{JFET}}\right] \quad (8)$$

$$R_{JFET,sp} = \frac{2\rho_{JFET} x_{JP+}(W_{AA'})^2}{\left[\pi\left(W_{JFET} - W_{D,JFET}\right)^2\right]} \quad (9)$$

$$R_{D,sp} = \frac{2\rho_D W_{AA'}(W_{AA'} - W_{JFET})}{\pi W_{JFET}} + \rho_D(t_{EPI} - x_{JP+} - r_{P+}) \quad (10)$$

where $R_{CS,sp}$, $R_{CH,sp}$, $R_{A,sp}$, $R_{JFET,sp}$, and $R_{D,sp}$ are specific resistances for the N^+ source contact, channel, accumulation layer, JFET, and drift regions, respectively.

The parameters in these equation are defined in Table 3. They are described here. ρ_C is the specific contact resistance to the N^+ source region; r_C is the contact radius ($W_{SCH} + W_{P+} + W_{N+}$) for the Hexagonal cell with $W_{SCH} = 1.5$ μm; L_{CH} is the channel length (0.5 μm for all the devices); $W_{AA'}$ is the half-cell pitch shown in Fig. 1 with values given in Table 1; r_{CH} is the channel radius ($W_{SCH} + W_{P+} + W_{N+} + W_I + W_{OV} + L_{CH}$) for the Hexagonal cell; C_{OX} is the specific gate oxide capacitance (6.19×10^{-8} F/cm^2 for a gate oxide thickness of 55 nm); V_G is the gate bias (20 V); V_{TH} is the threshold voltage (2.5 V); K_A is the current spreading factor (0.3 for SiC power MOSFETs [26]); W_{JFET} is the half-cell JFET width (1.5 μm for all cell designs); ρ_{JFET} is the resistivity of the JFET region with enhanced doping (0.34 Ω-cm for all cells); x_{JP+} is the depth of the P^+ region (0.8 μm for all cases); r_{P+} is radius of the P^+ shielding region ($W_{SCH}+W_{P+}+W_{N+}+W_I+W_{OV}+L_{CH}$) for the Hexagonal cell; ρ_D is the resistivity of the drift region (1.02 Ω-cm); W_{DJFET} is depletion width in the JFET region (0.4 μm); t_{EPI} is the epitaxial layer thickness (17 μm). The values of $W_{P+} = 1.0$ μm, $W_{N+} = 1.0$ μm, $W_I = 0.6$ μm, $W_{OV} = 0.5$ μm are the same for all cell designs with the exception of the Oct_A design with $W_{N+} = 0.7$ μm. The accumulation channel mobility (μ_{nA}) was measured as 25 cm^2/V-s for a 20 V gate bias using a FATFET test structure located on the same wafer as the devices.

The relative contributions from different components of the specific on-resistance for each of the four cell designs can be obtained by using the analytical models. It can be seen from Fig. 10 that the N^+ source contact resistance is the largest component for the JBSFET Linear cell design. This is because of a large specific contact resistance of 7×10^{-4} Ω-cm^2 to the N^+ source region resulting from a low 900 ^{o}C anneal temperature used for SiC JBSFETs [14],bib19. It has been shown that reducing the contact resistance to the N^+ region by increasing the anneal temperature degrades the Schottky barrier contact producing unacceptable levels of leakage current [14], [19]. The large contact resistance contribution is also observed for the JBSFET Hexagonal cell design. It is reduced for the JBSFET Octagonal cell designs because of a relatively larger contact area in these layouts. In contrast, the JBSFET Octagonal cell designs have a large contribution from the accumulation resistance because of current constriction as current flows radially from the channel into the JFET region. The analytical model provides an important insight that a large contact resistance contribution is inherent for the conventional Linear cell JBSFETs when the JBS diode is integrated into the MOSFET cells, while the accumulation region resistance makes a large contribution to the specific on-resistance for the Octagonal cell JBSFETs.

The specific on-resistance for a 2.3 kV power MOSFET fabricated on the same wafer with the Linear cell design was 8.0 mΩ-cm^2 as previously reported [32]. This value is 18 % smaller than the 2.3 kV JBSFET with the Linear design reported in this article because the cell pitch for the MOSFET can be reduced to 4.2 μm from 6.1 μm for the JBSFET. The cell pitch for the optimally designed MOSFET is smaller

TABLE 3. Definition of device parameters for analytical solutions.

Parameter	Definition
ρ_C	Specific contact resistance to the N^+ source region
r_C	Contact radius
L_{CH}	Channel Length
r_{CH}	Channel radius
C_{OX}	Gate oxide specific capacitance
K_A	Current spreading factor
W_{JFET}	Half-cell JFET width
ρ_{JFET}	JFET region resistivity
X_{JP+}	Depth of P+ shielding region
r_{P+}	Radius of P+ shielding region
ρ_D	Resistivity of drift region
W_{DJFET}	Depletion width in JFET region
μ_{NA}	Accumulation channel mobility
t_{EPI}	Epitaxial layer thickness
W_{P+}	Width of P+ contact region
W_{SCH}	Width of Schottky contact
W_{N+}	Width of N+ contact region
W_I	Width of contact to poly-gate
W_{OV}	Width of overlap between gate and N+ source

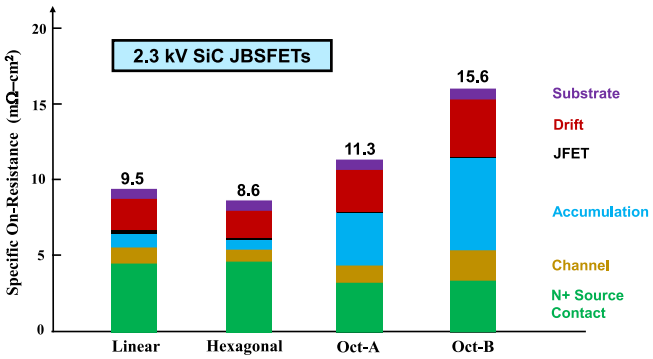

FIGURE 10. Distributions of the specific on-resistance components for the four cell designs of 2.3 kV JBSFETs.

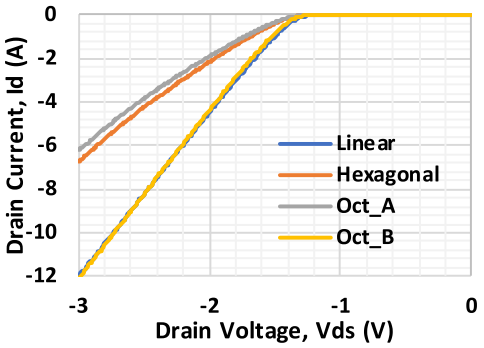

FIGURE 11. Third quadrant i-v characteristics for the four cell designs of SiC JBSFET.

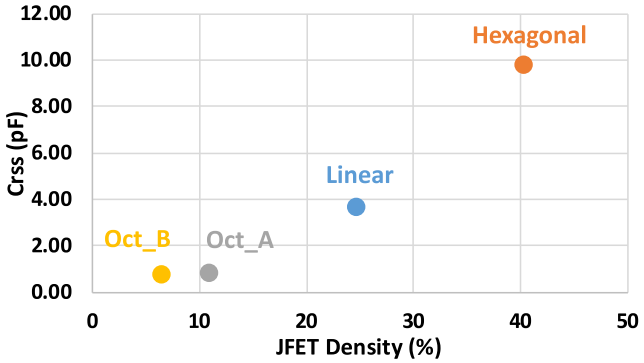

FIGURE 12. Correlation between measured reverse-transfer capacitances at 1000 V for the four cell designs of 2.3 kV JBSFETs with JFET density.

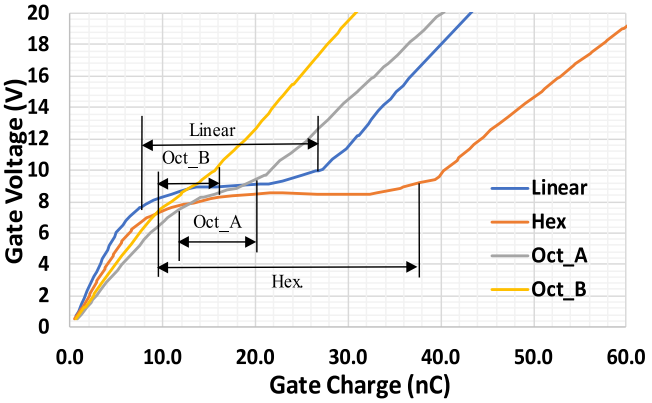

FIGURE 13. Measured gate charge waveforms for the 2.3 kV SiC JBSFETs for the four cell designs @V_{ds}=1200 V, I_d=10 A.

because space used for the Schottky contact in Fig. 1 is eliminated. The smaller cell pitch increases the channel density resulting in reducing the specific on-resistance.

D. THIRD QUADRANT CHARACTERISTICS

The JBS diode area inside the SiC JBSFET must be sufficiently large to ensure a third quadrant voltage drop of less than 3.0 V to prevent activation of the MOSFET P-N body diode. Previous publications [33], [34] have experimentally confirmed the improved performance of the JBSFETs under high temperature switching operation and during short-circuit events when the P-N body diode is by-passed by the JBS diode. This becomes more challenging with increasing voltage rating due to the larger drift region series resistance. The i-v characteristics in the third quadrant are shown in Fig. 11 for the four cell designs of the 2.3 kV JBSFETs. The characteristics for the Linear cell and Octagonal Oct_B cell designs are nearly identical with an on-state voltage drop of only 2.0 V at 4.5 A (100 A/cm^2). This is consistent with the same Schottky contact area and JBS diode density for both of these designs (see Table 1). The characteristics for the Hexagonal cell and Octagonal Oct_A cell designs are also nearly identical with an on-state voltage drop of 2.6-2.7 V at 4.5 A. This is consistent with the same but smaller Schottky contact area and JBS diode density for both of these designs (see Table 1). All four cell designs are demonstrated to have adequate JBS diode area to satisfy the goal of bypassing the P-N body diode of the SiC MOSFET while achieving low leakage currents in the blocking mode.

E. DEVICE CAPACITANCES

An assessment of the switching performance of power MOSFETs can be made by comparison of the device capacitances. The input capacitance is a weak function of the drain bias. Its measured values were 800, 900, 1400, and 1200 pF for the Linear, Hexagonal, Octagonal Oct A, and Oct_B cases, respectively. As expected, these values are proportional to the gate overlap area previously provided in Table 1. The measured output capacitances for the four cell designs up to a drain bias of 1000 V had the same value of about 34 pF at 1000 V because of a similar junction area.

The variation of the reverse-transfer capacitance with drain voltage was previously published [27]. Its magnitude is determined by the overlap of the gate electrode over the drift region in the power MOSFET structure [25]. As a consequence, the reverse-transfer capacitance for the 2.3 kV JBSFETs is found to be proportional to the JFET density in the cells as observed in the plot shown in Fig. 12.

F. GATE CHARGE

The gate charge waveforms shown in Fig. 13 were obtained for the four cell designs. The drain voltage transition time during turn-on and turn-off in an inductive load power circuit produces the largest switching power loss [25]. The gate voltage plateau charge (Q_{gd}) provides a good measure of this power loss and is provided in SiC power MOSFET datasheets. It can be seen that the Q_{gd} for the Hexagonal cell case is much larger than for the bench mark Linear cell case. On the other hand, it is much shorter for the Octagonal cell designs. The values for Q_{gd} obtained from the waveforms in Fig. 13 are 19, 29, 8.2, and 6.1 nC for the Linear, Hexagonal, Octagonal Oct_A and Oct_B cases, respectively.

The gate-drain charge is an integral of the reverse-transfer capacitance C_{rss} over the drain voltage excursion [25]. As a consequence, the Q_{gd} is found to be proportional to the

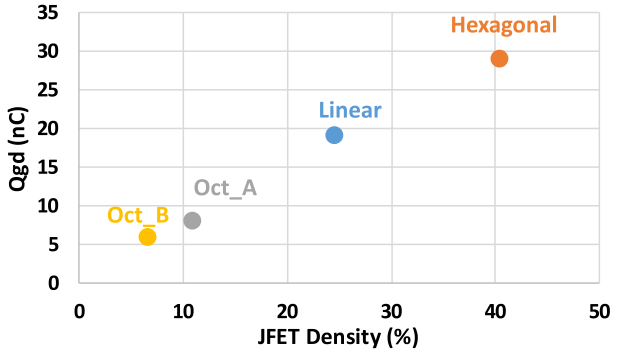

FIGURE 14. Correlation between measured gate-drain charge for the four cell designs of 2.3 kV JBSFETs with JFET density.

TABLE 4. 2.3 kV JBSFET figures-of-merit for various cell designs.

	Linear	Hexagonal	Oct_A	Oct_B
$Q_{gd,sp}$ (nC/cm^2)	422	644	182	136
FOM[R_{on}*Q_{gd}] (mΩ*nC)	4136	5216	2239	2638
V_{f3Q} @ 100 A/cm^2 (V)	2.0	2.6	2.7	2.0
FOM[V_{f3Q}*$Q_{gd,sp}$] (V*nC/cm^2)	894	1674	491	272

JFET density in the cells as observed in the plot shown in Fig. 14.

G. NEW JBSFET FIGURE-OF-MERIT

The specific on-resistance of the cell designs is an indicator of low frequency performance where switching losses are insignificant. The Hexagonal cell design is found to provide the lowest specific on-resistance for 2.3 kV 4H-SiC JBSFETs. However, SiC power transistors are targeted for high frequency applications to reduce the cost and size of passive elements and filters. It is therefore appropriate to employ the high frequency device figure of merit [$R_{on} * Q_{gd}$] for 2.3 kV 4H-SiC power MOSFETs [32].

The key attribute of the 4H-SiC JBSFETs is the integrated JBS diode for carrying current in the third quadrant. This enables elimination of reverse recovery power losses at high frequencies. Consequently, a new figure-of-merit is required to assess the relative performance of SiC JBSFETs. A new high frequency FOM for JBSFETs given by [$V_{f3Q} * Q_{gd,sp}$] is proposed in this article, where V_{f3Q} is the voltage drop in the third quadrant at a current density of 100 A/cm^2. The previously defined FOM[$R_{on} * Q_{gd}$] can be used to assess relative performance of JBSFETs in the first quadrant while the new proposed FOM[$V_{f3Q} * Q_{gd,sp}$] can be used to assess relative performance in the third quadrant for these devices. It has units of energy loss per cm^2.

Table 3 provides a summary of values used to compute the high-frequency figures-of-merit [$R_{on} * Q_{gd}$] and [$V_{f3Q} * Q_{gd,sp}$] for the four 2.3 kV JBSFET cell designs. From the data acquired in this work, it is found that best HF-FOM[$R_{on} * Q_{gd}$] is obtained with the Octagonal Oct_A cell design, with a value 1.85x superior to the 2.3 kV JBSFET with conventional Linear cell. The same Oct_A cell design for the JBSFET was previously found to provide the best HF-FOM[$R_{on} * Q_{gd}$] for 650 V devices as well [20]. However, the value of 2239 mΩ*nC for the 2.3 kV JBSFET Oct_A cell design is 1.82x larger than 1229 mΩ*nC for the 650V JBSFET devices. In addition, the value for V_{f3Q} at a current density of 100 A/cm^2 is much larger (2.7 V) for the 2.3 kV JBSFET Oct_A cell design compared with only 1.9 V for the 650 V JBSFETs with the Oct_A cell design. In addition, the data acquired from this work shows that the best HF-FOM[$V_{f3Q} * Q_{gd,sp}$] is obtained with the 2.3 kV JBSFET Octagonal cell Oct_B design, with a value 3.29x superior to the 2.3 kV JBSFET conventional Linear cell design.

V. CONCLUSION

2.3 kV SiC power JBSFETs with three cell topologies were successfully manufactured in a 6 inch foundry with excellent electrical characteristics. The performance of four cell designs at room temperature have been described and compared in detail in this article for the first time. All four cell designs were simultaneously fabricated using the same process and have identical die size. Consequently, there is no difference in the cost for manufacturing these designs. Analytical models and numerical simulation results provided insights into the observed electrical characteristics measured for each cell configuration.

An on-state voltage drop of less than 2.6 V in the third quadrant was achieved for all the cell topologies in spite of high drift region resistance for 2.3 kV devices by providing adequate area for the JBS diode portion to ensure MOSFET body-diode suppression. The chosen Schottky contact width within the JBSFET cells was able to maintain low leakage current for all cases. The best high-frequency figures-of-merit were observed for the Octagonal cell designs making them the most suitable for 2.3 kV SiC JBSFETs targeted for high frequency circuits.

REFERENCES

[1] J. W. Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. 26th Int. Symp. Power Semicond. Devices ICs*, Jun. 2014, pp. 79–82, doi: 10.1109/ISPSD.2014.6855980.

[2] S. Chowdhury, K. Matocha, B. Powell, G. Sheh, and S. Banerjee, "Next generation 1200V, 3.5 mΩ.cm^2 SiC planar gate MOSFET with excellent HTRB reliability," in *Proc. 30th Int. Symp. Power Semicond. Devices IC's*, 2018, pp. 427–430, doi: 10.1109/ISPSD.2018.8393694.

[3] Q. J. Zhang *et al.*, "Latest results on 1200 V 4H-SiC CIMOSFETs with Rsp,on of 3.9 mΩ·cm^2 at 150° C," in *Proc. 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 89–92, doi: 10.1109/ISPSD.2015.7123396.

[4] T. Zhao, J. Wang, A. Q. Huang, and A. Agarwal, "Comparisons of SiC MOSFET and Si IGBT based motor drive systems," in *Proc. IEEE Ind. Appl. Annual Meeting*, 2007, pp. 331–335, doi: 10.1109/07IAS.2007.51.

[5] A. Agarwal, S.-H. Ryu, M. Das, L. Lipkin, J. Palmour, and N. Saks, "Large area 4H-SiC power MOSFETs," in *Proc. 13th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2001, pp. 183–186, doi: 10.1109/ISPSD.2001.934585.

[6] K. Matocha, K. Chatty, S. Banerjee, and L. B. Rowland, "1700V, 5.5mOhm-cm^2 4H-SiC DMOSFET with Stable 225°C Operation," *Mater. Sci. Forum*, vol. 778, pp. 903–906, Feb. 2014, doi: 10.4028/www.scientific.net/MSF.778-780.903.

[7] A. Bolotnikov *et al.*, "Overview of 1.2 kV–2.2 kV SiC MOSFETs targeted for industrial power conversion applications," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, 2015, pp. 2445–2452, doi: 10.1109/APEC.2015.7104691.

[8] Q. J. Zhang *et al.*, "Next generation planar 1700 V, 20 mΩ 4H-SiC DMOSFETs with low specific on-resistance and high switching speed," *Mater. Sci. Forum*, vol. 897, pp. 521–524, May 2017, doi: 10.4028/www.scientific.net/MSF.897.521.

[9] W. Ni *et al.*, "1700V 34mΩ 4H-SiC MOSFET with retrograde doping in junction field-effect transistor region," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, 2019, pp. 1–3, doi: 10.1109/EDSSC.2019.8754174.

[10] K. Han and B. J. Baliga, "Comparison of four cell topologies for 1.2-kV accumulation-and inversion-channel 4H-SiC MOSFETs: Analysis and experimental results," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2321–2326, May 2019, doi: 10.1109/TED.2019.2905736.

[11] K. Han and B. J. Baliga, "The 1.2-kV 4H-SiC OCTFET: A new cell topology with improved high-frequency figures-of-merit," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 299–302, Feb. 2019, doi: 10.1109/LED.2018.2889221.

[12] A. Agarwal, K. Han, and B. J. Baliga, "Impact of cell topology on characteristics of 600V 4H-SiC planar mOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 773–776, May 2019, doi: 10.1109/LED.2019.2908078.

[13] C. Schmidt and M. Röblitz, "A performance comparison of SiC power modules with Schottky and body diodes," in *Proc. PCIM Europe*, 2017, pp. 816–823.

[14] W. Sung and B. J. Baliga, "Monolithically integrated 4H-SiC MOSFET and JBS diode (JBSFET) using a single ohmic/schottky process scheme," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1605–1608, Dec. 2016, doi: 10.1109/LED.2016.2618720.

[15] W. Sung and B. J. Baliga, "On developing one-chip integration of 1.2 kV SiC MOSFET and JBS diode (JBSFET)," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8206–8212, Oct. 2017, doi: 10.1109/TIE.2017.2696515.

[16] F. Hsu *et al.*, "High efficiency high reliability SiC MOSFET with Monolithically integrated schottky rectifier," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2017, pp. 45–48, doi: 10.23919/ISPSD.2017.7988889.

[17] C. T. Yen *et al.*, "Avalanche ruggedness and reverse-bias reliability of SiC MOSFET with integrated junction barrier controlled schottky rectifier," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2018, pp. 56–59, doi: 10.1109/ISPSD.2018.8393601.

[18] K. Han, A. Agarwal, and B. J. Baliga, "Comparison of new octagonal cell topology for 1.2 kV 4H-SiC JBSFETs with linear and hexagonal topologies: Analysis and experimental results," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2019, pp. 159–162, doi: 10.1109/ISPSD.2019.8757565.

[19] N. Yun, J. Lynch, and W. Sung, "Area-efficient, 600V 4H-SiC JBS diode-integrated MOSFETs (JBSFETs) for power converter applications," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 16–23, Oct. 2017, doi: 10.1109/JESTPE.2019.2947284.

[20] A. Agarwal, K. Han, and B. J. Baliga, "Assessment of linear, hexagonal, and octagonal cell topologies for 650 V 4H-SiC inversion-channel planar-gate power JBSFETs fabricated with 27 nm gate oxide thickness," *IEEE J. Electron Devices Soc.*, early access, Nov. 25, 2020, doi: 10.1109/JEDS.2020.3040353

[21] X. She, P. Losee, H. Hu, W. Earls, and R. Datta, "Evaluation of 2.5 kV silicon carbide MOSFET for 1.5 kV solar inverter application," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, 2018, pp. 2516–2523, doi: 10.1109/ECCE.2018.8557524.

[22] J. Wang *et al.*, "Power electronics building block (PEBB) design based on 1.7 kV SiC MOSFET modules," in *Proc. IEEE Electr. Ship Technol. Symp.*, 2017, pp. 612–616.

[23] X. Zhang and G. Sheh, "Implementation of 1.7 kV silicon carbide MOSFETs in auxiliary power supplies for industrial applications," *Chin. J. Elect. Eng.*, vol. 6, no. 3, pp. 46–55, Sep. 2020.

[24] H. Liu *et al.*, "Development of 1.7 kV 40 mΩ 4H-SiC power DMOSFETs," in *Proc. IEEE Elect. Light. Conf.*, 2018, pp. 117–119.

[25] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 2nd ed. Cham, Switzerland: Springer, 2019, ch. 6, pp. 283–440.

[26] B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices*. Hackensack, NJ, USA: World Sci., 2017, ch. 11, pp. 287–340.

[27] A. Agarwal, K. Han, and B. J. Baliga, "2.3 kV 4H-SiC accumulation-channel JBSFETs: Experimental comparison of linear, hexagonal and octagonal cell topologies," in *IEEE Device Res. Conf. Dig.*, 2020, pp. 84–85.

[28] W. Sung, K. Han, and B. J. Baliga, "Optimization of the JFET region of 1.2 kV SiC MOSFETs for improved high frequency figure of merit (HF-FOM)," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2017, pp. 238–241, doi: 10.1109/WiPDA.2017.8170553.

[29] W. Sung and B. J. Baliga, "A near ideal edge termination technique for 4500V 4H-SiC devices: The hybrid junction terminat Ion extension," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1609–1612, Dec. 2016, doi: 10.1109/LED.2016.2623423.

[30] B. J. Baliga, W. J. Sung, K. J. Han, J. Harmon, A. Tucker, and S. Syed, "PRESiCE^{TM}: Process engineered for manufacturing SiC electronic devices," *Mater. Sci. Forum*, vol. 924, pp. 523–526, Jun. 2018, doi: 10.4028/www.scientific.net/MSF.924.523.

[31] B. J. Baliga, H. R. Chang, T. P. Chow, and S. Al-Marayati, "New cell designs for improved IGBTsafe-operating-area," in *Proc. IEEE Int. Electron Devices Meeting*, 1988, pp. 809–812.

[32] A. Agarwal, K. Han, and B. J. Baliga, "Comparison of 2.3 kV 4H-SiC accumulation-channel planar MOSFETs fabricated with linear, square, hexagonal, and octagonal cell topologies," *IEEE Trans. Electron Devices*, vol. 67, no. 9, pp. 3673–3678, Sep. 2020.

[33] A. Kanale, B. J. Baliga, K. Han, and S. Bhattacharya, "Experimental study of high-temperature switching performance of 1.2 kV SiC JBSFET in comparison with 1.2 kV SiC MOSFETs," in *Proc. 12th Eur. Conf. Silicon Carbide Related Mater., Mater. Sci. Forum,* vol. 963, Jul. 2019, pp. 625–628.

[34] A. Kanale, K. Han, B. J. Baliga, and S. Bhattacharya, "Superior short circuit performance of 1.2 kV SiC JBSFETs compared to 1.2 kV SiC MOSFETs," in *Proc. 12th Eur. Conf. Silicon Carbide Related Mater., Mater. Sci. Forum,* vol. 963, Sep. 2019, pp. 797–800.