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# Graded Crystalline HfO<sub>2</sub> Gate Dielectric Layer for High-k/Ge MOS Gate Stack

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**ABSTRACT** Germanium (Ge) has gained great attention not only for future nanoelectronics but for back-end of line (BEOL) compatible monolithic three-dimensional (M3D) integration recently. For high performance and low power devices, various high-k oxide/Ge gate stacks including ferroelectric oxides have been investigated. Here, we demonstrate atomic layer deposited (ALD) polycrystalline (p-) HfO<sub>2</sub>/GeO<sub>x</sub>/Ge stack with an amorphous (a-) HfO<sub>2</sub> capping layer. The consecutively deposited a-HfO<sub>2</sub> capping layer improves hysteretic behaviors ( $\Delta V$ ) and interface state density ( $D_{it}$ ) of the p-HfO<sub>2</sub>/GeO<sub>x</sub>/Ge stack. Furthermore, leakage current density ( $J$ ) is significantly reduced ( $\times 100$ ) by passivating leakage paths through grain boundaries of p-HfO<sub>2</sub>. The proposed HfO<sub>2</sub> layer with the graded crystallinity suggests possible high-k/Ge stacks for further optimized Ge MOS structures.

**INDEX TERMS** Ge, amorphous, polycrystalline, ALD HfO<sub>2</sub>, leakage.

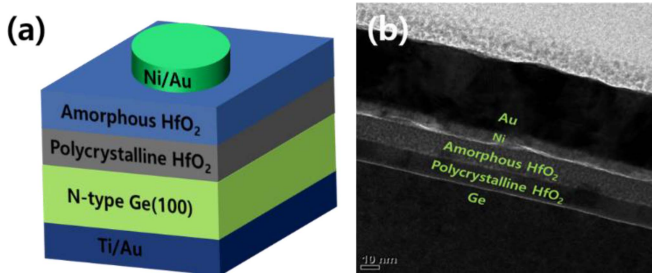
## I. INTRODUCTION

Germanium (Ge) has been one of the promising candidates for modern very large-scale integrated circuits and future nanoelectronics because of its high carrier mobility, stable performance and relatively silicon-compatible low-temperature process [1]–[5]. Most recently, back-end of line (BEOL) compatible monolithic three-dimensional (M3D) integration of high performance memory and logic has attracted much attention [6], [7]. Under the constraint of thermal budget ( $< 400$  °C), polycrystalline (p-) Ge is one of the strong candidates along with p-Si, metal-oxides, and two-dimensional semiconductors [7]–[11]. Although the scaling of Ge devices to the physical limit and thus thin equivalent oxide thickness (EOT) of gate-oxide are not aggressively demanded for BEOL-M3D integration, the thermal budget and other process conditions should be considered.

The stable and high quality gate stack formation on Ge has been the critical challenge to realize the aforementioned prediction [1], [3]. In particular, high-permittivity ( $k$ ) oxides is mandatory for low power consumption [12]. For the high-k/Ge gate stack, HfO<sub>2</sub>, one of the most promising

high-k materials in Si, is also very attractive because of its  $k$  value and/or ferroelectricity by doping or elaborated thermal annealing [13], [14], [15]. However, Ge atoms can easily diffuse into the HfO<sub>2</sub> during the atomic layer deposition (ALD) process and even low-temperature annealing process, resulting in large leakage current [16]. Moreover, the diffused Ge atoms significantly affect electrical characteristics such as poor hysteresis and mobility degeneration [1], [17], [18]. Other than single crystal oxides, poor interface properties and large leakage current are inevitable without an interfacial passivating layer.

Regarding the interfacial layer, extensive research has been conducted to passivate the Ge surface and various methods of high-quality GeO<sub>2</sub> [18]–[21], oxynitrides [22], [23], and 2-D materials such as molybdenum disulfide (MoS<sub>2</sub>) [24] have been investigated. Unlike the HfO<sub>2</sub> and ZrO<sub>2</sub>, the Y<sub>2</sub>O<sub>3</sub> layer is known to achieve high interface quality by suppressing the GeO<sub>2</sub> desorption [25]. However, the post-oxidation to introduce high-quality GeO<sub>2</sub> typically requires high-temperature thermal annealing process [26], [27], which is not compatible with the BEOL M3D integration. The Hf-based ferroelectric oxides with negative capacitance, which is very promising for



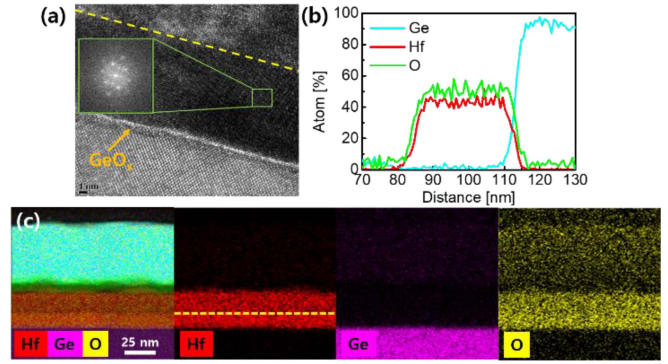
**FIGURE 1.** (a) A schematic diagram of the fabricated Ge MOSCAP with p-HfO<sub>2</sub> (10 nm)/a-HfO<sub>2</sub> (10 nm) gate dielectric layer, and (b) its cross-sectional TEM image.

low-power steep switching transistors, also require thermal annealing process. So alternative schemes of high-k oxide stack needs to be considered.

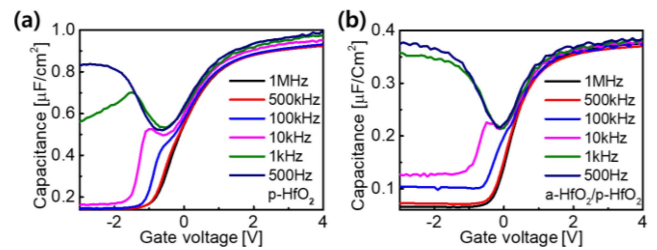
In this work, we proposed a-HfO<sub>2</sub> capping layer on top of the p-HfO<sub>2</sub>/GeO<sub>x</sub>/Ge gate stack. An oxide stack of HfO<sub>2</sub> with different oxide layers is known to have high density of dipoles inducing hysteresis and interface states [28], [29]; This HfO<sub>2</sub> stack allows minimized formation of dipoles inbetween. The crystallinity of the ALD p-HfO<sub>2</sub>/a-HfO<sub>2</sub> stack was confirmed by high resolution-transmission electron microscopy (HR-TEM). Bidirectional frequency-dependent capacitance- voltage (C-V) measurements were conducted to compare hysteretic behaviors ( $\Delta V$ ) of both p-HfO<sub>2</sub>/a-HfO<sub>2</sub> and p-HfO<sub>2</sub> gate stacks as a control sample. Moreover, interface trap densities ( $D_{it}$ ) were characterized and compared using Hi-Lo and conductance methods. Finally, leakage current density ( $J$ ) vs. oxide electric field ( $E_{OX}$ ) was characterized, and the effects of a-HfO<sub>2</sub> capping layer was discussed.

## II. EXPERIMENTS

Ge MOSCAPs were fabricated on n-type As-doped (100) Ge wafer with a nominal resistivity of 0.04 ~ 0.05  $\Omega\text{cm}$ . First, the surface was chemically cleaned, and then p-HfO<sub>2</sub> dielectric layer (10 nm) was deposited using ALD at an elevated stage temperature of 350 °C, followed by a-HfO<sub>2</sub> (~10 nm) deposition at 200 °C. Tetrakis(ethylmethy lamino)hafnium (TEMAH) and ozone were used as Hf precursor and oxygen source, respectively. The deposition rate was ~ 0.9  $\text{\AA}/\text{cycle}$ . To avoid crystallization of the a-HfO<sub>2</sub>, we first deposit p-HfO<sub>2</sub> using ALD at 350 °C followed by a-HfO<sub>2</sub> deposition at 200 °C, consecutively. Top contact electrodes of Ni/Au (10/50nm) were deposited by thermal evaporation and patterned using conventional photolithography and lift off process. Next, as a bottom contact, Ti/Au (20/80nm) was deposited by e-beam evaporation. No post-deposition annealing was conducted. For the comparison, Ge MOSCAPs with only p-HfO<sub>2</sub> dielectric layer (15 nm) was also prepared. Figs. 1 (a) and (b) show a schematic of the fabricated MOSCAP with p-HfO<sub>2</sub>/a-HfO<sub>2</sub> bilayer dielectrics and its cross-sectional TEM image at a low magnification, confirming the Ge gate stacks. C-V and current density-voltage (J-V) measurements were conducted using a HP 4284A LCR meter and 4200A SCS



**FIGURE 2.** (a) A cross sectional HR-TEM image of the p-HfO<sub>2</sub>/a-HfO<sub>2</sub>/GeO<sub>x</sub> stack with a FFT micrograph of the p-HfO<sub>2</sub> in the inset. (b) STEM EDS line profiles of the p-HfO<sub>2</sub>/a-HfO<sub>2</sub>/GeO<sub>x</sub>/Ge showing the change of atomic ratios at the interfaces. (c) Compositional element mapping of the several layer (Ge, Hf and O), and a higher density of Hf atom from the p-HfO<sub>2</sub> is observed.



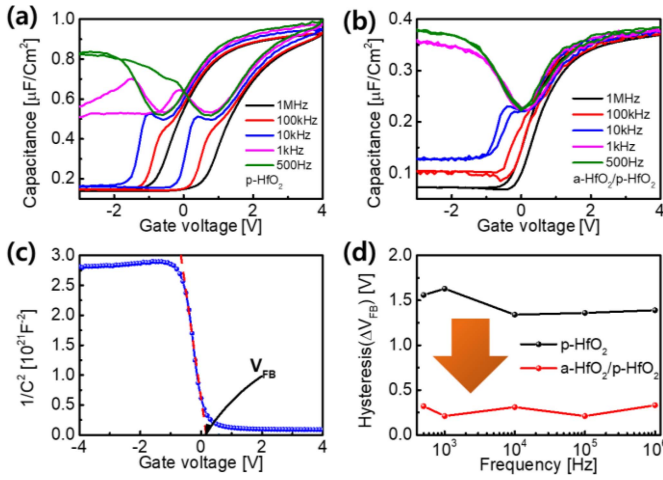
**FIGURE 3.** Frequency dependent C-V characteristics of Ge MOSCAPs with (a) p-HfO<sub>2</sub> monolayer and (b) p-HfO<sub>2</sub>/a-HfO<sub>2</sub> bilayer gate dielectric.

semiconductor parameter analyzer, respectively. Structural analysis was conducted using focused ion-beam (FIB)-SEM and transmission electron microscopy (TEM, JEOL JEM-2100F) equipped with an energy-dispersive X-ray spectrometer (EDS).

## III. RESULTS AND DISCUSSION

Fig. 2(a) shows the cross-sectional high-resolution (HR)-TEM image of the p-HfO<sub>2</sub>/a-HfO<sub>2</sub>/Ge (100) interface; The crystallinity of each HfO<sub>2</sub> layer is clearly shown. The p-HfO<sub>2</sub> layer possesses a polycrystalline structure containing multiple grains and boundaries, and an interfacial GeO<sub>x</sub> layer of ~ 0.54 nm is formed on the Ge surface. The inset shows a fast Fourier transform (FFT) micrograph of the HfO<sub>2</sub> grain, clearly indicating its crystallized phase. Fig. 2(b) shows changes of atomic ratio across the interface, and Fig. 2(c) represents the EDS mapping of individual layers, confirming the uniform distribution of elements Ge, Hf, and O. A higher density of Hf atom was observed in p-HfO<sub>2</sub> compared with a-HfO<sub>2</sub> layer.

Figs. 3(a) and (b) show the frequency-dependent C-V curves of the p-HfO<sub>2</sub>/a-HfO<sub>2</sub> and p-HfO<sub>2</sub> Ge MOSCAPs from 500 Hz to 1 MHz, respectively. Stronger inversion and less frequency-dispersion were observed in the p-HfO<sub>2</sub>/a-HfO<sub>2</sub> MOSCAPs due to improved leakage characteristics achieved by a-HfO<sub>2</sub> capping layer [30]. However, a relatively



**FIGURE 4.** Bidirectional C-V characteristics of Ge MOSCAPs with (a) p-HfO<sub>2</sub> monolayer and (b) p-HfO<sub>2</sub>/a-HfO<sub>2</sub> bilayer gate dielectric. (c)  $1/C^2$  vs. gate voltage plot for extracting  $V_{FB}$  through linear fitting. (d) Comparison of extracted hysteresis ( $\Delta V_{FB}$ ) versus frequency.

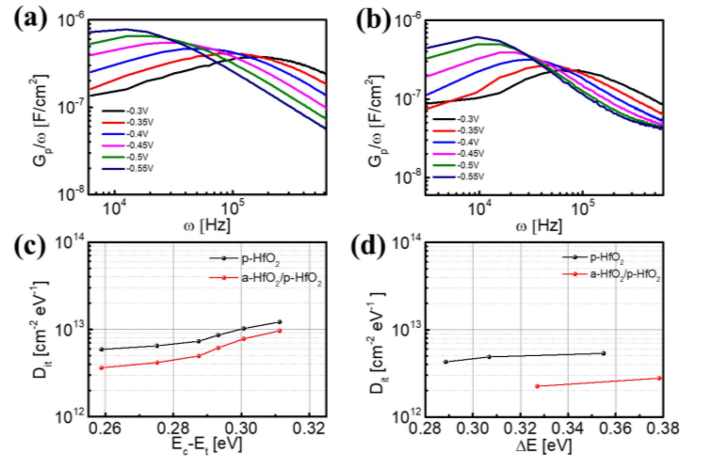
low  $k$  value of  $\sim 9$  was obtained from p-HfO<sub>2</sub>/a-HfO<sub>2</sub> in comparison with  $k \sim 15$  of p-HfO<sub>2</sub> gate dielectric. Further experiments to optimize the thickness ratio between p-HfO<sub>2</sub> and a-HfO<sub>2</sub> layer and ALD process conditions could enhance the  $k$  of p-HfO<sub>2</sub>/a-HfO<sub>2</sub> [31].

Figs. 4(a) and (b) show the frequency-dependent bidirectional C-V curves of the Ge MOSCAPs with p-HfO<sub>2</sub>/a-HfO<sub>2</sub> and p-HfO<sub>2</sub> for the same frequency range of 500 Hz to 1 MHz, respectively. Although the a-HfO<sub>2</sub> layer contains various oxide defects inducing non-ideal C-V properties, p-HfO<sub>2</sub> capped by a-HfO<sub>2</sub> layer (i.e., p-HfO<sub>2</sub>/a-HfO<sub>2</sub>) exhibits significant reduction of hysteresis ( $\Delta V_{FB}$ ) as well as dispersion. In order to describe the effect of a-HfO<sub>2</sub> capping layer on  $\Delta V_{FB}$  quantitatively, the  $V_{FB}$  is determined through the extrapolated line of  $1/C^2 - V_{GS}$  in the depletion region as shown in Fig. 4(c) exhibiting  $V_{FB}$  of 0.32 V.  $\Delta V_{FB}$  is calculated to be difference of  $V_{FB}$  under bi-directional bias sweep C-V measurements, and Fig. 4(d) compares the hysteresis ( $\Delta V_{FB}$ ) as a function of frequency. The average  $\Delta V_{FB}$  of p-HfO<sub>2</sub>/a-HfO<sub>2</sub> and p-HfO<sub>2</sub> was 0.28 V and 1.46 V, respectively. Therefore, the additional a-HfO<sub>2</sub> layer deposited on p-HfO<sub>2</sub> results in the reduction of  $V_{FB}$  by  $\sim 1.18$  V, and exhibits lower  $\Delta V_{FB}$  in comparison with the reported value of a Ge gate stack with a-HfO<sub>2</sub> layer [32].

Next, Hi-Lo and conductance methods were used to investigate  $D_{it}$  at the interface. The ac conductance ( $G_m$ ) and capacitance ( $C_m$ ) of the MOSCAPs were measured at various gate biases. Based on the measured  $G_m$ , the normalized equivalent parallel conductance is calculated using [28], [29]:

$$\frac{G_p}{\omega} = \frac{C^2 \omega G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \quad (1)$$

where  $C_{OX}$  is the oxide capacitance measured in accumulation region and  $\omega$  is the angular frequency. Figs. 5(a) and (b) show the extracted equivalent conductance ( $G_p$ ) versus measurement frequency ( $\omega$ ) for both MOSCAPs. The



**FIGURE 5.** Normalized equivalent conductance spectrum at various gate bias derived from conductance measurements for (a) p-HfO<sub>2</sub> and (b) p-HfO<sub>2</sub>/a-HfO<sub>2</sub>. Interface trap density ( $D_{it}$ ) versus  $\Delta E$  calculated from (c) conductance method and (d) Hi-Lo method.

peaks correspond to interface states' response, and their positions were modulated by the gate bias. From the conductance peak,  $D_{it}$  was extracted using [33], [34],

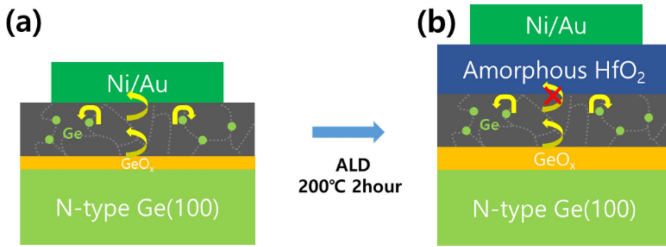
$$D_{it} = \frac{2.5}{Aq} \left( \frac{G_p}{\omega} \right)_{peak}, \quad (2)$$

where  $A$  is the area of devices. Fig. 5(c) shows the calculated  $D_{it}$  as a function of  $\Delta E$  which is the energy difference between trap level ( $E_T$ ) and conduction band edge ( $E_C$ ). The  $D_{it}$  of p-HfO<sub>2</sub> and p-HfO<sub>2</sub>/a-HfO<sub>2</sub> were extracted to be  $6.0 \times 10^{12}$  and  $3.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , respectively, at  $\Delta E = 0.26 \text{ eV}$ ;  $D_{it}$  from p-HfO<sub>2</sub>/a-HfO<sub>2</sub> was lower than that of p-HfO<sub>2</sub>. Because the conductance method could overestimate  $D_{it}$  due to the minority carrier responses in the weak inversion and provide  $D_{it}$  values only over the limited energy range [35], [36], we further investigated the  $D_{it}$  using the Hi-Lo method and  $D_{it}$  was calculated from Figs. 3(a) and (b) using

$$D_{it}(V_g) = \left( \frac{C_{OX} C_{LF}}{C_{OX} - C_{LF}} - \frac{C_{OX} C_{HF}}{C_{OX} - C_{HF}} \right) / qA, \quad (3)$$

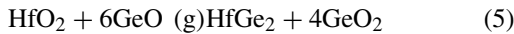
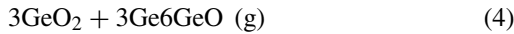
where  $A$  is the area,  $C_{LF}$  and  $C_{HF}$  is the capacitance at low and high frequency, respectively [33], [37]. The p-HfO<sub>2</sub>/a-HfO<sub>2</sub> also exhibits reduced  $D_{it}$  of  $2.0 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  compared with p-HfO<sub>2</sub> of  $4.0 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . The reduced hysteretic behaviors and improved interface states of Ge MOSCAPs with the p-HfO<sub>2</sub>/a-HfO<sub>2</sub> dielectric can be attributed not only to capping effects of the p-HfO<sub>2</sub> surface by the a-HfO<sub>2</sub> layer but the post-oxidation at the interface between p-HfO<sub>2</sub> and Ge during ALD deposition process [12], [38]. Although the ALD temperature ( $\sim 200 \text{ }^\circ\text{C}$ ) of a-HfO<sub>2</sub> was relatively low, thermal diffusion of oxygen can proceed and the oxidation at the interface is speculated to be involved [16].

Fig. 6 shows a schematic illustration of the a-HfO<sub>2</sub> capping effect on p-HfO<sub>2</sub>/GeO<sub>x</sub>/Ge stack. Although the p-HfO<sub>2</sub>



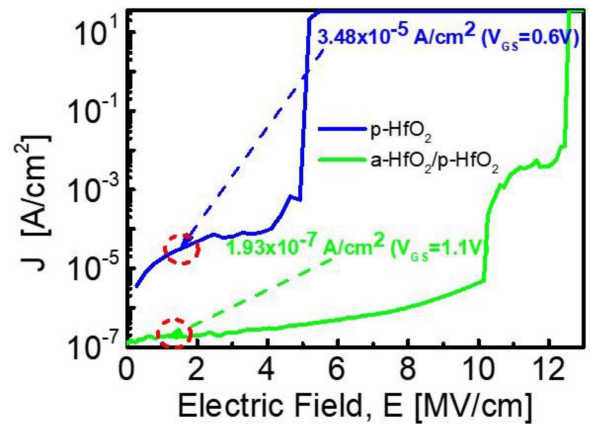
**FIGURE 6.** Schematic illustration of the reactions occurring within the Ge MOSCAPs with (a) p-HfO<sub>2</sub> and (b) p-HfO<sub>2</sub>/a-HfO<sub>2</sub> stack. The a-HfO<sub>2</sub> capping layer and post-oxidation at the interface during ALD a-HfO<sub>2</sub> process (200 °C, 2 hours) suppress the diffusion of Ge atoms through grain boundaries and passivate leakage paths.

monolayer provides a relatively higher  $k$  of  $\sim 15$ , the incorporation of Ge atoms into p-HfO<sub>2</sub> and their diffusion within the layer are known to be the origin of poor electrical characteristics [1], [18]. Even worse, the GeO (g) is known to trigger metal-Ge (HfGe<sub>2</sub>) generation playing a role of leakage current paths as shown in the following reactions [1],



As shown in Fig. 6(a), the diffusion of Ge atoms into the p-HfO<sub>2</sub> through grain boundaries induces larger hysteresis as well as higher  $D_{it}$ . In order to confine the Ge diffusion within the p-HfO<sub>2</sub>, the a-HfO<sub>2</sub> capping layer is deposited as shown in Fig. 6(b). Although other amorphous high- $k$  films can be applied as a capping layer, it is reported that the interface dipoles at the boundary of different oxide layers can cause additional hysteresis [28], [29]. Even compared with the direct diffusion of Ge atoms into the a-HfO<sub>2</sub> gate-dielectric, the proposed p-HfO<sub>2</sub>/a-HfO<sub>2</sub> dielectric shows better interface quality [32]. Therefore, the proposed p-HfO<sub>2</sub> dielectric capped by a-HfO<sub>2</sub> can exhibit improvement of interface quality and reduction of leakage current. Moreover, the consecutive ALD deposition of polycrystalline and amorphous HfO<sub>2</sub> at different temperature can simplify the gate-oxide deposition process. It is to be noted that the results can be limited because the reference p-HfO<sub>2</sub> dielectric did not adopt high-quality GeO<sub>2</sub> or passivation layer using additional processes. At the same time, it can be further improved by adopting thin Al<sub>2</sub>O<sub>3</sub> interlayer and/or additional pre-/post-oxidation of GeO<sub>x</sub> [21], [26], [27]. In particular, considering the thermal budget for BEOL-M3D integration, the plasma postoxidation method might be preferred [21], [39].

Furthermore, the proposed graded HfO<sub>2</sub> gate dielectric layer can yield significantly improved leakage current and breakdown characteristics. Fig. 7 shows the gate leakage current density ( $J$ ) vs. oxide electric field ( $E_{OX}$ ) of the measured devices; An equivalent oxide thickness (EOT) was used for calculating  $E_{OX}$ . At the same effective  $V_G$  bias condition of  $V_{FB} + 1$  V, the  $J$  of p-HfO<sub>2</sub> and p-HfO<sub>2</sub>/a-HfO<sub>2</sub> was  $3.47 \times 10^{-5}$  A/cm<sup>2</sup> and  $1.93 \times 10^{-7}$  A/cm<sup>2</sup>, respectively. This suppressed leakage current can be attained by



**FIGURE 7.** Current density ( $J$ ) versus oxide electric field ( $E_{OX}$ ) curves of the Ge MOSCAPs showing p-HfO<sub>2</sub>/a-HfO<sub>2</sub> stack exhibits reduced leakage current and improved breakdown characteristics compared with p-HfO<sub>2</sub>.

eliminating leakage paths. Regarding the breakdown  $E_{OX}$ , p-HfO<sub>2</sub>/a-HfO<sub>2</sub> exhibits  $4.9 \times 10^{-6}$  A/cm<sup>2</sup> at 4.4 MV/cm, and p-HfO<sub>2</sub> shows  $1.0 \times 10^{-4}$  A/cm<sup>2</sup> at 1.0 MV/cm. The p-HfO<sub>2</sub>/a-HfO<sub>2</sub> exhibits significantly lower  $J$  ( $< 100 \times$ ) and better breakdown characteristics ( $> 4 \times$ ) compared with p-HfO<sub>2</sub>, attributed to the aforementioned capping effect of the a-HfO<sub>2</sub>.

#### IV. CONCLUSION

In summary, we proposed and investigated p-HfO<sub>2</sub>/a-HfO<sub>2</sub> gate dielectric for n-Ge MOSCAPs in comparison with p-HfO<sub>2</sub> dielectric. The crystallinity of each HfO<sub>2</sub> layer and interfacial GeO<sub>x</sub> layer were confirmed by HR-TEM. Although the p-HfO<sub>2</sub>/a-HfO<sub>2</sub> has a lower dielectric constant ( $k \sim 9$ ) than that ( $k \sim 15$ ) of p-HfO<sub>2</sub>, it showed a reduced hysteresis ( $\Delta V_{FB}$ ) by the amount of  $\sim 1.3$  V. The  $k$  is expected to be increased by optimizing the thickness ratio. Both Hi-Lo and conductance methods were used to evaluate the interface state.  $D_{it}$  of p-HfO<sub>2</sub>/a-HfO<sub>2</sub> and p-HfO<sub>2</sub> were extracted to be  $6.0 \times 10^{12}$  and  $3.5 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup>, respectively, at  $\Delta E = 0.26$  eV. Similar level of difference ( $\sim 2.0 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup>) was obtained from the Hi-Lo method. These reduced hysteresis and improved interface quality can be attributed to the effect of surface capping by the a-HfO<sub>2</sub> layer and additional post-oxidation at the interface between p-HfO<sub>2</sub> and GeO<sub>x</sub>/Ge substrate during ALD a-HfO<sub>2</sub> deposition. Moreover, the diffused Ge atoms through the grain boundaries were speculated to be confined within p-HfO<sub>2</sub> layer by a-HfO<sub>2</sub> capping layer. Consequently, a-HfO<sub>2</sub> could suppress leakage current paths, and thus significantly reduced leakage  $J$  of  $1.93 \times 10^{-7}$  A/cm<sup>2</sup> was obtained from the p-HfO<sub>2</sub>/a-HfO<sub>2</sub> compared with  $3.47 \times 10^{-5}$  A/cm<sup>2</sup> from the p-HfO<sub>2</sub> at the bias of  $V_{FB} + 1$  V. These results show that the p-HfO<sub>2</sub> with consecutively deposited a-HfO<sub>2</sub> capping layer can be a promising gate stack for Ge devices.

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