Received 31 December 2020; accepted 31 January 2021. Date of publication 5 February 2021; date of current version 26 February 2021.
The review of this article was arranged by Editor M. J. Kumar.

Digital Object Identifier 10.1109/JEDS.2021.3057456

Low-Power Vertical Tunnel Field-Effect Transistor Ternary Inverter

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This work was supported in part by the Brain Korea 21 Plus Project in 2021; in part by the Future Semiconductor Device Technology Development Program under Grant 10067739 and Grant 20010847 funded by Ministry of Trade, Industry and Energy (MOTIE); in part by Korea Semiconductor Research Consortium (KSRC); in part by the National Research Foundation (NRF) funded by the Korean Ministry of Science; in part by ICT under Grant 2020M3F3A2A01081670, Grant 2020M3F3A2A01081666, and Grant 2020R1A2C2103059; and in part by Synopsys Inc.

ABSTRACT In this study, vertical tunnel FET-based ternary CMOS (T-CMOS) is introduced and its electrical characteristics are investigated using TCAD device and mixed-mode simulations with experimentally calibrated tunneling parameters. This new T-CMOS utilizes two different types of tunneling currents to form three different output voltage states: (1) source-to-drain tunneling current; and (2) conventional source-to-channel tunneling current. To form a half supply voltage (V_{DD}) output voltage during the inverter operation, the n-/p-type devices of the proposed T-CMOS are designed to have constant source-to-drain tunneling current regardless of gate voltage (V_{GS}) by using nitride spacer between gate and drain. Also, typical binary inverter operation is performed using the source-to-channel tunneling. In voltage transfer characteristics (VTC), it is confirmed that there is the clear half V_{DD} state after matching the tunneling currents of the n-/p-type devices. It is revealed that the stable half V_{DD} state cannot be achievable if the currents are mismatched by gate workfunction, gate dielectric thickness, and interface trap variations, implying that the current matching between n-/p-type devices is crucial to obtain stable ternary operations.

INDEX TERMS Band-to-band tunneling (BTBT), vertical tunnel field-effect transistor (vertical tunnel FET), ternary inverter, subthreshold swing (SS), ternary CMOS (T-CMOS), line tunneling.

I. INTRODUCTION

Over the past several decades, CMOS dimensions have been continuously scaled down to make switching speed faster and integration density increasing in accordance with Moore's Law [1]. At the same time, power consumption has been rapidly increased due to high leakage current such as off-state leakage current by short-channel effects (SCEs), gate leakage current, and junction leakage current while CMOS technology node becomes smaller [2], [3]. Beyond sub-22nm node, especially, it is not easy to handle supply voltage (V_{DD}) scaling for low operating power devices [4]. Thus, in order to realize the continuous V_{DD} scaling, steep subthreshold swing (SS) devices such as impact-ionization FET (I-MOS), tunnel FET, and negative capacitance FET (NCFET), which make low V_{DD} operations possible, have been extensively studied [5]–[21].

As one of the candidates, tunnel FET can have SS of sub-60 mV/dec because it uses band-to-band tunneling (BTBT) as a carrier injection mechanism as contrast to MOSFETs which have SS limitation (> 60 mV/dec) by thermionic emission at room temperature. Moreover, typical n-type tunnel FET consists of p-type source, intrinsic channel, and n-type drain and thus it is compatible with conventional MOSFET process since only source dopant type is changed. Although tunnel FETs have low on-current by high tunneling resistance between source and channel, many researchers have extensively studied how to design it to boost on-current using various low bandgap materials

and process techniques that are able to improve tunneling probabilities [22]–[24].

Recently, to overcome V_{DD} and power scaling limitations of conventional CMOS circuits, human brain mimic systems, which have maximized parallelism with low-frequency processing, has been proposed for low-power artificial neural network applications [25], [26]. Particularly, neuromorphic systems on chips based on binary CMOS have been demonstrated by using parallelized neuro synaptic cores and spiking neural networks with low-frequency operations. Furthermore, for the significant increase of information density, the wafer-level integrated ternary CMOS (T-CMOS) using tunneling has been successfully reported and the possibility for the mass production of the T-CMOS neuromorphic system has been presented [27]. These ternary logics can reduce the number of transistors as compared to binary logics [28]. However, since the ternary state are implemented by the tunneling mechanism, the switching speed of the ternary inverters is relatively too slow compared to the conventional binary inverters. Nevertheless, the T-CMOS can operate a single comparator with two internal references in a 1.5 bit stage of a pipelined analogue-to-digital converter (ADC) [27]. As ADCs are necessary for integrated circuit designs, in the neuromorphic system which works at a low operating frequency (∼1kHz) [25], [26], it is expected that the ternary inverter can enhance the computation density as contrast to the binary inverter.

In this work, the new T-CMOS with vertical fin structure (T-CMOS$_{VF}$) is proposed. In contrast to the previously reported T-CMOSs [27], [29], the proposed T-CMOS$_{VF}$ uses only BTBT mechanism to form three output voltage (V_{OUT}) states. Thus, it can be operated at the lower V_{DD} by the steeper subthreshold swing than other MOSFET-based ternary inverters. For the T-CMOS$_{VF}$, silicon-germanium (SiGe) is used for source/channel/drain regions and line-tunneling between source and channel are adapted to obtain high on-current with small tunneling resistance. In addition, the process integration for the T-CMOS$_{VF}$ is introduced in terms of the fabrication feasibility.

II. DEVICE STRUCTURE AND PARAMETERS

Fig. 1(a) shows the device structure of the proposed T-CMOS$_{VF}$ used in this simulation study. The proposed device has the double gates and SiGe materials excluding the substrate, which can improve the gate controllability on the channel and enhance the tunneling current drivability simultaneously.

The idea to be implemented for ternary inverter operations is to use BTBT generated at source-to-channel and source-to-drain. In conventional tunnel FETs, it has been reported that only the source-to-channel tunneling contributes to on-current related to switching characteristics, whereas channel-to-drain tunneling (ambipolar current) is considered to be suppressed as leakage current [30]. In contrast, as illustrated in Fig. 1(b), the T-CMOS$_{VF}$ is utilizing both

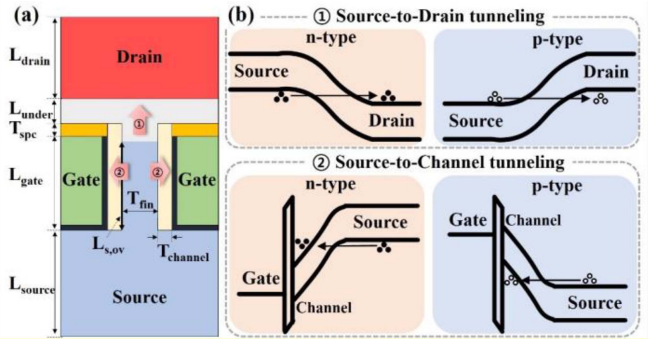

FIGURE 1. (a) The schematic image of the new T-CMOS device based on the vertical tunnel FET which has two current paths: (1) source-to-drain tunneling and (2) source-to-channel tunneling. (b) Energy band diagrams for n-/p-type devices are illustrated to explain the mechanism for each current flow.

source-to-channel tunneling for typical binary V_{OUT} formation and source-to-drain tunneling which makes additional third V_{OUT} by flowing gate voltage (V_{GS})-independent constant tunneling current in n-/p-type devices. For the constant source-to-drain tunneling current, the part of the source region close to the drain is intentionally underlapped by forming the nitride spacer to make the region uncontrollable by V_{GS}.

All the device evaluations are performed by Synopsys Sentaurus^{TM} (Synopsys, Mountain View, CA, USA) [31]. To analyze the T-CMOS$_{VF}$, gate length (38 nm), equivalent oxide thickness (1 nm), and channel thickness (5 nm) are adapted respectively. Also, 20% Ge content is applied to achieve the smaller tunneling resistance than silicon and the feasibility of process integration. Growing single-crystalline SiGe on Si wafer is quite difficult due to threading dislocations which induce huge amount of traps. Considering the critical thickness for SiGe with more than 30% Ge contents [32], the thickness of epitaxially-grown SiGe film is only allowed less than 30 nm to obtain high quality SiGe material without dislocations. However, over 100 nm high quality SiGe film is achievable with Ge contents below 20%. Hence, 20% Ge content is adapted by considering the total SiGe thickness (100 nm) of the proposed devices. In addition, 35 nm of source overlap length (gate-to-source overlapped region) and 15 nm of fin thickness are applied. The drain is 10 nm underlapped for constant source-to-drain tunneling. Other detailed parameters used in the TCAD simulations are listed in Table 1.

For accuracy analysis on tunneling current, the dynamic nonlocal BTBT model is activated in the whole regions and the tunneling model is calibrated to experimental data for the planar Si/SiGe (20% Ge) TFETs. The planar TFET with width/length = 400/400 nm was fabricated on a (100) p-type bulk Si wafer. The TFET has 200 nm polycrystalline silicon gate electrode and 3 nm SiO_2 gate dielectric. After gate patterning, source and drain regions were defined by implantation process. Source and drain implantations are performed separately to inject the different types of dopants. BF_2 with

TABLE 1. Physical parameters of proposed ternary device.

Symbol	Quantity	Value
L_{gate}	Gate Length	38 nm
L_{under}	Drain Underlap	10 nm
L_{source}	Source Length	30 nm
L_{drain}	Drain Length	18 nm
$L_{s.ov}$	Source Overlap	35 nm
T_{ox}	Equivalent Oxide Thickness	1 nm
T_{spc}	Spacer Thickness	4 nm
T_{fin}	Fin Thickness	15 nm
$T_{channel}$	Channel Thickness	5 nm
$N_{channel}$	Channel Conc.	1×10^{15} cm^{-3}
N_{source}	Source Conc.	1×10^{20} cm^{-3}
N_{drain} (n/p)	Drain Conc.	3.0×10^{18} / 2.8×10^{18} cm^{-3}
N_{under}	Drain Underlap Conc.	1×10^{15} cm^{-3}
ε	Dielectric Constant (Ge 20%)	12.6
E_g	Bandgap (Ge 20%)	1.03 eV
WF (n/p)	Workfunction	4.08 / 5.0 eV

dose of 8×10^{14} cm^{-2}, 7° tilt, and energy of 10 keV was used for source implantation. As with the same condition is implanted into drain. Subsequently, dopants are activated by rapid thermal process (RTP) at 900 °C during 5s.

To calculate BTBT generation rate (G) per unit volume in the uniform electric field, Kane's model is used (Eq. 1) and fitted parameters from Figs. 2(a) and (b) are as follows.

$$G = A(\frac{F}{F_0})^P \exp(-\frac{B}{F}) \quad (1)$$

where F_0 = 1 V/m, P = 2.5 for indirect BTBT, A_{SiGe} = 6.5×10^{15} cm^{-3}·s^{-1}, and B_{SiGe} = 8.1×10^6 V/cm are the Kane's parameters of the experimentally calibrated SiGe materials and F is the electric-field. Furthermore, Slotboom model is adapted to consider the impact of heavy doping on bandgap narrowing. Fermi statistics, drift-diffusion, and Shockley-Read-Hall (SRH) recombination model are used. For the SRH recombination, the interpolated SRH parameters between Si and Ge parameters are applied [33]. Also, to match the currents, the workfucntions for n-/p-type devices are used with 4.08 eV and 5.0 eV, respectively. The mixed-mode simulations are performed with n-/p-type devices and a load capacitor of 5×10^{-16} F to analyze the circuit (inverter) characteristics based on physical models. However, gate leakage current is ignored because this study is mainly focused on the effects of ternary inverter operation.

III. ANALYSIS ON TERNARY OPERATION

Fig. 3(a) shows the transfer characteristics of the proposed n-/p-type devices at V_{DS} = 0.6 V. As above-mentioned, the T-CMOS$_{VF}$ device is designed to utilize BTBT currents generated at different locations with respect to V_{GS}. Below V_{GS} = 0.4 V, the I_{DS} is dominantly composed of source-to-drain tunneling which is slightly increased by the change of V_{GS}. When V_{GS} reaches to ~ 0.4 V, where the valence energy band of the source and the conduction energy band of the channel are aligned, source-to-channel tunneling current additionally starts to flow, resulting in abrupt I_{DS} increase.

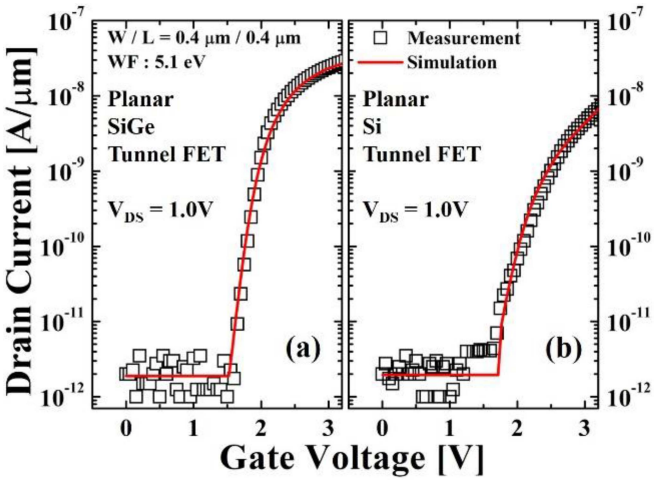

FIGURE 2. Calibration of BTBT parameters from measurements and TCAD simulations for planar (a) SiGe tunnel FET and (b) Si tunnel FET's transfer characteristics. Dynamic nonlocal tunneling model is used for the simulations.

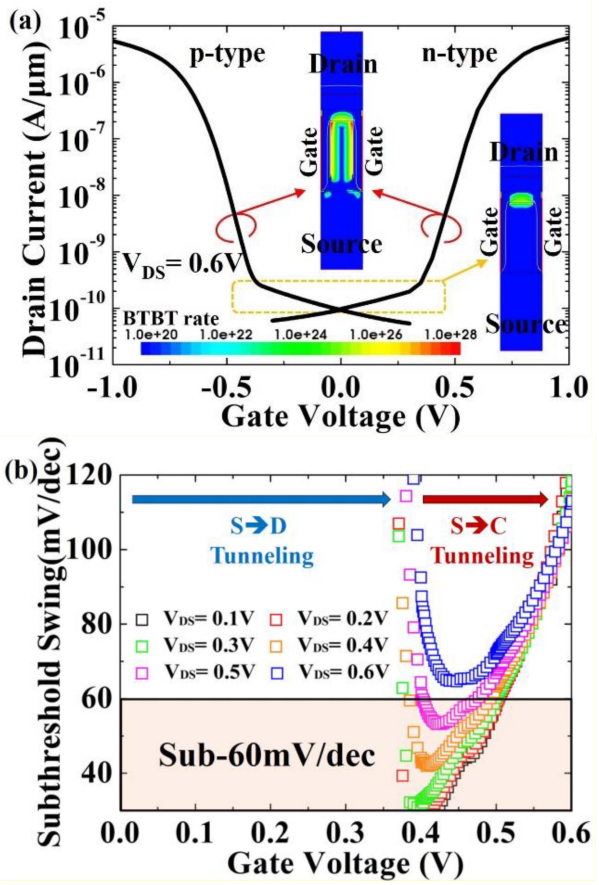

FIGURE 3. (a) Transfer characteristics on the T-CMOS$_{VF}$ for n-/p-type devices with source-to-drain and source-to-channel tunneling currents. The insets show 2D BTBT generation rate contours with respect to V_{GS}. (b) For n-type device, the extracted SS values depending on I_{DS} at V_{DS} = 0.1~0.6 V.

SS of sub-60 mV/dec can be achieved since the current is generated by BTBT mechanism rather than thermal injection [Fig. 3(b)]. Interestingly, the peak value of BTBT rate

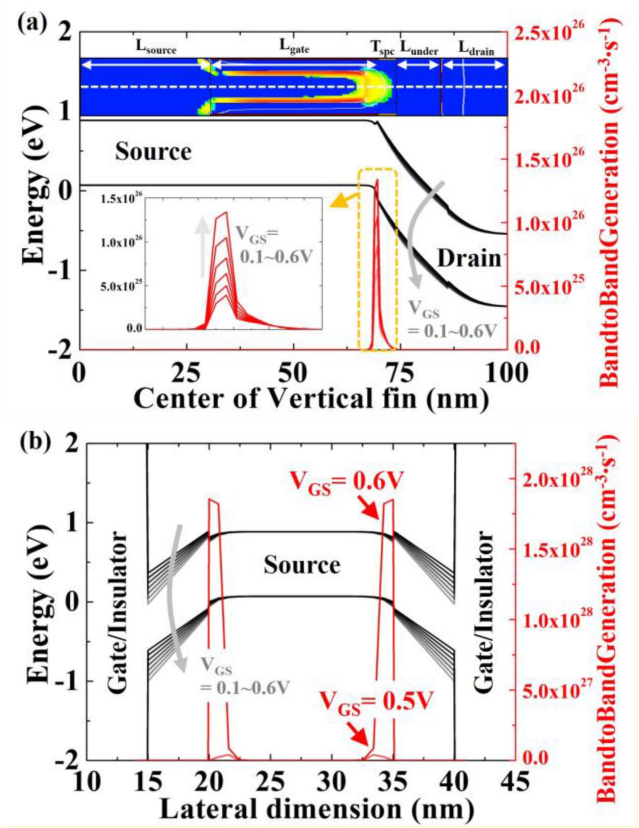

FIGURE 4. Energy band diagrams and BTBT generation rates along with (a) source-to-drain direction at the center of the vertical fin and (b) channel-to-source direction at a half Lg. Energy band diagrams and BTBT generation rates are extracted with respect to V_{GS} at V_{DS} = 0.6 V.

is observed near the gate edge toward the drain side because the T-CMOS$_{VF}$ utilizes line-tunneling [34] as contrast to the conventional TFETs which have the peak BTBT rate at the source-gate edge.

To investigate each tunneling current occurring at different locations and V_{GS}s in detail, energy band diagrams are specifically analyzed as shown in Fig. 4. First, in the entire V_{GS} range, source-to-drain tunneling barrier width is slightly changed so that almost constant BTBT is generated at the junction between source and drain as can be seen in Fig. 4(a). This is because nitride spacer between gate and drain prevents the gate from controlling the source-to-drain junction. Thus, in an inverter, as n-/p-type devices are operated in the V_{GS} range where only source-to-drain tunneling occurs, V_{OUT} is determined by the resistance difference between them as a voltage divider and the V_{OUT} with a stable third half V_{DD} state (V_{3rd}) can be formed if both the devices have the equivalent tunneling current. If the source-to-drain tunneling current is meaningfully changed by V_{GS}, it is impossible to form the stable V_{3rd} because the V_{3rd} cannot be sustained and thus V_{OUT} is converged to 0 V or V_{DD} by the V_{GS}-induced I_{DS} changes of the n-/p-type devices with the opposite direction. Beyond V_{GS} = 0.4 V, source-to-channel tunneling starts to increase abruptly. This can be understood by confirming energy band diagram in the normal direction to the channel. Fig. 4(b) shows that the source-to-channel vertical tunneling start to occur abruptly over V_{GS} = 0.4 V where the source-to-channel tunneling barrier become narrow enough to generate BTBT. Note that the bandgap discontinuity between the source and the channel results from the different bandgap narrowing by the different dopants concentrations.

Fig. 5(a) illustrates the voltage transfer characteristics (VTC) evaluated from the optimized T-CMOS$_{VF}$ at V_{DD} = 0.6 V. The half V_{DD} state is clearly shown between conventional binary V_{OUT} states. The ternary CMOS operation for the T-CMOS$_{VF}$ can be explained as follows. When the input voltage (V_{IN}) of the T-CMOS$_{VF}$ starts to make a transition from 0 V to V_{DD} (below V_{IN} = 0.2 V), p-type device is in saturation region (on-current region) while n-type device is in flat off-state region (source-to-drain tunneling region), resulting in $V_{OUT} \approx V_{DD}$. Then, as V_{IN} goes up continuously and reaches to V_{IN} = 0.2 V, both p-type and n-type devices enter and stay in the flat off-state region until source-to-channel tunneling starts to occur in the n-type device. Thus, V_{OUT} is maintained at a half V_{DD} since both have the similar resistance by the current matching. Beyond V_{IN} = 0.4 V, while the p-type device is still in the flat off-state region, the n-type device operates in the on-current region, leading to $V_{OUT} \approx 0$ V.

In addition, various input step voltages with a peak-to-peak voltage from 0.5 V to 0.7 V are applied to the T-CMOS$_{VF}$ to verify the V_{3rd} dependence on V_{DD}. The inset of Fig. 5(a) indicates that the V_{3rd} (half V_{DD}) is decreased and the V_{3rd} is sustainable in the wider V_{IN} range as V_{DD} becomes reduced. This can be understood by the transfer characteristics with various V_{DS} as described in Fig. 5(b). Here, note that V_{GS} (corresponding to V_{IN}) is swept from 0 V to V_{DD} by swapping drain voltage and source voltage for the I_{DS}-V_{GS} curves of the p-type device to intuitively confirm the V_{IN} margin for the V_{3rd} in the T-CMOS$_{VF}$ inverter operations. Fig. 5(b) shows that the V_{3rd} window becomes reduced as V_{DS}, which corresponds to the V_{3rd} in the T-CMOS$_{VF}$ inverter, increases. Therefore, the 0.6 V of input voltage is required to secure the stable V_{IN} margins for the output voltages (0 V, V_{DD}, and V_{3rd}). For both conventional MOSFETs and TFETs, it is hard to achieve V_{IN} < 0.4 V operations because overdrive voltage (V_{OV}= V_{GS}-V_{TH}) of at least > 0.3 V is required to obtain sufficient on-current. Considering that the T-CMOS$_{VF}$ is intentionally designed to have the wide flat leakage current region regardless of V_{GS} before source-to-channel tunneling occurs at V_{GS} > 0.4V, it is remarkable that the proposed device can be operated at V_{IN} = 0.6 V, which is the lower operation voltage than that of the previous T-CMOS with V_{IN} > 1V for the proper ternary operations [27]. However, the T-CMOS$_{VF}$ might be susceptible to noise since the output node is connected to V_{DD} through a very high-resistance path. Thus, the T-CMOS$_{VF}$ should be carefully designed for the V_{3rd} implementation.

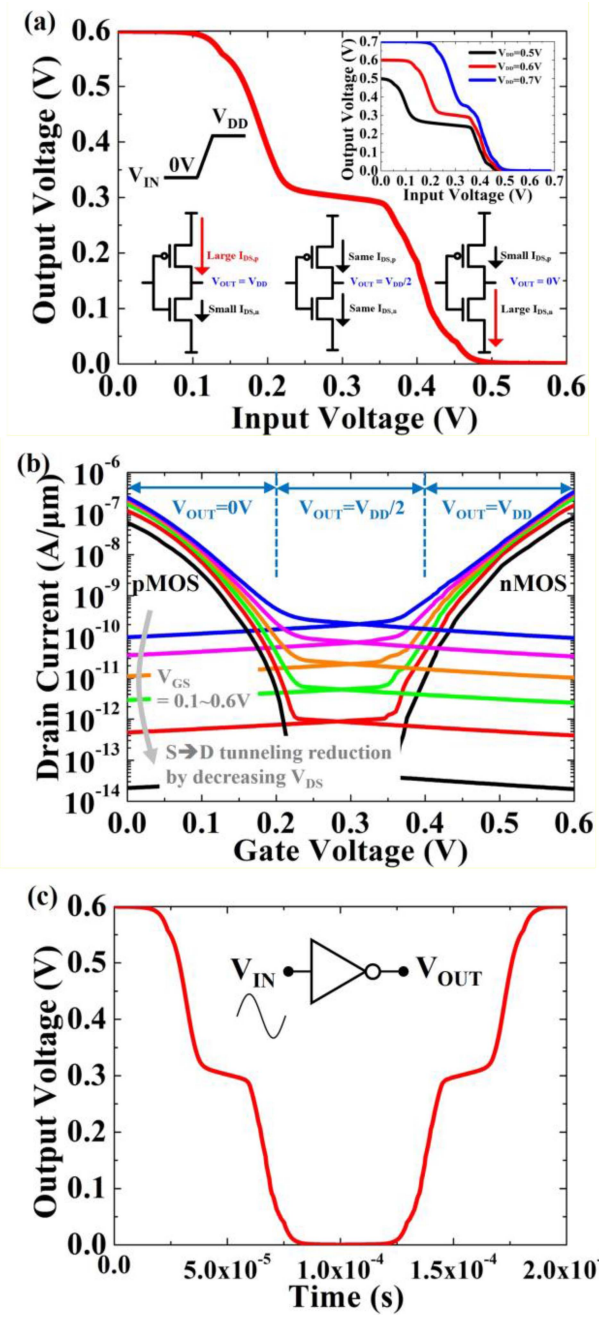

FIGURE 5. **(a) Voltage transfer characteristics of the T-CMOS$_{VF}$ device at V_{DD} = 0.6 V (In the inset, VTC for various input step voltages from 0.5 V to 0.7 V are evaluated). (b) Transfer characteristics of n-/p-type devices with respect to V_{DS} to verify V_{IN} window of each voltage state (V_{DD}/0.5V_{DD}/0V). (c) Transient response of the T-CMOS$_{VF}$ at V_{DD} = 0.6V.**

In terms of the delay comparison between the T-CMOS$_{VF}$ and the conventional T-CMOS, the T-CMOS$_{VF}$ have almost the same (V_{DD} -> V_{3rd}) and (0 V -> V_{3rd}) switching delay as the conventional T-CMOS because both the devices use the similar BTBT current for the switching. However, it is easily expected that the conventional T-CMOS can have the faster (V_{3rd} -> V_{DD}) and (V_{3rd} -> 0 V) switching since the switching speeds are strongly related to the driving current (on-current) of n-/p-type transistors and the I_{DS} of the

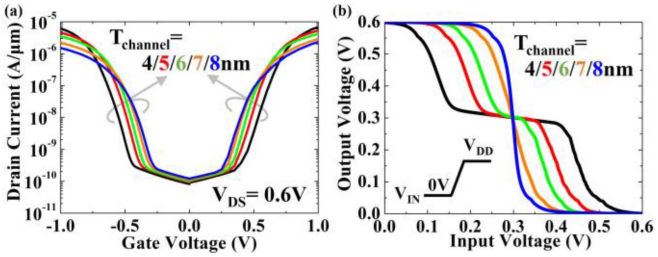

FIGURE 6. **Changes of (a) transfer characteristics and (b) voltage transfer characteristics by channel thickness variations (from 4 nm to 8 nm).**

T-CMOS$_{VF}$ is relatively low compared to the conventional T-CMOS. Fortunately, considering the much lower current level of the BTBT compared to the on-current, the (V_{DD} -> V_{3rd}) and (0 V -> V_{3rd}) transitions are a lot slower and thus the entire switching delay in the ternary operation is limited by the switching toward V_{3rd}. For better understanding, Fig. 5(c) shows the transient response of the T-CMOS$_{VF}$ at V_{DD} = 0.6 V. However, the ternary inverter is not for logic applications, but for parallel neural network systems with a low operating frequency [35]. In addition, the power dissipation of the ternary inverter becomes inevitably increased as compared to the binary inverter because the source-to-drain tunneling current continuously flows during the V_{3rd} formation. However, ternary inverters can decrease the number of transistors by designing ternary arithmetic circuits compared to binary logics and thereby power consumption can be reduced despite of the power dissipation by the third state formation.

IV. OPTIMIZATION OF DEVICE STRUCTURE

In this section, the effects of various device structure parameters on the electrical characteristics of the T-CMOS$_{VF}$ are investigated to optimize the ternary operation. For the simulations, the physical parameters of Table 1 are used except for the variable parameter.

A. CHANNEL THICKNESS

For the proposed T-CMOS$_{VF}$, the line tunneling is adapted for the tunneling current enhancement. The tunneling current can be significantly modulated by $T_{channel}$. Hence, the effects of $T_{channel}$ are confirmed. Fig. 6(a) shows that the turn-on voltage for the source-to-channel tunneling gets reduced and the on-current becomes decreased as $T_{channel}$ is increased. This phenomenon can be explained by the channel surface potential and the electric field across the channel with respect to $T_{channel}$. As $T_{channel}$ is thinner, the tunneling width is reduced and the electric field across the channel is enhanced although the surface potential is decreased by the increased channel capacitance [36]. However, the band-alignment for the BTBT generation occurs at the larger V_{GS} with the thinner $T_{channel}$ since the band-bending is limited by $T_{channel}$ [36]. Thus, the thinner $T_{channel}$ induces the tunneling current enhancement and the increased turn-on voltage. For the VTC characteristics, the VTC starts to be changed toward

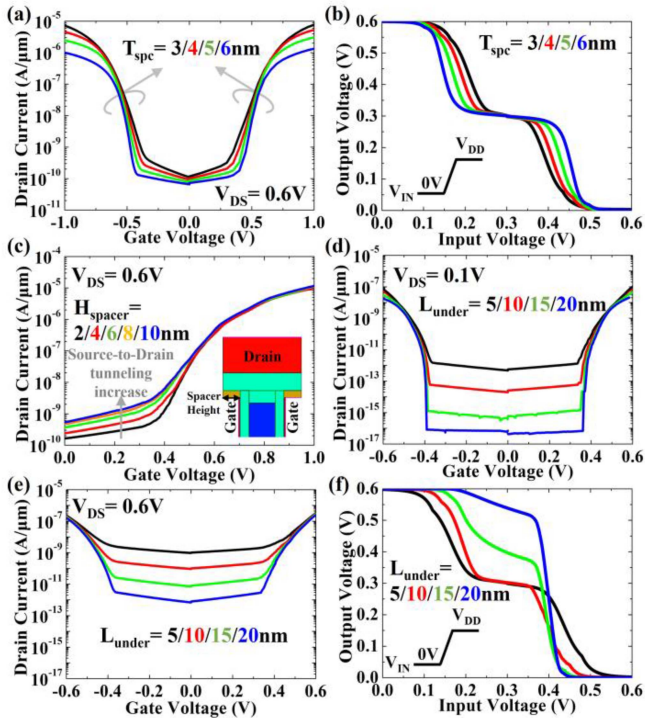

FIGURE 7. For nitride spacer thickness variations (3 nm to 6 nm), changes of (a) transfer characteristics and (b) voltage transfer characteristics. (c) changes of transfer characteristics by spacer height variations to evaluate fringing field effects. For drain underlap length (5 nm to 20 nm), change of transfer characteristics at (d) V_{DS}= 0.1 V and (e) V_{DS}= 0.6 V and (f) changes of voltage transfer characteristics.

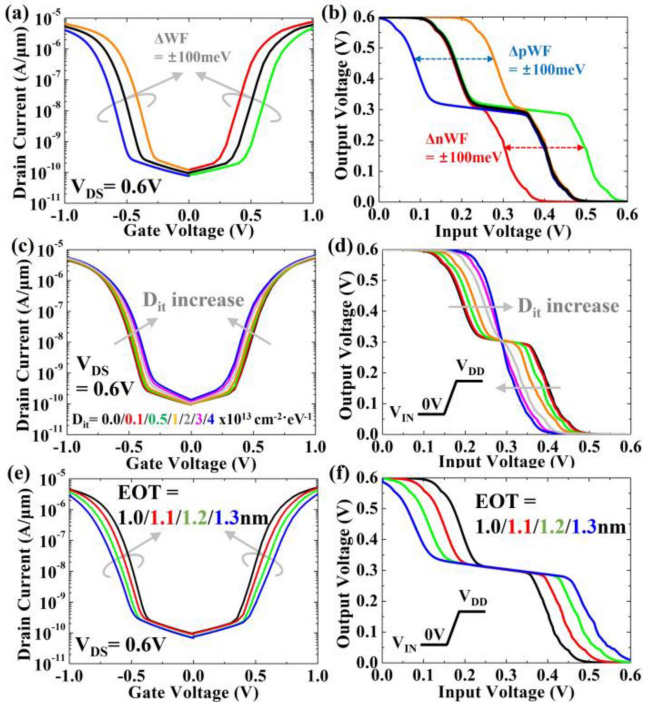

FIGURE 8. For n-/p-type gate WF variations (-100 meV to +100 meV), changes of (a) transfer characteristics and (b) voltage transfer characteristics. Also, for interface trap density variations (0 $cm^{-2}eV^{-1}$ to $4x10^{13}$ $cm^{-2}eV^{-1}$), changes of (c) transfer characteristics and (d) voltage transfer characteristics. Additionally, by equivalent oxide thickness variations (1.0 nm to 1.3 nm), changes of (e) transfer characteristics and (f) voltage transfer characteristics.

that of typical binary inverters with the thicker $T_{channel}$ whereas the input voltage margin for the output voltages (V_{DD} and 0 V) is reduced with too thin $T_{channel}$. Therefore, 5 nm $T_{channel}$ is selected as the optimized channel thickness by considering the stable V_{3rd} state and the wide input voltage margin.

B. NITRIDE SPACER THICKNESS AND HEIGHT

In the T-CMOS$_{VF}$, the nitride spacer plays a critical role to make the source-to-drain tunneling current uncontrollable by V_{GS}. The effects of T_{spc} on the constant source-to-drain tunneling current is investigated. In the transfer characteristics of Fig. 7(a), as T_{spc} decreases (namely, the closer source to the drain), the source-to-drain tunneling becomes more controllable by V_{GS} and thus the SS is degraded with the enhanced on-current by the increased gate-to-source overlap. Also, as expected, Fig. 7(b) indicates that the V_{3rd} state starts to disappear with the decreased T_{spc} since the source-to-drain tunneling current becomes more dependent on V_{GS}. Moreover, the impact of the spacer height (H_{spc}) is verified. Fig. 7(c) shows that the source-to-drain tunneling current becomes larger by the increased fringing field and the current starts to be saturated from $>$ 8 nm as H_{spc} increases. As similar to the T_{spc} reduction, the increased H_{spc} makes the source-to-drain tunneling more controllable by V_{GS} through the fringing field and the margin for the V_{3rd} state becomes reduced in the consequence. However, fortunately, the undesirable source-to-drain tunneling change by H_{spc} can be controlled by the adjustment of T_{spc}. Thus, T_{spc} and H_{spc} are considered simultaneously for the optimization of the ternary operation.

C. UNDERLAP LENGTH

L_{under}, which affects the source-to-drain tunneling, is also the key device design parameter. As L_{under} increases (5 nm -> 20 nm), the source-to-drain tunneling is continuously decreased by the higher tunneling resistance between the source and the drain as depicted in Figs. 7(d) and (e). Also, the on-/off-current ratio between the on-current and the source-to-drain tunneling current is increased, which causes the steeper output voltage transitions (V_{DD} -> V_{3rd} and V_{3rd} -> 0 V) due to the increased resistance difference between the n-/p-type TFETs [Fig. 7(f)]. However, from $>$ 15 nm L_{under}, the T-CMOS$_{VF}$ cannot play the role as a ternary device because the source-to-drain tunneling cannot be generated at low V_D by too wide L_{under} (namely, too large tunneling resistance) as depicted in Fig. 7(f).

V. VARIATION EFFECTS ON TERNARY OPERATIONS

A. WORKFUNCTION VARIATION

In the T-CMOS$_{VF}$, tunneling current matching between n-/p-type devices is essential for proper ternary operations.

Here, the effects of threshold voltage (V_{TH}) variation on the tunneling current matching are evaluated by changing gate workfunction (WF). Fig. 8(a) shows the transfer characteristics with n-/p-type gate WF variations (-100 meV to +100 meV). It is observed that I_{DS} is shifted in parallel by changing gate WF. When n-type gate WF decreases compared to reference WF, the source-to-channel tunneling current is shifted (V_{TH} shift) in negative direction and thus the flat off-state region gets reduced. A n-type device in typical inverters serves to discharge the load capacitance (C_L) as a pull-down device, leading to V_{OUT} = 0 V [37]. Hence, the V_{3rd} disappears by the negative-shifted V_{TH} of n-type device because the n-type device already moves toward the on-current region and discharge the C_L before the p-type device reaches to the off-state region [Fig. 8(b)]. On the contrary, in the case of increasing n-type gate WF, V_{TH} is positive-shifted. Accordingly, both the n-/p-type devices can stay at the off-state region in the wider V_{IN} range and the V_{3rd} transition to 0 V is delayed in the consequence [Fig. 8(b)]. For p-type gate WF variations, it shows the opposite behaviors to n-type device. As p-type gate WF is reduced (V_{TH} becomes larger), the V_{3rd} keeps maintained in the larger V_{IN} range and the transition from V_{DD} to V_{3rd} occurs at the smaller V_{IN}. If p-type gate WF increases, the V_{3rd} disappears due to the reduced off-state region of the p-type device. Considering these effects of V_{TH} variation, the current matching between n-/p-type devices is critical to guarantee the proper ternary operations.

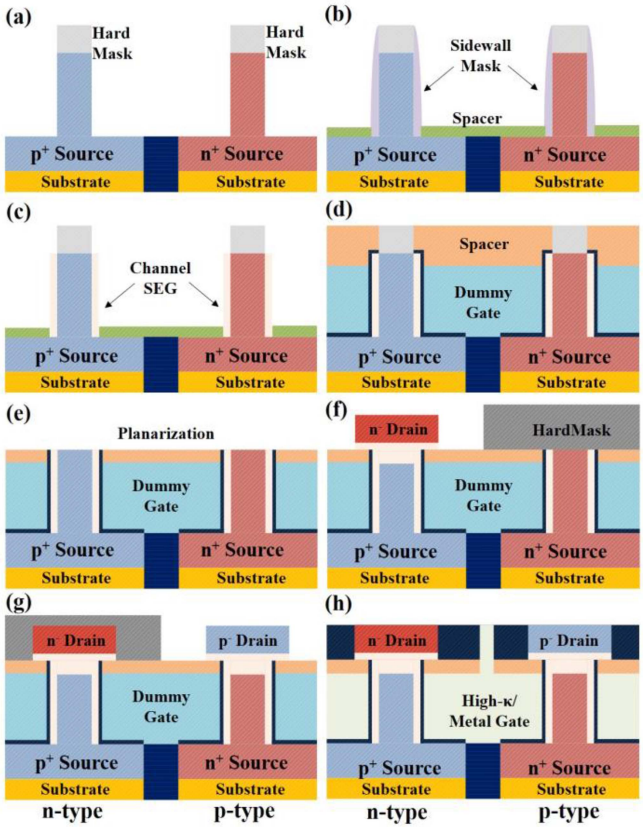

FIGURE 9. Summarized process integration for the proposed ternary device.

B. INTERFACE TRAP DENSITY VARIATION

In the T-CMOS$_{VF}$, 20% SiGe is used to boost tunneling current. However, it has been reported that SiGe degrades the device performance with serious interface trap densities (D_{it}) at SiGe-to-Si and SiGe-to-SiO_2 interfaces. In TFETs, the D_{it} causes trap-assisted tunneling (TAT) and it can have the serious effects on the performance of TFETs. To evaluate the effects of the TAT, various trap densities are applied to the source-to-channel, source-to-drain, and gate oxide-to-channel interfaces. For the TAT model, Hurkx trap-assisted tunneling was adapted with tunneling mass as above-mentioned in Section II. In order to investigate the effects of the interface trap density, traps near conduction band and those near valence band were set as acceptor-type trap and donor-type trap, respectively. Then, the interface trap densities were changed from 0 to $4x10^{13}$ $cm^{-2}eV^{-1}$. As the trap density increases, overall leakage current gets increased and subthreshold swing becomes worse in the transfer characteristics [Fig. 8(c)], which leads to the degradation of the V_{3rd} state in the VTC as shown in Fig. 8(d). It should be noted that the V_{3rd} state totally disappears over D_{it} = $2x10^{13}$ $cm^{-2}eV^{-1}$. Thus, the suppression of trap generation is critical for the stable ternary operations of the T-CMOS$_{VF}$. At least, interface trap density should be less than $5x10^{12}$ $cm^{-2}eV^{-1}$ for proper ternary operations.

C. GATE DIELECTRIC THICKNESS VARIATION

To maximize gate controllability on channel, the thinnest equivalent oxide thickness (EOT) is required by considering the allowable gate leakage current in TFETs. It means that the small EOT variation can significantly fluctuate the tunneling current. Furthermore, the tunneling current variation induced by quantum capacitance and random dopant fluctuation (RDF) can be also reflected to the EOT variation (Thus, in the simulations, quantum confinement and RDF effects are ignored for the simplified analysis). Fig. 8(e) shows that overall switching characteristics become worse (namely, higher turn-on voltage, lower on-current, and degraded subthreshold swing). Although the increased EOT extends the V_{3rd} state, the input voltage margin for V_{DD}/0V states get reduced as can be seen in Fig. 8(f).

VI. PROCESS INTEGRATION

The proposed T-CMOS based on the vertical tunnel FET can be integrated as shown in Figure 9. First, in-situ p^+ and n^+ heavily-doped SiGe are respectively grown on bulk silicon wafer to define the source region for n-/p-type devices. To form the thin vertical fin which is associated with the channel controllability, dry etching is carried out using a hardmask [Fig. 9(a)]. After the formation of sidewall oxide to protect the channel, nitride layer is deposited on the source region [Fig. 9(b)] and sidewall oxide is stripped by wet chemical

etchant. Next, selective epitaxial growth (SEG) is performed with intrinsic SiGe on the source to widen the tunneling area underlying the gate [Fig. 9(c)] and then nitride layer is etched. Subsequently, sacrificial oxide and dummy poly-Si gate are deposited and the etch-back process for dummy gate formation is performed. To form the spacer between gate and drain, nitride is deposited on the whole region and the planarization is conducted using chemical mechanical polishing (CMP) process [Fig. 9(d)]. Before defining the drain region, the nitride is etched back until the hardmask is removed and the SiGe is exposed [Fig. 9(e)]. For the n-type device, SiGe is partially trimmed while the p-type device area is blocked using a hardmask. Then, intrinsic and in-situ n^- doped SiGe (drain region) are grown sequentially on the exposed SiGe which plays the role as a seed layer for SEG process [Fig. 9(f)]. The same process (intrinsic and in-situ p^- doped SiGe drain) is repeated for the p-type device [Fig. 9(g)]. To passivate the drain region, oxide is deposited and planarized for inter-dielectric layer (ILD) formation. Finally, the part of oxide and the dummy gate are selectively etched and replaced with ALD interfacial oxide, high-κ dielectric, and metal gate [Fig. 9(h)]. Back-end-of-line (BEOL) flows are skipped because it is the same as the conventional CMOS process.

VII. CONCLUSION

In this study, the new T-CMOS which consists of the vertical tunnel FETs is introduced and analyzed using TCAD simulations with the calibrated model parameters. As contrast to the previously reported T-CMOS, the proposed T-CMOS$_{VF}$ is utilizing only the tunneling currents generated at source-to-channel and source-to-drain junctions to form the three different V_{OUT} states. It is successfully demonstrated that the T-CMOS$_{VF}$ can have the stable V_{3rd} in the VTC after the tunneling currents of n-/p-type tunnel FETs are properly matched. Hence, it can have the steeper subthreshold swing than other CMOS-based ternary inverters, which leads to be more suitable for V_{DD} scaling (namely, low power operations). The operation mechanism for the T-CMOS$_{VF}$ is clearly explained with the energy band diagram and transfer characteristics analysis. Furthermore, the effects of gate WF/D*it*/EOT variation on the VTC are evaluated considering the current mismatch which is critical to determine the stable ternary operation. In addition, the process integration flow of the T-CMOS$_{VF}$ is introduced in terms of the fabrication feasibility.

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