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Impact of Sulfur Passivation on Carrier Transport Properties of $In_{0.7}Ga_{0.3}As$ Quantum-Well MOSFETs

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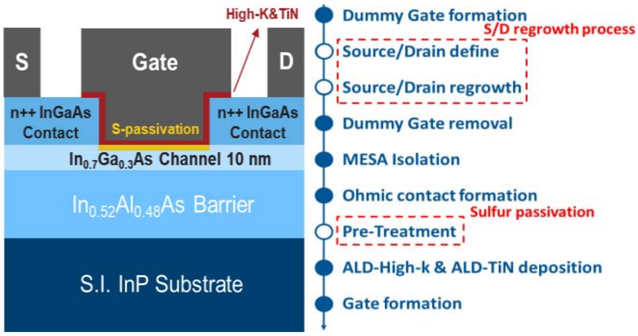
ABSTRACT We investigated the impact of a sulfur passivation (S-passivation) process step on carrier transport properties of surface-channel $In_{0.7}Ga_{0.3}As$ quantum-well (QW) Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) with source/drain (S/D) regrowth contacts. To do so, we fabricated long-channel $In_{0.7}Ga_{0.3}As$ QW MOSFETs with and without $(NH_4)_2S$ treatment prior to a deposition of $Al_2O_3/HfO_2 = 1\text{-nm}/3\text{-nm}$ by atomic-layer-deposition (ALD). The devices with S-passivation exhibited a lower value of subthreshold-swing (S) = 74 mV/decade and more positive shift in the threshold voltage (V_T) than those without S-passivation. From the perspective of carrier transport, S-passivated devices displayed excellent effective mobility (μ_{eff}) in excess of 6,300 $cm^2/V\cdot s$ at 300 K. It turned out that the improvement of μ_{eff} was attributed to reduced Coulombic and surface-roughness scatterings. Using a conductance method, a fairly small value of interface trap density (D_{it}) = 1.56×10^{12} $cm^{-2}eV^{-1}$ was obtained for the devices with S-passivation, which was effective in mitigating the Coulombic scattering at the interface between the high-k dielectric layer and the $In_{0.7}Ga_{0.3}As$ surface-channel layer.

INDEX TERMS $In_{0.7}Ga_{0.3}As$, MOSFET, passivation, carrier scattering mechanism, interface trap density, effective mobility.

I. INTRODUCTION

Metal-oxide semiconductor field-effect transistors (MOSFETs) with an indium-rich $In_xGa_{1-x}As$ ($x > 0.53$) quantum-well (QW) channel have been extensively explored as an n-channel device for next-generation logic applications with an operating voltage (V_{DD}) of 0.5 V or below, yielding excellent progress and accomplishments. This is a consequence of their superior carrier transport properties, such as high electron mobility (μ_{n_eff}) and virtual-source injection velocity (v_{inj}) [1]. Among them, it is particularly remarkable that del Alamo *et al.* reported nanometer-scale III-V MOSFETs from planar to fin [2], Tseng *et al.* demonstrated a record of subthreshold-swing of 70 mV/decade with InP MOSFETs [3], and Zota *et al.* reported a strong potential of an InGaAs QW MOSFET technology for next-generation RF applications [4]. At its heart is an extremely high quality interface between high-k (HK) dielectric layers and high-mobility III-V channel materials [5]. For the past two decades, significant breakthroughs have been made on a variety of III-V MOSFETs by using atomic-layer-deposition (ALD), coupled with various surface pre-treatment and/or passivation process steps including sulfur passivation (S-passivation). Several groups reported the S-passivation technique to demonstrate $In_{0.53}Ga_{0.47}As$ MOS-capacitors (MOSCAPs) with excellent interfacial characteristics, in which not only did the S-passivation effectively remove native oxides from the exposed $In_{0.53}Ga_{0.47}As$ surface but also passivated its surface with sulfur atoms [6]–[8]. Despite the fact that the impact of the S-passivation has been extensively investigated



(a) (b)

FIGURE 1. **(a) A schematic cross-section of an $In_{0.7}Ga_{0.3}As$ QW MOSFET and (b) process flow to fabricate the long-channel $In_{0.7}Ga_{0.3}As$ QW MOSFETs with sulfur passivation.**

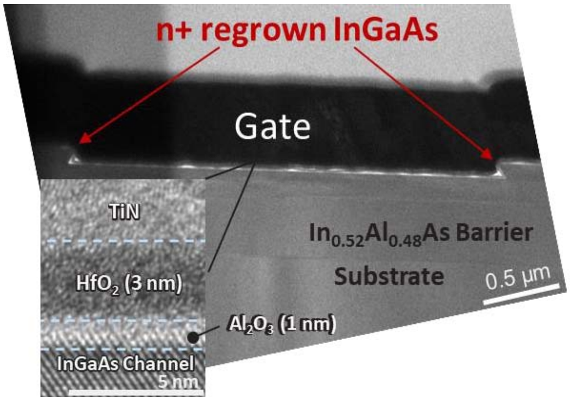


FIGURE 2. **TEM images of the fabricated $In_{0.7}Ga_{0.3}As$ QW MOSFET with S/D regrown contacts and the bi-layer gate stack of Al_2O_3 and HfO_2.**

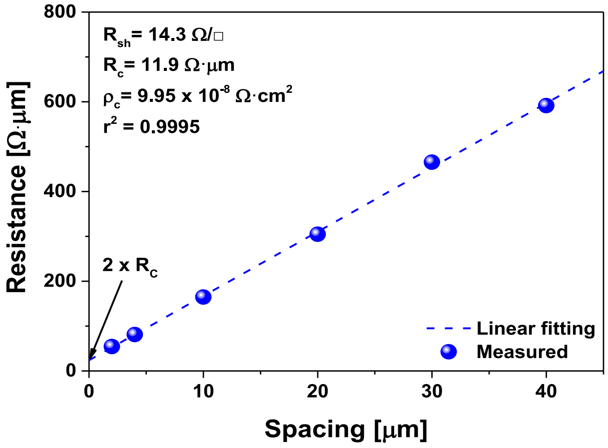


FIGURE 3. **Result of TLM data for the regrown n+ $In_{0.53}Ga_{0.47}As$ layers with a non-alloyed metal stack of Ti/Mo/Ti/Pt/Au.**

on the interfacial quality of $In_{0.53}Ga_{0.47}As$ MOSCAPs, there have been few reports on how the S-passivation would affect electrical characteristics of $In_xGa_{1-x}As$ QW MOSFETs from the perspective of electrostatic integrity and carrier transport. In this work, we adopted the S-passivation to fabricate surface-channel $In_{0.7}Ga_{0.3}As$ QW MOSFETs with selective S/D regrowth contacts. The devices with S-passivation exhibited outstanding electrical characteristics, including subthreshold-swing (S), effective mobility (μ_{eff}) and interfacial properties. Particularly, we carried out an analysis of dominant scattering mechanisms with respect to the average vertical electric field intensity (E_{v-eff}) under the gate of the device, such as Coulombic scattering, phonon scattering and surface roughness scattering. We found that the S-passivation helped to mitigate both Coulombic scattering due to the interface-state density (D_{it}) and surface-roughness scattering.

II. FABRICATION PROCESS

Figure 1(a) shows a schematic drawing of an $In_{0.7}Ga_{0.3}As$ QW MOSFET. The epitaxial layer structure was grown on a semi-insulating InP substrate using molecular beam epitaxy (MBE). From bottom to top, the epitaxial layer consisted of a 300-nm thick $In_{0.52}Al_{0.48}As$ buffer and a 10-nm thick $In_{0.7}Ga_{0.3}As$ surface channel on a semi-insulating InP substrate. The device fabrication process is highlighted in Fig. 1(b). Firstly, a 50 nm thick SiO_2 film was deposited on the surface of the as-grown epi-wafer by plasma enhanced chemical vapor deposition (PECVD) and S/D regions were opened by a mixture of BOE and DI. For S/D contacts, we adopted a Metal-Organic-Chemical-Vapor-Deposition (MOCVD)-based selective regrowth of a 60-nm thick $In_{0.53}Ga_{0.47}As$ layer with a doping concentration of 5×10^{19} cm^{-3} on top of the exposed $In_{0.7}Ga_{0.3}As$ channel. After removal of the SiO_2 dummy gate, electrical isolation of the active region was carried out using a mixture of H_3PO_4, H_2O_2 and DI. Next, we used a non-alloyed metal stack of Ti/Mo/Ti/Pt/Au on the heavily-doped regrown $In_{0.53}Ga_{0.47}As$ layer as S/D ohmic contacts. For the design of the passivation experiments, we used the S-passivation process with 21% $(NH_4)_2S$ solution for 10 min at room temperature, immediately followed by a diluted HCl treatment. In parallel, a reference device only with the HCl treatment was also prepared for comparison. Then, we deposited a bilayer gate stack of Al_2O_3/HfO_2 (1-nm/3-nm) at 200°C by ALD, and finished the device fabrication by forming a gate metal stack of TiN by ALD and Ti/Au by e-beam evaporation. Cross-sectional transmission-electron-microscopy (TEM) images of the fabricated device are shown in Fig. 2. Figure 3 shows the results of transmission-line-method (TLM) data, where the contact resistivity (ρ_c) and the sheet resistance (R_{sh}) were extracted to be $9.95 \times 10^{-8} \Omega \cdot cm^2$ and 14.3 $\Omega/\square$, with correlation coefficient (r^2) of 0.995, respectively.

III. RESULTS AND DISCUSSION

Figure 4 plots the output characteristics of the fabricated $L_g = 50$ μm $In_{0.7}Ga_{0.3}As$ QW MOSFETs with and without S-passivation for different values of the gate overdrive voltage ($V_{GS} - V_T$). The device with S-passivation exhibited better drain current driving capability and a much smaller value of the on-resistance (R_{ON}), indicating a lot higher value of the effective mobility in this device.

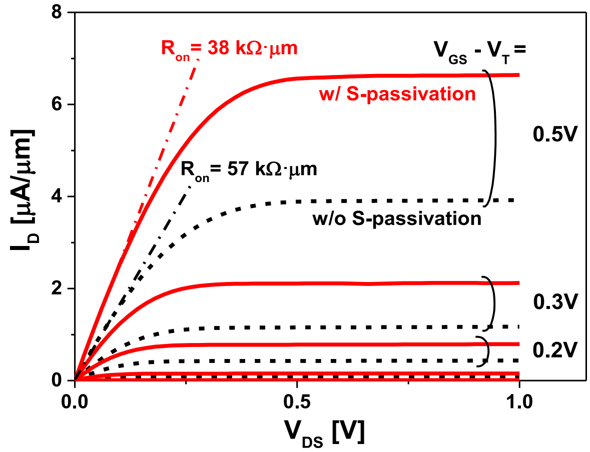


FIGURE 4. **Output characteristics for the fabricated $L_g = 50$ μm $In_{0.7}Ga_{0.3}As$ MOSFETs without S-passivation and with S-passivation. From top to bottom, the gate overdrive voltages sweep from 0.5 V to 0 V in -0.1 V steps.**

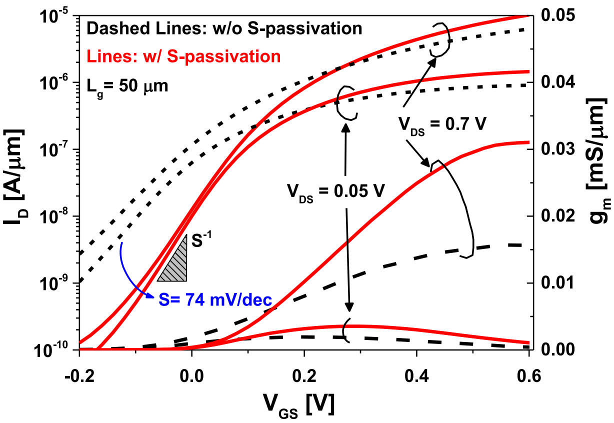
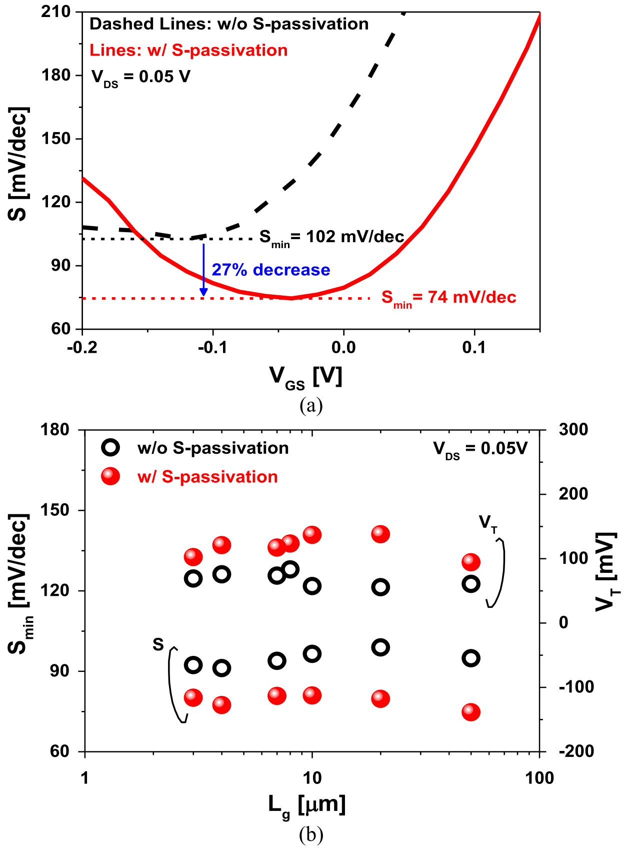


FIGURE 5. **DC subthreshold and transconductance (g_m) characteristics for the two devices at $V_{DS} = 0.05/0.7$ V.**



(a)

(b)

FIGURE 6. **(a) Locally extracted S against V_{GS} and (b) S_{min} and V_T against L_g for the two devices at $V_{DS} = 0.05$ V.**

Figure 5 plots the DC subthreshold and transconductance (g_m) characteristics of both $In_{0.7}Ga_{0.3}As$ QW MOSFETs. The device with S-passivation exhibited a positive value of the threshold voltage (V_T) = 94 mV at V_{DS} = 0.05 V, much higher value of the maximum transconductance (g_{m_max}) = 0.03 mS/μm in saturation (V_{DS} = 0.7 V) and, more importantly, much sharper subthreshold characteristics. Here, we used the linear extrapolation method of I_D against V_{GS} near maximum g_m bias point in linear for the extraction of V_T. In principle, the slope of g_m in saturation is proportional to the effective mobility of an FET. The device with S-passivation yielded a value of $d^2(I_D)/d^2(V_{GS}) = 0.072$ $\mu A \cdot \mu m^{-1} \cdot V^{-2}$, whereas the device without S-passivation 0.024 $\mu A \cdot \mu m^{-1} \cdot V^{-2}$, indicating that there would be an improvement of the effective mobility in the device with S-passivation. Figure 6(a) plots the extracted subthreshold-swing (S) at a given gate-to-source bias point and V_{DS} = 0.05 V for the two devices. A value of minimum subthreshold-swing (S_{min}) = 74 mV/decade was obtained for the device with S-passivation at room temperature. According to [9]–[10], the oxygen vacancies in high-k dielectric film induced unexpected positive charges and/or charge-dipoles, leading to a negative shift of V_T and poor interfacial quality by altering the electrostatic potential at the HK/InGaAs interface and forming electrically active traps from dangling bonds. The results in this work clearly confirm that the S-passivation process prior to the high-k dielectric deposition was effective in mitigating the oxygen vacancies, and therefore was attributed to the positive shift of V_T and the improvement of the device performance including g_m and S. Figure 6(b) summarizes the measured S_{min} and V_T against L_g for the two devices at V_{DS} = 0.05 V. All the S-treated devices with L_g from 50 μm to 3 μm possessed improved subthreshold characteristics and a positive shift in V_T by around 50 mV.

To investigate the impact of the $(NH_4)_2S$ treatment on the interfacial quality at the surface of the $In_{0.7}Ga_{0.3}As$ channel, we used a conductance method to estimate a value of D_{it} [10]–[13]. In doing so, we first removed all of the parasitic capacitance components from the measured capacitance-voltage (CV) characteristics and estimated a value of the insulator capacitance (C_{ins}) by correlating the measured CV curve to the modeled CV curve from the theoretical one-dimensional (1D) calculation for the same structure as in the device fabrication. Figures 7(a) and (b), respectively, show

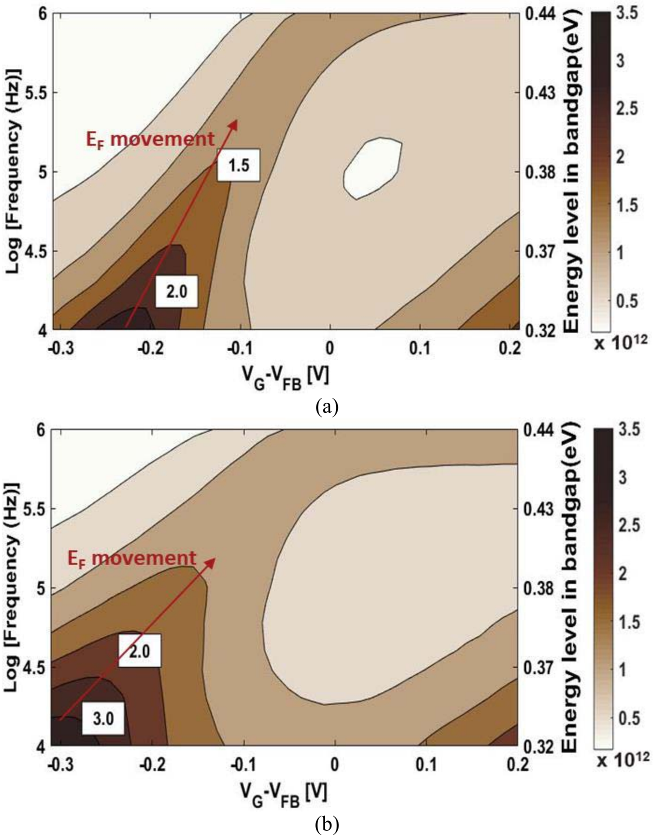


FIGURE 7. **(a) A contour map of D_{it} for both devices with S-passivation and (b) without S-passivation.**

a contour map of D_{it} for the same devices as a function of the measured frequency and the gate overdrive voltage with respective to the flat-band voltage (V_{FB}). The panel on the right shows the magnitude of D_{it} along with the degree of the band-bending (ϕ_s) in response to V_{GS}. Clearly, the peak of the contour map of D_{it} moves more vertically in the device with S-passivation, indicating more efficient movement of the Fermi-level (E_F) in response to V_{GS}. In order to evaluate the Fermi-level movement under the applied gate bias, we used a Fermi-level efficiency (FLE) method which was proposed to estimate the degree of the Fermi-level pinning phenomenon [14]. Using this method, the improvement of the interface quality with the S-passivation process was about 10% increase in the peak FLE. Along the right axis in Figs. 7(a) and (b), the energy distribution of the extracted D_{it} values for the same devices was plotted [15]–[16]. Overall, the D_{it} values of the device with the S-passivation were lower than those without the S-passivation. In particular, we obtained a minimum value of $D_{it} = 1.56 \times 10^{12}$ $\mathrm{cm^{-2}eV^{-1}}$ for the device with S-passivation, close to the mid-gap energy level.

Figure 8 plots the extracted effective mobility (μ_{eff}) of the fabricated $In_{0.7}Ga_{0.3}As$ QW MOSFETs with and without S-passivation, against the gate overdrive voltage ($V_{GS}-V_T$). Consistent with DC subthreshold and D_{it} results, the device with S-passivation possessed an excellent value of $\mu_{eff\_max} = 6{,}300$ $\mathrm{cm^2/V{\cdot}s}$ at 300 K. In order to understand the physical origin of the improvements and how the carrier transport properties of the devices were influenced by the S-passivation process, we attempted to analyze the dominant scattering mechanism by correlating the measured effective mobility into the average vertical electric field intensity (E_{eff}) and investigate each dominant scattering mechanism by correlating the measured effective mobility curve to the modeled one.

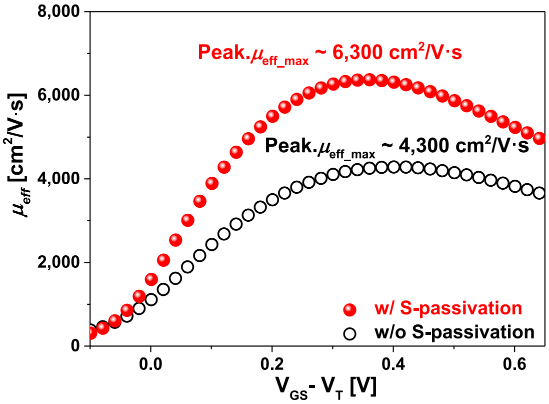


FIGURE 8. **The measured effective mobility (μ_{eff}) against the gate over-drive voltage ($V_{GS} - V_T$) for the two devices.**

By definition, E_{eff} is given by:

$$E_{eff} = \frac{\left(\frac{Q_{QW}}{2} + Q_{II}\right)}{\varepsilon_{InGaAs}} \tag{1}$$

Here, Q_{QW} is the areal electron charge density of the $In_{0.7}Ga_{0.3}As$ QW channel, Q_{II} is the areal ionized impurity charge density of the $In_{0.7}Ga_{0.3}As$ QW channel and the $In_{0.52}Al_{0.48}As$ buffer, and ε_{InGaAs} is the permittivity of the $In_{0.7}Ga_{0.3}As$ QW channel. Since Q_{II} is very small due to the use of the unintentionally doped $In_{0.7}Ga_{0.3}As$ QW channel and $In_{0.52}Al_{0.48}As$ buffer layers, $E_{v\text{-}eff}$ is approximated as $E_{v\text{-}eff} \sim Q_{QW}/\varepsilon_{InGaAs}$. Considering a wide range of the transverse field intensity, the dominant scattering mechanisms for the 2-DEG of the $In_{0.7}Ga_{0.3}As$ QW channel are Coulombic, phonon, and surface-roughness scattering, respectively. We can therefore approximate the total scattering mechanism ($1/\mu_{Total}$) by Matthiessen's rule [17]–[18]:

$$\frac{1}{\mu_{Total}} = \frac{1}{\mu_{cs}} + \frac{1}{\mu_{phs}} + \frac{1}{\mu_{srs}} \tag{2}$$

The dependence of each scattering mechanism on E_{v-eff} has been extensively explored not only in Si MOSFETs [19], but also in InGaAs QW MOSFETs [18], showing an exponential dependency on E_{v-eff} with appropriate values of coefficient and exponent. In the low-field regime, the scattering mechanism associated with the Coulombic interactions matters, due to the ionized impurities inside the $In_{0.7}Ga_{0.3}As$ QW channel and the charged defects at the interface between the high-k dielectric layer and the $In_{0.7}Ga_{0.3}As$ QW channel.

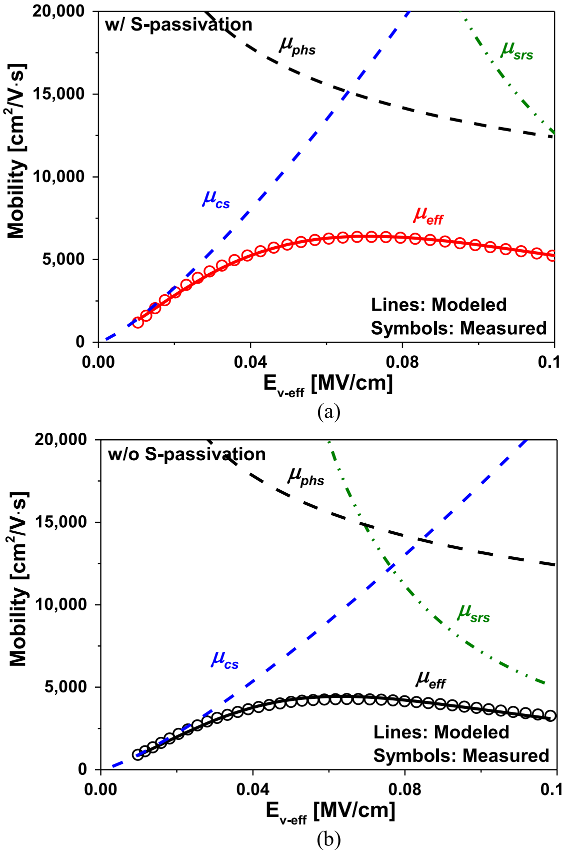


FIGURE 9. Comparison of the measured (circle) and modeled (line) effective mobility for the two devices with S-passivation (a) and without S-passivation (b).

TABLE 1. The results of the analysis of each scattering mechanism in both devices.

	$\mu_{cs}^{-1}= A \times E_{v\text{-}eff}^{\alpha}$		$\mu_{phs}^{-1}= B \times E_{v\text{-}eff}^{\beta}$		$\mu_{srs}^{-1}= C \times E_{v\text{-}eff}^{\gamma}$	
	A	α	B	β	C	γ
w/ Sulfur	98	-1.28	$1.7 \text{x} 10^{-6}$	0.33	$5.5 \text{ x} 10^{-15}$	2
w/o Sulfur	145	-1.28	$1.7 \text{x} 10^{-6}$	0.33	$1.4 \text{ x} 10^{-14}$	2

TABLE 2. Benchmarking of the key device metrics in this work against those reported by other groups [20]–[26].

	Gate stack	S [mV/dec]	D$_{it}$ [cm^{-2}·eV^{-1}]	μ_{eff_max} [cm^2/V·s]	comment
This work	**Al_2O_3/HfO_2**	**74**	**$1.56 \text{ x} 10^{12}$**	**6300**	**Surface ch. S-treated**
[20]	α -Si/Al_2O_3	150	N/A	3800	Buried ch. HF-treated
[21]	Al_2O_3	106	N/A	4400	Buried ch. HCl-treated
[22]	Al_2O_3	94	~1 $\text{x} 10^{12}$	5700	Buried ch. HCl-treated
[23]	Al_2O_3/HfO_2	80	N/A	5500	Surface ch. HF-treated
[24]	Al_2O_3	N/A	2.7 $\text{x} 10^{12}$/ 1.9 $\text{x} 10^{12}$	2030/720	Surface ch. S/HCl treated
[25]	Al_2O_3	170	3.0 $\text{x} 10^{12}$	3000	Surface ch. S-treated
[26]	$TaSiO_x$	73	2 x 10^{11} [MOSCAP]	N/A	Buried ch.

In the medium-field regime, the phonon scattering matters, due to the acoustic and optical phonons in the lattice. In the high-field regime, the surface-roughness scattering matters. Each scattering mechanism can be modeled as in [18]–[19] and mathematically given by

$$\frac{1}{\mu_{cs}} = A \times E^{\alpha}_{v-eff} \tag{3}$$

$$\frac{1}{\mu_{phs}} = B \times E^{\beta}_{v-eff} \tag{4}$$

$$\frac{1}{\mu_{srs}} = C \times E^{\gamma}_{v-eff} \tag{5}$$

Figures 9(a) and (b) plot the measured and the modeled μ_{eff} against $E_{v-\text{eff}}$, together with each modeled mobility components (μ_{cs}, μ_{phs} and μ_{srs}) for the two devices with S-passivation and without S-passivation. The same values of $\beta = 0.33$ and $\gamma = 2$ were used for the two devices. This makes sense because the same $In_{0.7}Ga_{0.3}As$ QW channel was used in both devices. First, the modeled μ_{eff} was in excellent match with the measured one, confirming that the total scattering mechanism in the fabricated $In_{0.7}Ga_{0.3}As$ QW MOSFETs was explained well by three different scattering sources as mentioned above. Second, the S-passivation process was effective in mitigating not only Coulombic scattering which resulted from the improved interfacial behavior, but also surface-roughness scattering in strong inversion. Particularly, the reduction of the surface-roughness scattering would be of great importance, since it directly affects the on-current (I_{ON}) and the peak transconductance (g_{m_max}) of an InGaAs QW MOSFET for future logic and RF applications.

Table 1 summarizes the result of the analyzed scattering mechanisms for the two devices. Note that phonon scattering was irrelevant with the S-passivation process as explained above, whereas both coefficients of the Coulombic and surface-roughness scatterings for the device with S-passivation were significantly reduced with the same values of exponent.

Table 2 finally compares the key device metrics obtained in this work to those reported in the literature [20]–[26]. It is clear that the results in this work display the best balance of the carrier transport properties and the interfacial characteristics in any InGaAs QW MOSFET technology, indicating a successful demonstration of the S-passivation process in the QW MOSFETs

IV. CONCLUSION

In summary, we experimentally investigated the impact of a sulfur passivation process on the electrostatic integrity and carrier transport properties of surface-channel $In_{0.7}Ga_{0.3}As$ QW MOSFETs with S/D regrown contacts. The fabricated device with S-passivation showed an excellent combination of subthreshold, interfacial and carrier transport characteristics. To understand how those improvements arose from, we carried out the extraction of D_{it} using a conductance method and the analysis of the dominant scattering mechanism for the two devices with and without S-passivation, indicating that both Coulombic scattering and surface-roughness scattering were significantly suppressed with the S-passivation process.

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