Received 6 October 2020; revised 23 December 2020; accepted 30 January 2021. Date of publication 4 February 2021; date of current version 25 February 2021. The review of this article was arranged by Editor X. Guo.

Digital Object Identifier 10.1109/JEDS.2021.3057195

Fast Progressive Compensation Method for Externally Compensated AMOLED Displays

HING-MO LAM, HEZI QIU, CHENGLIN LI (Student Member, IEEE), JINYUAN WEN, WENLONG BAI, CONGWEI LIAO, MIN ZHANG (Member, IEEE), HAILONG JIAO (Member, IEEE), AND SHENGDONG ZHANG (Senior Member, IEEE)

School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School, Shenzhen 518055, China

CORRESPONDING AUTHORS: S. ZHANG AND H. JIAO (e-mail: zhangsd@pku.edu.cn; jiaohailong@pku.edu.cn)

This work was supported by the Shenzhen Municipal Scientific Program under Grant GGFW2017072816344703 and Grant JCYJ20180504165449640.

ABSTRACT The externally compensated display system has been proved to have greater potential to completely solve aging and uniformity issues of the AMOLED display system than the internally compensated display system. However, the traditional compensation method is time consuming and responses slowly to the mobility change of TFT. The traditional compensation method performs calibration during the inter-frame blanking period, the length of which is limited. Only a few rows of pixel circuits can be calibrated per frame. Furthermore, each pixel circuit needs multiple times of calibration to reach compensated state. In this article, a fast progressive compensation method is proposed. The calibration of a row of pixel circuits is performed K rows ahead of the display line during the display data updating period. By doing so, the proposed fast progressive compensation method can approach compensated state faster than the traditional method because display data updating period is significantly longer than the inter-frame blanking period. For the case of 10% inter-frame blanking period and 20 μs waiting delay for feedback data line to be stable, the proposed method reduces the compensation time by ∼14x than the traditional method.

INDEX TERMS Thin-film transistor (TFT), external compensation, fast calibration.

I. INTRODUCTION

After decades of development, Active-Matrix Organic Light-Emitting Diode (AMOLED) display technology shows better performance than Active-Matrix Liquid Crystal Display (AMLCD) display technology in color gamut, contract ratio, response time, viewing angle, and working temperature. Increasing number of consumer electronic devices adopt AMOLED display technology, such as smart phones, smart watches, and high-end televisions.

Thin Film Transistor (TFT) is used as the backplane for both AMLCD and AMOLED display technologies. The TFT in AMLCD is only used as a switch to transfer the display voltage. The aging or non-uniformity of the TFT is therefore not crucial for AMLCD. However, in AMOLED, TFT is also used as a current source to provide a constant current to drive OLED to emit a constant luminance of light. Therefore, if the aging and non-uniformity of the TFT are not properly compensated, these two issues are fatal to AMOLED displays.

The compensation schemes of AMOLED displays can be generally classified as internal and external compensations. The internal compensation performs compensation by a limited number (typically less than ten) of TFTs [1]–[7] inside a pixel circuit on a display panel. The internal compensation scheme is preferable for compensating the non-uniformity of threshold voltage of TFTs, as well as the threshold voltage shifting of TFTs and OLEDs. However, internal compensation is not effective in handling issues due to the physical location of each pixel and luminance degradation of OLEDs. Alternatively, the external compensation feedbacks the aging information from on-panel pixel circuits to the off-panel sensing module which is

usually realized by CMOS technology [8]–[14]. More off-panel resources, such as, DSP, CPU and memory, could be employed to implement any complicated compensation algorithms. The external compensation can be further classified into real-time compensation [14] and non-real-time compensation [8]–[13]. The real-time external compensation is a design in which the feedback sensing and pixel circuit programming are performed in the same time period. The feedback aging or non-uniformity data are immediately applied to the display data. The non-real-time external compensation is a design in which the feedback sensing and pixel circuit programming are performed in the different time periods. Usually, accurate feedback sensing takes time to complete. Compared to the real-time compensation, the non-real-time compensation has lower requirement for the source driver design and allows feedback sensing and display compensating at different time periods. Furthermore, a simple comparator rather than an ADC is used as a sensing block to sense the feedback aging data [8], [12]. Since the 1-bit output comparator only senses whether the feedback data is larger or smaller than the reference data, multiple iterations of calibration are needed to approach the final compensation value which is able to feedback the data close to the reference data. This compensation method is therefore named as progressive compensation.

With the traditional non-real-time external compensation scheme, the feedback sensing of pixel circuits is carried out during inter-frame blanking period. Only a few rows of pixel circuits can complete one iteration of calibration in the limited period of inter-frame blanking. In [15], the blanking period is indicated as $\sim$500 μs, which is only long enough to complete one iteration of calibration of $\sim$10 rows of pixel circuits. Therefore, a significant amount of frame times is needed to complete the compensation of all pixel circuits on panel.

In this article, a fast compensation method is proposed, which allows the design to carry out calibration during the display data updating period instead of inter-frame blanking period. The proportion of the display data updating period is significantly larger than the inter-frame blanking period. Therefore, the proposed method can complete the compensation faster than the traditional method.

The rest of this article is organized as follows. The background of the external compensation display system is introduced in Section II. The proposed external compensation method is presented in Section III. The performance of the proposed and traditional external compensation methods is compared in Section IV. Simulation results are provided in Section V. The paper is concluded in Section VI.

II. REVIEW OF THE EXTERNALLY COMPENSATED DISPLAY SYSTEM

In this section, the non-real-time external compensation display system and two basic operations, display operation and calibration operations, are presented.

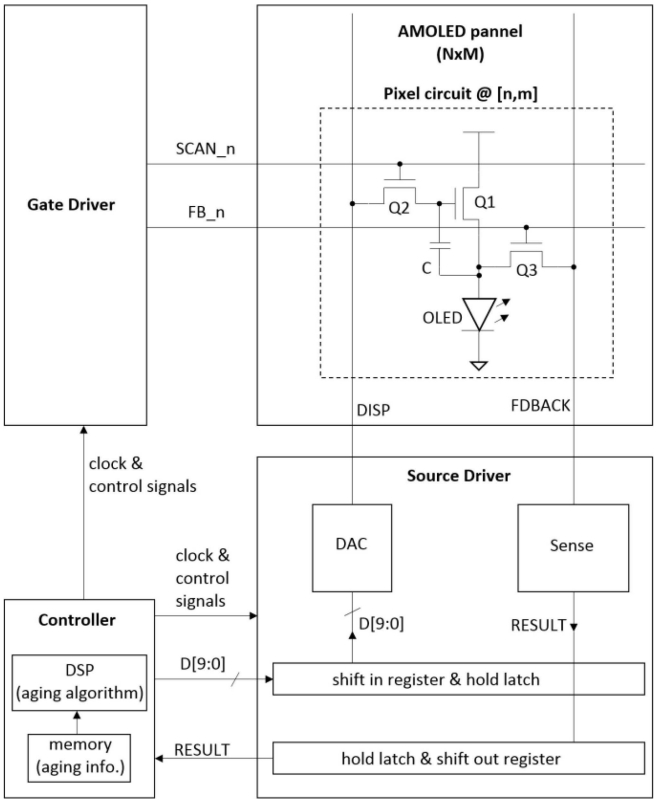

FIGURE 1. Block diagram of a non-real-time external compensation display system.

The block diagram of a non-real-time external compensation display system is shown in Fig. 1. The system consists of an AMOLED panel, a gate driver, a source driver, and a controller. The AMOLED panel includes an array of N$\times$M pixel circuits. One example of pixel circuit is drawn in Fig. 1, which consists of three TFTs, a storage capacitor, and an OLED. Q1 is a driving TFT used to provide a constant current for the OLED. Q2 and Q3 are switching TFTs. Q2 is for writing the display or calibration datum into the pixel circuit. Q3 is for feeding back the aging information to a sense module in the source driver. In this work, the feedback aging data is the current of driving TFT Q1. If the driving TFT Q1 is aged, the threshold voltage shifts up, so that the feedback current decreases. The sense module includes a current comparator to compare the feedback current of the driving TFT Q1 with a fixed reference current to judge if the calibration data is over or under compensated. The result is used to update the memory of aging information in the controller.

The non-real-time external compensation display system carries out two types of operations, display operation and calibration operation. The display operation is used to display a picture accurately on the panel. The controller runs a compensation algorithm to compensate each incoming display datum based on the aging information stored in the memory and controls the gate driver and source driver to sequentially display a picture on the panel line by line.

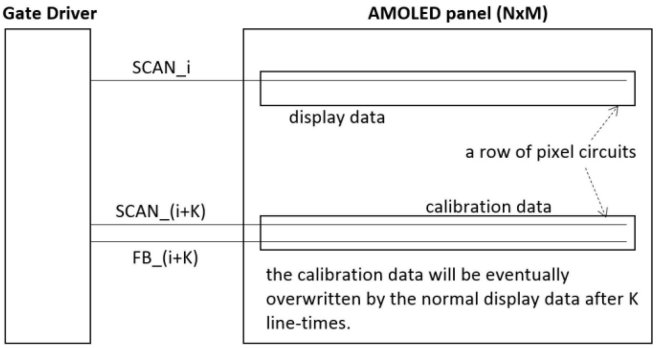

FIGURE 2. Diagram of the conceptual idea of the proposed fast progressive compensation method.

The calibration operation is used to keep tracking the aging status of every pixel circuit on the panel and to update the stored aging information in the memory. The calibration operation includes three steps. The first step is to write the calibration data into the selected row of the pixel circuit through the display operation. The second step is to feedback the current of TFT Q1 to the sense module in the source driver. The third step is to sense if the feedback current is higher or lower than the expected reference current. Both the first and third steps take one line-time to complete (the definition of line-time is shown in Fig. 4). The second step is relatively longer (usually multiple line-times) until the feedback data lines (FDBACK) become sufficiently stable for sensing. The actual length of the feedback period depends on the loading of feedback data lines and the target accuracy to achieve. The design flexibility of the feedback period of the second step is one of the major differences between the traditional and proposed compensation methods.

In the traditional compensation method of the non-real-time external compensation display system, the display operation and the calibration operation are performed separately in different time periods. The calibration operation is carried out outside the display data updating period (t_{UPDATE} in Fig. 4). The inter-frame blanking period (t_{BLANK} in Fig. 4) is a natural choice if not want to stop the normal display and specifically spare a period for calibration operation. The inter-frame blanking period (t_{BLANK}) is typically short compared to the display data updating period (t_{UPDATE}). Only few rows of pixel circuits are able to carry out one iteration of calibration. Therefore, it takes many frame-times (t_{FRAME} in Fig. 4) to complete one iteration of calibration of all pixel circuits on the panel. Even worse, a pixel circuit typically takes multiple iterations of calibration to approach the final compensation value of the pixel circuit. Especially when the display panel turns on again after a long shutdown because the aging of TFT and OLED is recovered to some extent during the shutdown and deviates from the previously stored compensated value. All of the above makes the traditional compensation method response slowly to the aging of the pixel circuit. Alternatively, the proposed compensation method of the non-real-time external compensation display system enables the design to carry out the calibration operation during the display data updating period (t_{UPDATE}). Therefore, the proposed method can approach the final compensation value much faster than the traditional design.

III. PROPOSED FAST PROGRESSIVE COMPENSATION

In this section, a new fast progressive compensation method is proposed for the non-real-time external compensation display system. The basic concept of the proposed compensation method is illustrated in Fig. 2. This method takes the advantage of any display system which sequentially updates display data of a picture on the panel line by line. The proposed compensation method is to perform a calibration operation on the row of pixel circuits of K rows ahead of the row undergoing display operation. The K rows ahead also means K line-times, which is the feedback delay of the second step of the calibration operation. As shown in Fig. 2, when the display operation proceeds on Row i, the calibration operation carries out on Row i+K. After K line-times, the normal sequential display operation eventually overwrites the calibration data of the pixel circuits of Row i+K. The calibration data only occupy the pixel circuits of Row i+K for K line-times, which is short and not visible to human eyes.

The step-by-step derivation of the proposed compensation method from a general display system is illustrated in Fig. 3. The sequential display data updating of a general display system is shown in Fig. 3a. The display data transfer from the controller to the source driver row by row during the display data updating period (t_{UPDATE}). The box with L_n inside and t_n beneath represents the n-th row of display data writing into the n-th row of pixel circuits at the n-th line-time through a display operation, where the value of n is between 1 and N. For simplicity and without loss of generality, we assume that the display panel is single-colored and the resolution is N×M. N is the number of rows of pixel circuits, while each row includes M pixel circuits. t_{LINE} is line-time, which represents the time interval to transfer one row of display data from the controller to the source driver. t_{UPDATE} is the time period to transfer one frame (N rows) of display data from the controller to the source driver. After transferring the last row of display data, there is a short period of inter-frame blanking, t_{BLANK}.

The first step of the derivation of the proposed method is shown in Fig. 3b. N rows of display data (or pixel circuits) are divided into K rows per segment. The last segment (segment S) may be less than K if the value N is not multiple of K. The thick bold boxes in Fig. 3b shows the segmentation of all N lines of display data. There is totally S = ceil[N/K] number of segments.

The second step of the derivation is to insert an extra line-time (yellow box) into each segment, as shown in Fig. 3c. This extra line-time is used to perform the third step of the ongoing calibration operation (sensing the feedback current

FIGURE 3. **(a) The sequence of display data transferred from the controller to the source driver in a conventional display system. (b) The sequence of display data is divided into K rows per segment. (c) Insert an extra line-time for each segment to write calibration data and sense the feedback current, and insert Segment 0 for calibration of first K rows of pixel circuits. (d) An example of a complete iteration of calibration of all pixel circuits on the panel with K equal to 3.**

of pixel circuits of Row i) and the first step of the next calibration operation (writing calibration data into pixel circuits of Row i+K). The second step of the ongoing calibration operation (feedbacking the driving current of pixel circuits of Row i) can be carried out simultaneously with display operations. C_y in the yellow box of Fig. 3c represents the first step of a calibration operation on the pixel circuits of y-th row. S_x represents the third step of the calibration operation on the pixel circuits of x-th row. The value of x and y is between 1 and N, while the value of $y = x + K$. Some yellow boxes having both C_y and S_x inside mean that the pixel circuits of y-th row and x-th row perform the first step and third step of the calibration operation in parallel at the same line-time.

In order to keep the display frame frequency, the frame-time (t_{FRAME}) and the length of each segment remain unchanged. The line-time t_{LINE} is shortened to be t_{LINE}'. One line-time t_{LINE}' is spared in each segment for performing the first and/or the third step of the calibration operation. Therefore, the delay of new line-time is $t_{LINE}' = t_{LINE} \times [K/(K+1)]$. The reduction in new line-time is negligible if K is sufficiently large. The design requirement of the source driver would not be increased significantly.

In order to carry out the calibration operation on the first K rows of pixel circuits in Segment 1, one extra segment needs to be added in front of Segment 1. As shown in Fig. 3c, the extra segment, Segment 0, is added at line-time from t_{-4}' to t_{-1}'.

An example of a complete iteration of calibration of all pixel circuits on the panel with K equal to 3 is illustrated in the three sub-figures of Fig. 3d. The display and calibration operation in three successive frames are shown in these three sub-figures.

The first step of the calibration operation (C_1) is shown in the first sub-figure of Fig. 3d, writing the calibration data into the first row of pixel circuits at line-time t_{-4}'. Then in the second step, driving current feedback period, wait for 3 line-times from t_{-3}' to t_{-1}', until the feedback

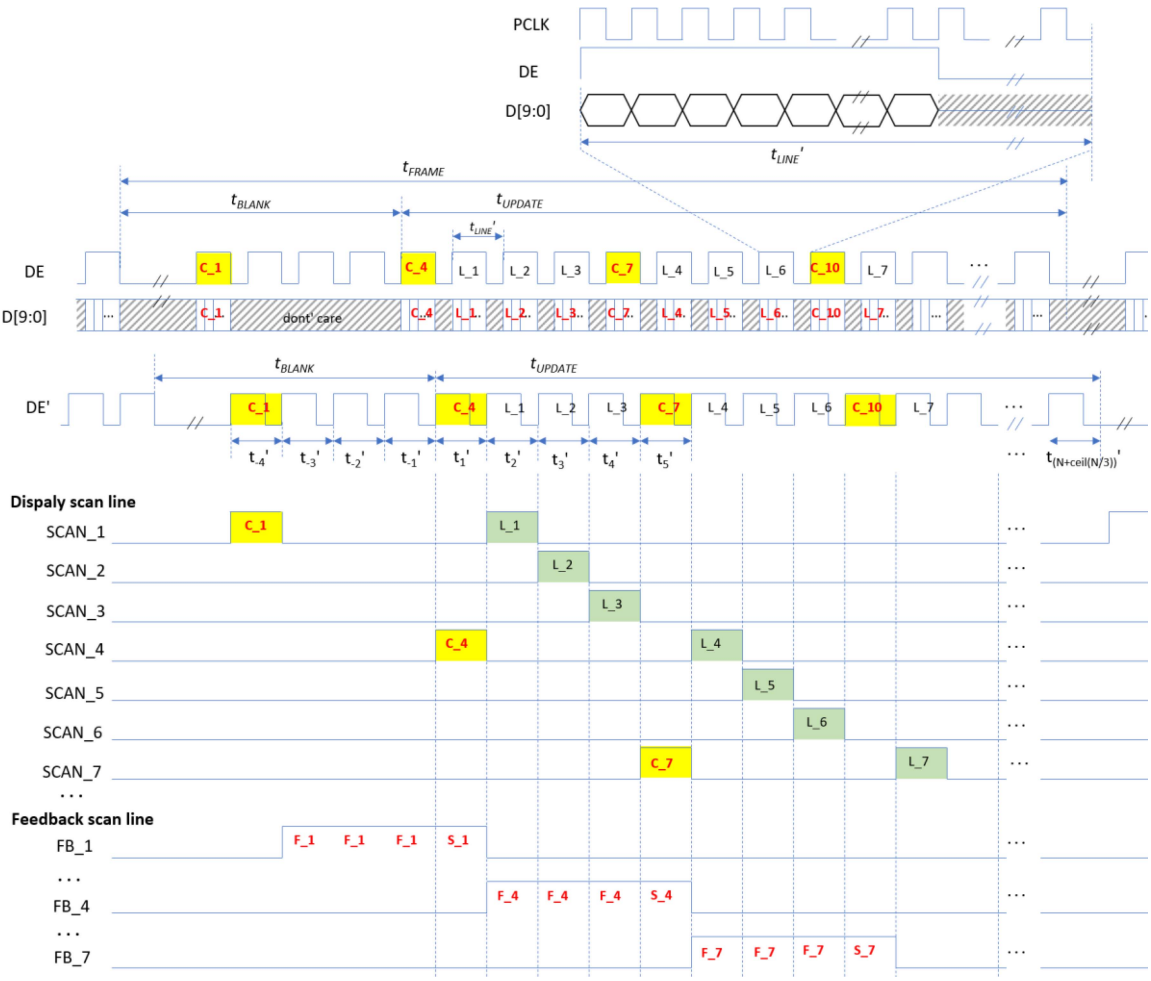

FIGURE 4. **Timing diagram of the proposed fast progressive compensation method.**

data line (FDBACK) becomes sufficiently stable for sensing. The third step (S_1) is to sense the feedback current of the first row of pixel circuits at line-time t_1' in Segment 1. Meanwhile, the first step of the next calibration operation (C_4) is carried out. The calibration data that were previously written into the first row of pixel circuits are overwritten by the normal display data L_1 at line-time t_2'.

In the example above, there is no display operation carried out in the period of Segment 0 because Segment 0 is located inside the inter-frame blanking period and no display data are transferred from the controller to the source driver in that period. However, in all other segments, display operations are carried out parallelly with the second step (driving current feedback period) of the calibration operation. For example, in the first sub-figure of Fig. 3d, the display data L_1, L_2, and L_3 are written into the first, second, and third row of the pixel circuits in Segment 1 at the line-time t_2', t_3', and t_4', respectively. Meanwhile, the aging information of the fourth row of pixel circuits is fed back to the sense module in the source driver.

The yellow boxes in the first sub-figure of Fig. 3d shows the calibration operations for Rows 1, 4, 7, 10 of pixel circuits at line-time t_{-4}', t_1', t_5', t_9', respectively. The second sub-figure carries out the calibration operation for Rows 2, 5, 8, 11 of the pixel circuits at the line-time t_{-3}', t_2', t_6', t_{10}', respectively. The third sub-figure carries out the calibration operation for Rows 3, 6, 9, 12 of the pixel circuits at the line-time t_{-2}', t_3', t_7', t_{11}', respectively. After three frames, an iteration of calibration of all pixel circuits is completed.

There are four line-times within each segment. However, only three frame-times are required to complete one iteration of all pixel circuits. Therefore, the fourth line-time in each segment is never used for writing the calibration data or sensing the feedback current.

The timing diagram of the display and calibration operation of the example in the first sub-figure of Fig. 3d with K=3 is shown in Fig. 4. In this article, we assume that the panel is single colored without loss of generality. The timing diagram of other two sub-figures are similar, while the location of calibration operation is shifted by one row of pixel circuits. The signal PCLK and DE are pixel clock and data enable, respectively. D[9:0] is a compensated display or calibration datum of a pixel circuit. All above signals are the outputs of the controller. The raw display data is 8-bit and becomes 10-bit after getting compensated in the controller. The compensated display or calibration datum is valid only

when DE is asserted. DE' is the delayed signal of DE and is for internal usage of the source driver to parallelly output a row of compensated display or calibration data to 10-bit linear DACs. SCAN_n and FB_n are the scan signals generated by the gate driver for writing compensated display or calibration data into the n-th row of pixel circuits and for feedbacking the driving current of the n-th row of pixel circuits to the sensing blocks, respectively.

In Fig. 4, the word C_n, L_n, F_n, or S_n are marked on the top of some signals in the timing diagram, representing that the signals are doing below operations, such as, writing calibration data (C_n) into, writing compensated display data (L_n) into, feedbacking current (F_n) from or sensing the feedback current (S_n) of the n-th row of pixel circuits.

The example in the timing waveform in Fig. 4 starts from the controller transferring the calibration data (C_1) of the first row of pixel circuits to the source driver. The word C_1 with yellow background on the top of signal DE represents that DE is enabled to validate calibration data D[9:0] at the time period of the yellow background. After transferring the last calibration datum, DE pulls down and triggers DE' to be pulled up.

The word C_1 with yellow background marked on the top of signals DE' and SCAN_1 at line-time t_{-4}' represents that the calibration data of the first row of pixel circuits pass to ADCs and then outputs to display data lines (DISP). Meanwhile, the gate driver turns on the scan line SCAN_1 to write the calibration data into the first row of pixel circuits.

The words F_1, F_1, F_1, and S_1 put on the top of signal FB_1 at line-time t_{-3}', t_{-2}', t_{-1}', and t_1', respectively, representing that signal FB_1 is turned on to feedback the driving current of the first row pixel circuits from line-time t_{-3}' to t_{-1}', and kept on during the sense block sensing the feedbacked current at t_1'. At line-time t_1', word C_4 with yellow background also puts on the top of signal DE' and SCAN_4, which means to carry out the first step of calibration operation to write the calibration data into the 4-th row of the pixel circuits.

The words L_1, L_2, and L_3 put on the top of signal DE', SCAN_1, SCAN_2, and SCAN_3 at line-time t_2', t_3', and t_4', representing that those signals are performing display operation to write the display data into the first, second, and third row of pixel circuits at line-time t_2', t_3', and t_4', respectively. The reset of the timing waveform can be interpreted in the same manner.

To design the display line and feedback line gate drivers by TFT on the panel (GOA, gate-on-array) in a custom way is challenging for the proposed compensation method. Especially for the display line, the scan line is required to be able to jump to K lines ahead and then jump back. Furthermore, the value of K is required to be programmable. In [17] and [18], IGZO (indium gallium zinc oxide) TFTs are used to implement logic gates and SRAM (Static Random Access Memory) arrays, respectively. Therefore, one possible solution is to use TFT to design the scan line gate driver similar to the row-decoder, which is commonly used in memory design to select a row of memory cells with the row address. Another possible solution is to design the row-decoder type gate driver as an external discrete gate driver IC.

IV. PERFORMANCE COMPARISON

In this section, the performance of the traditional and the proposed compensation methods is evaluated by comparing how many rows of pixel circuits can be calibrated per frame. As mentioned above, the calibration operation of a row of pixel circuits includes below three steps in both the proposed and traditional compensation methods. The first step is to write the calibration data into the selected row of pixel circuits. The second step is to wait for feedback data line to be sufficiently stable for sensing. The third step is to sense feedback driving current. The traditional compensation method actually also includes the fourth step, i.e., writing the original display data back to the row of pixel circuits before completing the calibration operation. In this article, we assume that the first, third, and fourth steps all take one line-time to complete, while the delay of the second step is variable.

In the traditional compensation method, the calibration operation is carried out during the inter-frame blanking period. The length of the inter-frame blanking period is limited. Therefore, only few rows of pixel circuits are able to be calibrated per frame. In the display industry, there is no specific standard for the length of the inter-frame blanking period. In this article, we assume that the inter-frame blanking period occupies 1%, 5%, and 10% of the frame interval. The frame frequency is 60 Hz. The display panel resolution is 3840×2160.

Below (1) and (2) are used to calculate the length of inter-frame blanking period (t_{BLANK}) and line-time (t_{LINE}) of the traditional compensation method.

$$t_{BLANK} = \frac{1}{60} \times blanking\_percentage. \tag{1}$$

$$t_{LINE} = \frac{\left(\frac{1}{60} - t_{BLANK}\right)}{2160}. \tag{2}$$

(3) is used to calculate the length of line-time of the proposed compensation method.

$$t'_{LINE} = t_{LINE} \times \frac{K}{K+1}. \tag{3}$$

The value of K is selected so that the minimum value of K can fulfill (4) below.

$$t'_{LINE} \times K \geq t_{FDBACK}, \tag{4}$$

where t_{FDBACK} is the feedback delay of the second step of the calibration operation. In Table 1, we assumed the feedback delay is from 20 μs to 160 μs with 20 μs per step.

According to the above equations, the length of the inter-frame blanking period of the traditional compensation method is 166.67 μs, 833.33 μs, and 1666.67 μs for 1%, 5%, and 10% inter-frame blanking percentages, respectively, as listed in Table 1. The line-time of the traditional design is

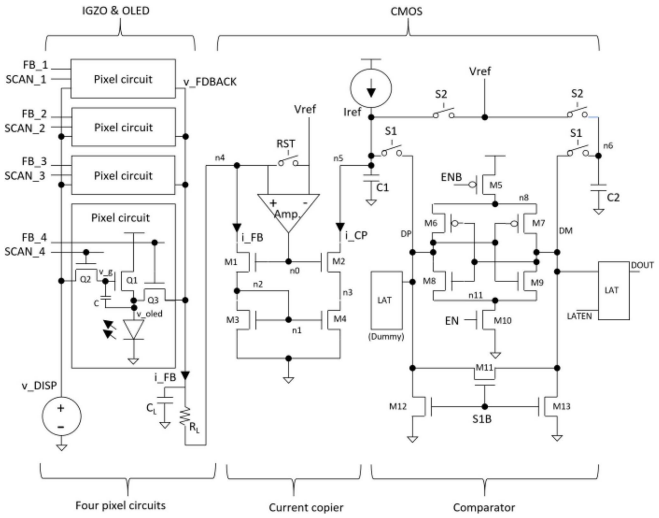

FIGURE 5. **Circuit to demonstrate the proposed fast progressive compensation method.**

7.64 μs, 7.33 μs, and 6.94 μs for 1%, 5%, and 10% inter-frame blanking percentages, respectively. The line-time of the proposed compensation method is between 5.56 μs to 6.68 μs for K ranging from 4 to 25 and 10% inter-frame blanking percentage.

The total number of rows calibrated per frame of the traditional compensation method is calculated by (5).

$$row\#/frame = floor\left[\frac{t_{BLANK}}{3 \times t_{LINE} + t_{FDBACK}}\right]. \quad (5)$$

In this article, 10% inter-frame blanking period is selected for performance comparison. The number of rows calibrated per frame with the proposed compensation method is calculated by (6).

$$row\#/frame = floor\left[\frac{N}{K}\right]. \quad (6)$$

If the length of the calibration operation is longer than the inter-frame blanking period, no calibration operation can be performed by the traditional compensation method. For example, in the case of 160 μs feedback delay and 1% inter-frame blanking period as listed in Table 1, after adding three additional line-times for other steps of calibration operation, the total delay is longer than the inter-frame blanking period.

In Table 1, 10% inter-frame blanking period is assumed for performance comparison. For 20 μs feedback delay, the traditional design only calibrates 40 rows of pixel circuits per frame, while the proposed design calibrates 540 rows of pixel circuits per frame, which is ∼14x faster than the traditional design.

V. SIMULATION RESULTS

A circuit is built with a-IGZO TFT and a 0.25-μm CMOS process to demonstrate the idea of the proposed compensation method, as shown in Fig. 5. The circuitry is derived from [16]. The circuitry consists of four pixel circuits, a voltage source, a current copier, and a comparator. The current copier and the comparator from the feedback current sensing module. The pixel circuits are built with a-IGZO TFT and OLED process, while the other circuitry is built in CMOS process.

TABLE 1. **Performance comparison.**

	Design [8][9]			This work	
Frame frequency (Hz)	60				
Resolution	3840x2160				
Inter-frame blanking	1%	5%	10%	10%	
Inter-frame blanking length (us)	166.67	833.33	1666.67	1666.67	
Line-time (us)	7.64	7.33	6.94	5.56~6.68	
Feedback delay (us)	Row# / frame			K	Row# / frame
20	3	19	40	4	540
40	2	13	27	7	308
60	2	10	20	10	216
80	1	8	16	13	166
100	1	6	13	16	135
120	1	5	11	19	113
140	1	5	10	22	98
160	0	4	9	25	86

The operational amplifier (Amp) in the current copier is used to keep the voltage of feedback data line (v_FDBACK) close to the fixed reference voltage (Vref). The value of the fixed reference voltage (Vref) is configured to be 0.9 V which is lower than the threshold voltage of OLED. Therefore, the OLED is off during the current feedback period, so that all the current of TFT Q1 is sunk to the current copier. The feedback current (i_FB) is copied to the output (i_CP) of the current copier. The current i_CP draws the current from storage cap C1 and the fixed reference current (Iref) pumps into the storage cap C1. The voltage of C1 changes according to the difference between i_CP and Iref. The current comparator output tells if the feedback current (i_FB) is larger or smaller than the reference current (Iref).

The simulation waveform in Fig. 6 shows a complete three-step calibration operation of Pixel circuit 4 and display operation of Pixel circuit 1, 2, 3 and 4. At T2, all display scan lines (SCAN_1, SCAN_2, SCAN_3 and SCAN_4) turn on. The initial voltage 3.0 V is written into four pixel circuits. At T4, display scan line SCAN_4 turns on and performs the first step of calibration operation to write 3.4 V calibration voltage into Pixel circuit 4. From T5 to T7, feedback scan line FB_4 turns on. The second step of the calibration operation is performed to feedback the driving current of Q1 of Pixel circuit 4 to the current copier. Meanwhile, the display operation of writing display voltage 4.0 V into Pixel circuit 1, 2, and 3 is performed sequentially. At T8, feedback scan line FB_4 keeps on. The third step of the calibration operation is performed to compare the feedback current with the reference current Iref = 10.0 nA. The feedback current i_FB is 8.984 nA. Therefore, the voltage of C1 is increased slightly. DP is pulled high, while DM is pulled down after EN = 1 to enable the comparator. The result is captured by the Latch. Feedback scan line FB_4 turns off at the end of current comparison. At T9, the normal display data overwrite

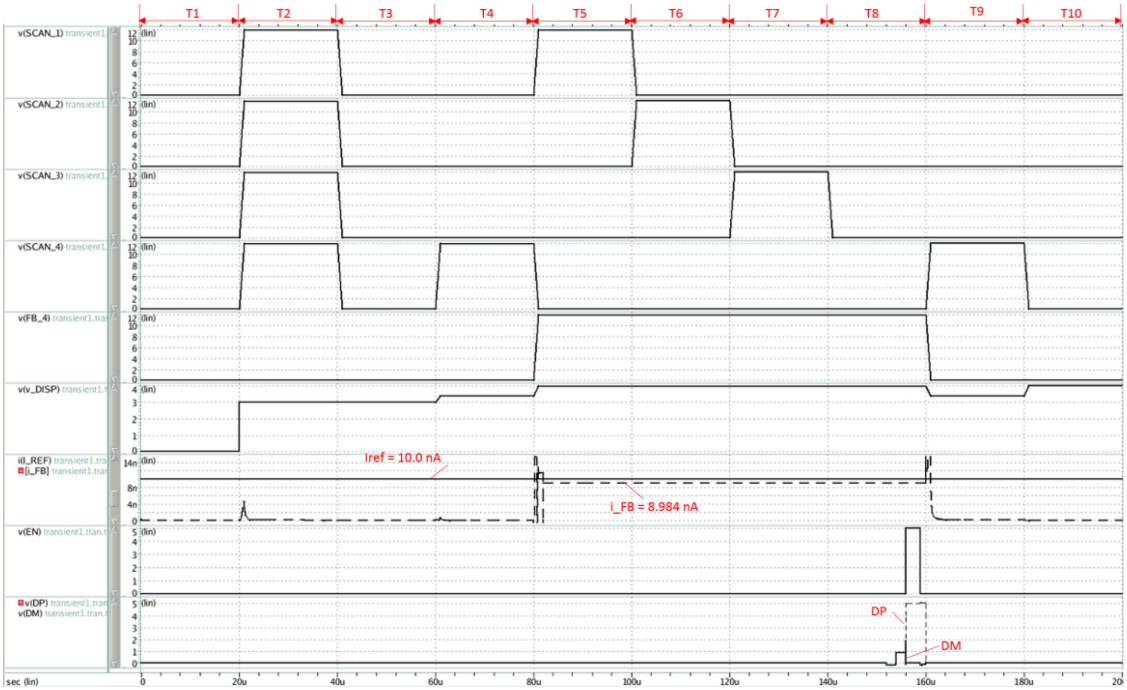

FIGURE 6. **Waveform of simulation results.**

the calibration data stored in Pixel circuit 4 before the end of the simulation.

VI. CONCLUSION

In this article, a new fast progressive compensation method is proposed for externally compensated AMOLED displays. The proposed method allows the calibration operation of pixel circuits to be performed during the display data updating period. The compensation of pixel circuits can progressively approach the compensated state much faster than the traditional method. The analysis result shows that the proposed compensation method is ∼14x faster than the traditional compensation method. The impact of the proposed method is negligible for large value of K which represents the length of feedback period of the calibration operation. The simulation result successfully demonstrates one complete iteration of calibration operation of a row of pixel circuits during display data updating period.

REFERENCES

[1] W.-J. Wu, L. Zhou, R.-H. Yao, and J.-B. Peng, "A new voltage-programmed pixel circuit for enhancing the uniformity of AMOLED displays," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 931–933, Jul. 2011.

[2] C.-L. Lin, T.-T. Tsai, and Y.-C. Chen, "A novel voltage-feedback pixel circuit for AMOLED," *IEEE J. Display Technol.*, vol. 4, no. 1, pp. 54–60, Mar. 2008.

[3] S.-J. Song, Y. Chen, J. Jang, and H. Nam, "Hybrid voltage and current programming pixel circuit for high brightness simultaneous emission AMOLED display," *IEEE J. Display Technol.*, vol. 11, no. 3, pp. 255–260, Mar. 2015.

[4] C. Wang, Z. Hu, X. He, C. Liao, and S. Zhang, "One gate diode-connected dual-gate a-IGZO TFT driven pixel circuit for active matrix organic light-emitting diode displays," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3800–3803, Sep. 2016.

[5] J.-P. Lee, H.-S. Jeon, D.-S. Moon, and B. S. Bea, "Threshold voltage and IR drop compensation of an AMOLED pixel circuit without a V_{DD} Line," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 72–74, Jan. 2014.

[6] W.-J. Wu *et al.*, "High-speed voltage-programmed pixel circuit for AMOLED displays employing threshold voltage one-time detection method," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1148–1150, Sep. 2013.

[7] C.-L. Lin, W.-Y. Chang, and C.-C. Hung, "Compensating pixel circuit driving AMOLED display with a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1166–1168, Sep. 2013.

[8] G. R. Chaji *et al.*, "Stable RGBW AMOLED display with OLED degradation compensation using electrical feedback," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2010, pp. 118–119.

[9] G. R. Chaji and A. Nathan, "A current-mode comparator for digital calibration of amorphous silicon AMOLED displays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 7, pp. 614–618, Jul. 2008.

[10] H.-C. Seol, J.-H. Ra, S.-K. Hong, and O.-K. Kwon, "An AMOLED panel test system using universal data driver ICs for various pixel structures," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 189–194, Jan. 2017.

[11] H.-J. In and O.-K. Kwon, "External compensation of nonuniform electrical characteristics of thin-film transistors and degradation of OLED devices in AMOLED displays," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 377–379, Apr. 2009.

[12] G. R. Chaji, S. Alexander, A. Nathan, and G. Church, "Low-cost AMOLED television with IGNIS compensating technology," in *SID Symp. Dig. Tech. Papers*, 2008, pp. 1219–1222.

[13] G. R. Chaji *et al.*, "Electrical compensation of OLED luminance degradation," *IEEE Electron Device Lett.*, vol. 28, no. 12, pp. 1108–1110, Dec. 2007.

[14] P. Gong and H. Li, "A novel compensation circuit for AMOLED source driver," in *SID Symp. Dig. Tech. Papers*, 2019, pp. 1026–1029.

[15] G. R. Chaji, "Thin-film transistor integration for biomedical imaging and AMOLED displays," Ph.D. dissertation, Elect. Comput. Eng., Univ. Waterloo, Waterloo, ON, Canada, 2008.

[16] J. Fan *et al.*, "A high accuracy current comparison scheme for external compensation circuit of AMOLED displays," in *SID Symp. Dig. Tech. Papers*, 2016, pp. 1261–1264.

[17] H. Luo, P. Wellenius, L. Lunard, and J. F. Muth, "Transparent IGZO-based logic gates," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 673–675, May 2012.

[18] F. D. Roose *et al.*, "A thin-film, a-IGZO, 128b SRAM and LPROM matrix with integrated periphery on flexible foil," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3095–3103, Nov. 2017.