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Ultrathin Sub-5-nm $Hf_{1-x}Zr_xO_2$ for a Stacked Gate-all-Around Nanowire Ferroelectric FET With Internal Metal Gate

SHEN-YANG LEE, CHIA-CHIN LEE, YI-SHAN KUO, SHOU-WEI LI, AND TIEN-SHENG CHAO

Department of Electrophysics, National Chiao Tung University, Hsinchu 30010, Taiwan

CORRESPONDING AUTHOR: T.-S. CHAO (e-mail: tschao@mail.nctu.edu.tw)

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ABSTRACT This study investigates a device's ability to boost its on-state current and subthreshold behavior using a ferroelectric field-effect transistor (FeFET) with an ultrathin sub-5-nm $Hf_{1-x}Zrx$O2 (HZO). A conventional field-effect transistor (FET) with pure hafnium (HfO_2) is used as a control measure and the impact of an internal metal gate (IMG) is also discussed. The study was conducted by using a sub-5-nm HZO and seed layer to fabricate a gate-all-around (GAA) nanowire (NW); a FeFET with a metal-ferroelectric–metal-insulator-semiconductor (MFMIS) structure; and a double layer (DL) of the channel. The channel size used in the experiment was approximately 9.6 × 16 nm^2 and the total thickness of the gate stack was 9.2 nm. This thickness is 50.5% less than our previous experiment. The FeFET exhibits a considerably high I_{on}–I_{off} ratio exceeding 107. The IMG serves as a potential equalizer and the ferroelectric material is arranged in a more symmetrical electric field. This results in a lower subthreshold (sub-V_{TH}) swing ($S.S._{min}$= 49.3mV/decade) with a wide range (10^3) of drain currentcompared to that without an IMG. The findings indicate that a high-performance GAA FET can be achieved by combining a DL channel, GAA NW, ferroelectric material, and an IMG.

INDEX TERMS Stacked channel, gate-all-around, nanowire, FeFET, Poly-Si, MFMIS, IMG, seed layer, HZO.

I. INTRODUCTION

Hafnium has been widely investigated in the semiconductor industry for several decades [1], [2]. Recently, the industry has evaluated technologies for the sub-5-nm node, with some researchers approaching 3 nm. Lowering the supplied voltage (V_{DD}) is one of the most effective methods for reducing power consumption. The subthreshold (sub-V_{TH}) swing ($S.S.$) must be optimized because lowering the V_{DD} can reduce standby power [3] The hafnium-based ferroelectric field-effect transistor (FeFET) is a contributing factor for a steep $S.S.$ (<60 mV/decade), and it assists in overcoming physical limitations [4], [5] In this study, $Hf_{1-x}Zr_xO_2$ (HZO) was utilized as a ferroelectric layer due to its small coercive field (E_C) and compatibility with complementary metal-oxide semiconductors (CMOS) [6]. When HZO is paired with a ZrO_2 seed layer (SeL), HZO can further enhance its non-centrosymmetric orthorhombic phase (o-phase) [7], [8]. The o-phase dominates the ferroelectricity and hysteresis loop in the ferroelectric material [9], [10]. Furthermore, the simulated results demonstrated that FeFET with an internal metal gate [IMG; i.e., a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure] can contribute a better sub-V_{TH} slope and on-state current than that with metal-ferroelectric-insulator-semiconductor (MFIS) structure [11]–[13].

However, the IMG in the MFMIM structure has been shown that retards the stabilization of NC effect whatever with single- and multi-domain Landau free energy potentials [14] Generally, to focus on the development of ferroelectric material to compatible with the current CMOS process, most of the researchers fabricate the planar capacitor with the MFM structure to investigate the ferroelectricity and try to optimize. On the other hand, there are still many papers that suggest the MFMIS structure. In addition, [15]

TABLE 1. Comparison between the thickness of the gate stack for the FeFET with an MFMIS structure in this and a previous study. Gate stack module was scaled by a factor of 50.5% for this study.

(nm)	[22]	This work	Scaled
SiO_2	3.8	2.3	39.4%
IMG	2.7	1.2	55.5%
SeL	2.4	1.1	54.1%
HZO	9.7	4.6	52.5%
Total	18.6	9.2	50.5%

indicates "The need for appropriate parasitic capacitance to avoid performance degradation in MFMIS NC FinFET was presented through the internal gate voltage estimation." It seems to us the connection between the result of the MFM structure and the NC-FET with the MFMIS structure should be further investigated and clarified. Therefore, we deduce that the result of MFM maybe shouldn't directly apply to MFMIS NC-FET owing to the capacitance matching between $C_{insulator}$ and $C_{semiconductor}$.

On the other hand, Poly-Si is a good candidate for vertical integration with the More than More (MtM) on portable electronic devices by using IoT applications. This is due to its easy-stacking ability, coupled with a simple, low-cost fabrication process [16]. The gate-all-around (GAA) architecture is preferred to the conventional FinFET (or Tri-Gate) structure because it enables better gate controllability. The most effective approach to increase the drain current (I_D) is by enlarging the effective channel width (W_{eff}). Stacking the multichannel vertically is the most efficient method if the same device footprint is used.

Furthermore, the fin pitch (FP) has an essential function in reducing cell size for logic circuits [17]. The developmental trend in the technology node has indicated that the FP decreases proportionately with the node size. The technology node reduces from 14 to 10 nm and then to 7 nm, whereas the FP has been scaled down to 48 [18], 36 [19], and 30 [20] nm. In our previous study [21], [22], we used an MFMIS device with a total stacked gate thickness of 18.6 nm. The FP was >37.2 nm when the multichannel scheme was implemented for performance improvement. Thick stacked gate dielectrics are not feasible for the 10-nm or the 3-nm technology node. Therefore, the total thickness of the stacked gate dielectrics was reduced by 50.5%, compared with our previous results related to maintaining the FeFET in line with the CMOS scaling trend. Moreover, HZO ferroelectric properties can be maintained when the thickness is scaled down to ultrathin sub-5-nm. The current findings will greatly facilitate the construction of 5-nm, perhaps even 3-nm, technology nodes in the future.

In our previous work [23], the device named "NC-FET" is a novel device at that time. However, the NC-effect is still improbable (is it just in the theoretical prediction or can be realized in reality?). In the same year, a new option from imec has been published in 2019 Scientific Reports [24], the author suggested the behavior of non-linear positive capacitance also can induce a body factor less than unity (observe in our previous publication [25]). Therefore, we named the device in this work "FeFET" and investigated the impact of Zr dopant and the internal metal gate of FeFETs

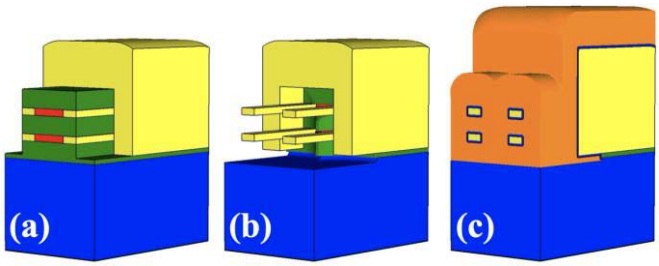

FIGURE 1. Schematic of the critical fabrication process of GAA FeFET with a DL channel. (a) Poly-Si RSD and channel were deposited via the LPVCD system, crystalized by the SPC process, and formed by the RIE process. Furthermore, the nitride and oxide layers were sequentially shrunk by hot H_3PO_4 in (a) and dilute HF in (b). (c) The FeFET fabrication process was terminated via the IL, gate dielectric, HZO layer deposition, and gate formation.

II. DEVICE FABRICATION

Fig. 1 illustrates the cross-sectional three-dimensional schematic images of the critical fabrication processes used in this study. The detailed device fabrication process is illustrated in [1] and [2]. Fig. 1(a) presents the channel and raised source/drain (RSD) was formed by the reactive ion etching (RIE) process after solid-phase crystallization (SPC). Fig. 1(b) demonstrates how the Poly-Si channel suspension process. It was conducted using hot phosphoric acid and dilute hydrofluoric acid. Thereafter, hot H_2O_2 solution was added to grow a thin chemical oxide layer with 1.2-nm-thickness, namely an interfacial layer (IL). Fig. 1(c) demonstrates that the atomic layer disposition was applied to the gate stack process. The gate stack configuration was comprised of IL/1.5-nm IMG/5-nm HZO/TiN for the FeFET with an MFMIS structure. The control measure (conventional FET) was also fabricated with an IL/5-nm HfO_2/TiN. Finally, the devices were terminated by the gate pattern and gate formation via the i-line stepper and RIE systems, respectively. In our fabrication process, we perform ion implantation with the element of P^{31+} and dosage of 5 10^{15} cm^{-2}. The thickness of the source and drain is 200-nm-thickness. In other words, the concentration of source and drain is around 2.5 10^{20} cm^{-3}.

III. RESULTS AND DISCUSSION

Fig. 2(a) illustrates the physical characteristics and shows the TEM cross-sectional images of the GAA DL NW FeFET with an MFMIS structure. This cross-section was taken along the A-A' section of the scanning electron microscopy (SEM) top-view profile depicted in Fig. 2(b). Magnification shows that the FeFET was stacked with a double-layer GAA channel and that the gate was formed all around the channel. The size of the channel was approximately 9.5 × 16 nm^2. Furthermore, energy-dispersive X-ray spectroscopy (EDS) mapping was used to verify the configuration of the stacked

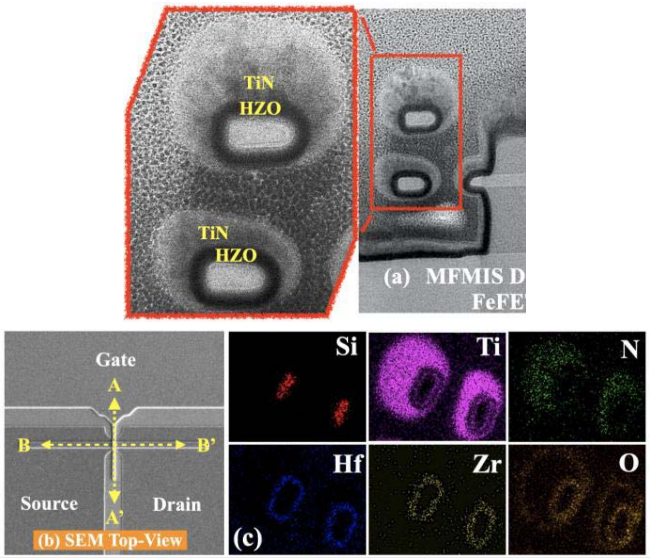

FIGURE 2. **(a) TEM cross-sectional images of the GAA DL NW FeFET with an MFMIS structure. (b) SEM top-view image with section A-A′. (c) The corresponding gate stack configuration is highlighted by EDS mapping.**

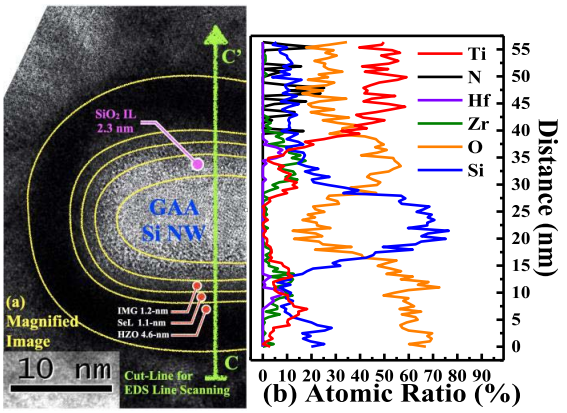

FIGURE 3. **(a) The magnification of a portion of the NW. The thickness of each layer is given. (b) The qualitative analysis from EDS along section C-C′.**

gate dielectrics, as shown in Fig. 2(c) The channel's configuration consisted of TiN/HZO/ZrO_2/TiN/SiO_2/Si and EDS mapping confirms that the TiN, IMG, and top metal gate covered the entirety of Si NW channels. Table 1 provides a comparison between this study and our previous work. Fig. 3(a) is a magnified image of a Si NW channel. A sub-5-nm (4.6-nm) HZO padded with a 1.1-nm ZrO_2 SeL, and a 1.2-nm IMG were identified. Fig. 3(b) provides a qualitative analysis of the elements in the gate stack configuration along section C-C'.

The electrical characteristics are illustrated in Figs. 4 and 5. Fig. 4(a) illustrates the $I_D - V_G$ curves of a conventional FET (pure HfO_2) with an MIS structure (control), and the FeFETs with MFIS and MFMIS structures. The I_D of the GAA FeFET with MFIS structure (blue line) is superior to that of a conventional FET (green line). This is a result of the dipoles in the additional ferroelectric material (HZO), which is directly stacked with an IL and Poly-Si nanowire (NW).

The corresponding $S.S. - I_D$ curves are plotted in the inset of Fig. 4(a). Based on the Gibbs free energy and L-K model [17], [18], the ferroelectric capacitor contributes to a negative differential capacitance regime. This can be stabilized by stacking with a dielectric capacitor. The value of $S.S.$ can be decreased by the lowering body factor and this is the reason that the NC effect can achieve an $S.S.$ of <60 mV/decade. The inset of Fig. 4(a) demonstrates the sub-V_{TH} behavior, the $S.S._{min}$ of FeFET with an MFIS structure ($S.S._{min}$ = 53.5 mV/decade) is better than that of a conventional pure HfO2 FET ($S.S._{min}$ = 84.5 mV/decade).

In addition, the V_D affects the potential distribution from source to drain. The electric field influences the behavior of dipole switching in the ferroelectric material of FeFET [11]. Inserting an IMG between the HZO and IL (MFMIS structure) can equalize the electric potential and create a more symmetrical electric field, which allows for uniform dipole switching.

Therefore, an IMG assists in increasing the I_D–V_G of a FeFET with an MFMIS structure [red line in Fig. 4(a)] when compared with a FeFET with an MFIS structure. The inset in Fig. 4(a) shows that for a wide range of I_D, the $S.S.$ ($S.S._{min}$ = 49.3 mV/decade) of the GAA FeFET with an MFMIS structure is lower than that with an MFIS structure. Uniform dipole switching induced by the IMG provides a negative differential capacitance regime and sub-V_{TH} behavior enhancement.

Fig. 4(b) presents the I_D–V_G curves of the MFMIS FeFET with a single and double layer. An additional layer of channel stacked directly on top of each other is the most effective method to increase the W_{eff} using the same footprint as SL devices. The FeFET with DL MFMIS structure provides a remarkable $I_{on} - I_{off}$ ratio over 7 orders of magnitude, where $I_{on} - I_{off}$ ratio is a quantity produced by the division of I_{max} ($V_G - V_{TH}$ = 2 V) and I_{min} ($V_G - V_{TH}$ = – 0.3 V). Fig. 4(c) is the $S.S. - I_D$ of GAA MFMIS FeFETs with single and double layer of channel. Owing to fewer domains in the ferroelectric material, SL FeFET provides more uniform dipole switching and results in a relatively better $S.S.$ compared to DL FeFET.

The stacking technology used in CMOS manufacturing can contribute to an increased current density that boosts performance. Ideally, the additional stacked channel in the DL device should provide twice as much current as the SL device. However, research has suggested that series resistance affects exponential growth.

The I_D–V_D of both the FeFETs with and without an IMG (MFIS and MFMIS structures) are illustrated in Fig. 5(a): the IMG for MFMIS FeFET assists in equalizing the potential and creating a symmetrical electric field in the HZO. The I_D shows a lower output resistance linearly and a higher on-state current. Fig. 5(b) illustrates the MFMIS FeFET with a SL and DL. The FeFET with a double layer has a more favorable current drain rate because of its enlarged W_{eff}. Practically speaking, the FeFET with a double layer can

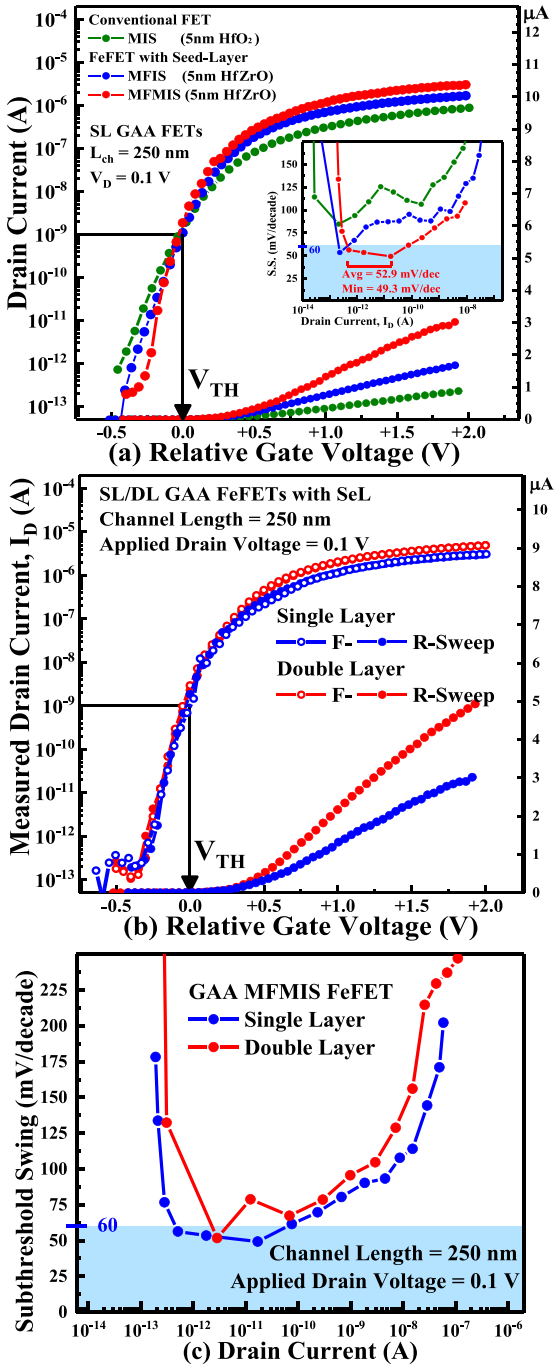

FIGURE 4. (a) The I_D–V_G curves of the FeFETs with MIS, MFIS, and MFMIS structures demonstrate improvement in I_D and sub-V_{TH} beavior with the presence of HZO and an IMG (V_D = 0.1 V for all curves). The inset illustrates the respective I_D – $S.S.$ curves. (b) The I_D – V_G of the FeFETs (i.e., the MFMIS structure) with a SL/DL of the channel indicates an improvement inI_D. (c) The $S.S.$ – I_D of GAA MFMIS FeFETs with single and double layer of channel.

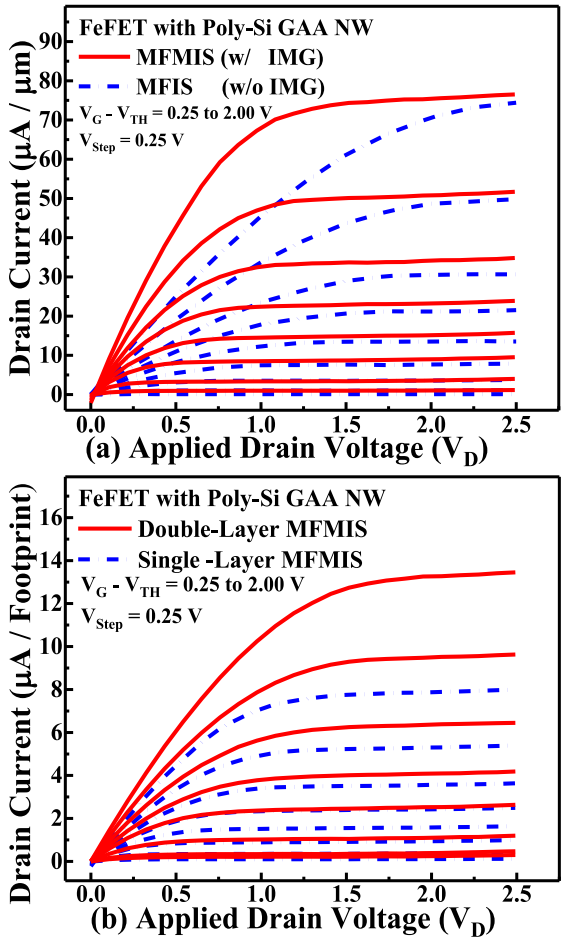

FIGURE 5. (a) The I_D – V_D of the FeFETs with an MFIS and MFMIS structure. The significant NC-related effect in the HZO boosts the $I_{D,sat}$ due to the uniform dipole switching induced by the presence of an IMG. (b) The I_D – V_D of the FeFET (MFMIS structure) with an SL/DL. The DL device can contribute additionalI_D using the same device footprint because of its enlarged W_{eff}.

improve the I_D by approximately 1.65 times more than a FeFET with a single NW region.

The trapping effect of the IMG for FeFET with MFMIS structure is shown in Fig. 6, and compared with the device with the MFIS structure. As we have known, the $|\Delta V_{TH}|$ is highly sensitive to the trapping effect. It seems to us that the conduction band of IMG is relatively lower than silicon nanowire and easily traps the electrons. In addition, the trapped electron might tend to concentrate in the IMG and create a similar $|\Delta V_{TH}|$; however, in the case of a device with MFIS structure, the position of the trapped electron is hard to be concerned about; it exhibits a wider distribution of $|\Delta V_{TH}|$. In this manner, the IMG can provide a certain degree of device-to-device variation. On the other hand, poly-channel is affected by grain boundaries and its crystallinity. In the near future, poly-channel can be crystalized vis metal-induced lateral crystallization (MILC) [26] process and combine with the filter effect [27] to improve the crystallinity and hamper the formation of grain boundaries.

On the other hand, we have not studied capacitance matching; in reality, the S-curve based on the L-K model is hard to be directly measured and detected even with the criteria of capacitance matching. Although, [28] reported the direct observation of NC-effect, which means the quasi-static NC (QSNC) is still a scientific controversy. Reference [29]

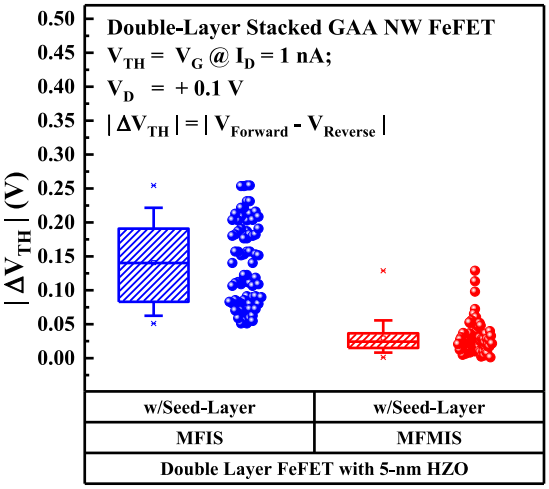

FIGURE 6. The absolute value of the difference of threshold voltage between forward and reverse sweep. In the case of "forward", the V_G is swept from 0 to positive; for the case of "reversed," the V_G sweeping starts from positive and goes back to 0. The threshold voltage is the gate voltage with the drain current of 1nA for both cases.

has experimentally demonstrated the observation of the NC-effect via the L-K model (assuming QSNC exists) and Miller model (assuming QSNC does not exist). So far, either of these approaches has been no scientific falsification. There is a new option from imec has been published on 2019 Scientific Reports [24], the author suggested the behavior of non-linear positive capacitance also can induce a body factor less than unity (in our previous work [25]). In this manner, we can achieve a swing of the FeFET below the physical limitation.

IV. CONCLUSION

This study effectively used a sub-5-nm $Hf_{1-x}Zr_xO_2$ to fabricate an MFMIS FeFET with a stacked DL GAA Poly-Si NW channel, and the GAA architecture is proper to the technology node below 5-nm. With the introduction of ferroelectric material, both the I_D and *S.S.* are superior to that of a conventional MIS FET. Even though, the thinner ferroelectric layer exhibits less ferroelectricity because of few dipoles in HZO, the FeFET still has notable electrical characteristics when HZO is reduced to <5 nm. However, the device with lower gate-insulator thickness is beneficial to further technology nodes. These characteristics can be further improved by inserting a SeL and an IMG. This results in an enhancement of HZO crystallinity and electric field symmetry. We find that the inserted IMG can hinder the device-to-device fluctuation as well. Furthermore, using a stacked channel is the most effective approach to increase W_{eff} (with the same device footprint) without negatively affecting the electrical properties. For the capacitance matching, we are going to perform a new experiment in the near future with different thicknesses of the interfacial layer.

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