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Planarized Trench Isolation of $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ Metamorphic High-Electron-Mobility Transistor by Liquid Phase Chemical Enhanced Oxidation

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ABSTRACT The liquid phase chemical enhanced oxidation (LPCEO) technique was applied to achieve planarized isolation of a high-indium-content $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ metamorphic high-electron-mobility transistor (MHEMT). Through a simple, low-temperature process not requiring costly machinery, electrical isolation of components was accomplished. In addition, multiple advantages were gained, including the production of planarized surfaces, low pollution, and reduction in the subsequent disposal of wet etching solution and costs for dry etching or ion implantation. Because of the decrease in lateral defect density caused by wet or dry etching and the further decrease in gate leakage current owing to the isolated oxide film, the performance of devices, with improved DC characteristics, less flicker noise, and enhanced high-frequency performance, can be increased.

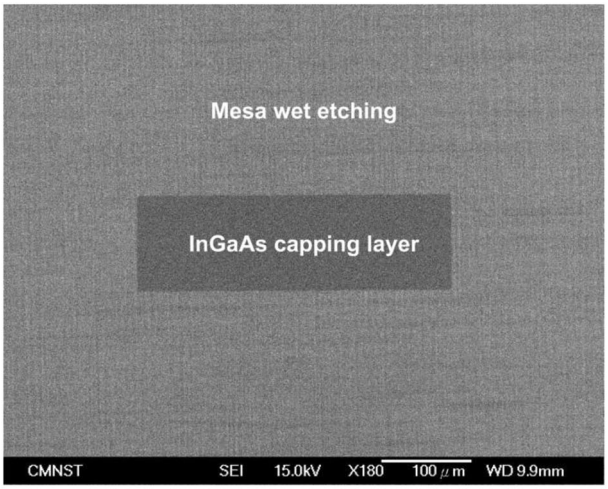
INDEX TERMS Isolation, metamorphic high-electron-mobility transistor (MHEMT), oxidation.

I. INTRODUCTION

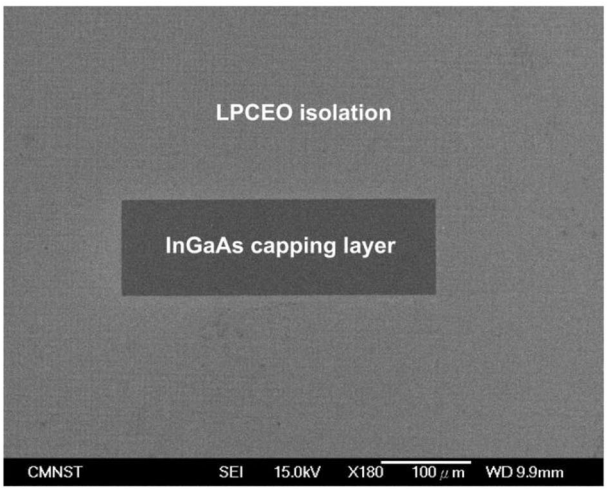
In the gallium arsenide (GaAs) integrated circuits (ICs) fabrication process, electrical isolation is necessary to reduce gate leakage current between components. To achieve a superior isolation effect, electrical insulating materials are typically adopted to space the components at specific distances. These materials include air, dielectrics, and semiconductor materials involving defects or doping with a deep-level impurity caused by ion bombardment. Mesa isolation [1]–[3] using air as the insulating material is the simplest approach. Specifically, isolation regions are etched deeply into the insulating substrates; therefore, the components are isolated in a pattern similar to islands. However, the surfaces of isolation regions produced using wet or dry etching are excessively heterogeneous in height, which is unfavorable for improving the photolithography resolution and reliability of metal interconnects.

A planarization isolation process provides the optimal conditions for photolithography imaging, facilitating the subsequent fabrication process. In addition, the planarization process can improve the reliability of metal interconnects and effectively enhance product density and functions. Chemical mechanical planarization (CMP) is currently a mainstream process for nanofabrication; however, the required equipment is complex and expensive. Moreover, using high-energy ion beams to perform ion bombardment or implantation (e.g., 100 keV to 5 MeV) on semiconductors has been widely studied. Again, however, the required equipment is complex and expensive, and the cost of machine maintenance is high [4]–[6].

Our previous studies have investigated an $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ metamorphic high-electron-mobility transistor (MHEMT) with an oxidized InGaAs as gate oxide [7], [8] through liquid phase chemical enhanced



(a)



(b)

FIGURE 1. Top-view SEM images of the samples (a) with mesa wet etching and (b) with LPCEO isolation before ohmic contacts.

oxidation (LPCEO) [9]. In the present study, we adopted the near-room-temperature technique to conduct a planarized component isolation of a Schottky-gate high-indium-content $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ MHEMT. Wu *et al.* [10] performed substrate isolation by employing a GaAs MOS field effect transistor (MOSFET) and compared the effects of the no isolation process, mesa isolation, and planar oxide isolation. Their experimental results revealed that ohmic resistance at the two ends after insulation was 10^6 times higher than that before isolation, and the effect of planar oxide isolation was comparable to that of mesa isolation. Notably, the degree of planarity obtained through planar oxide isolation was superior to that obtained from the nonplanar process of conventional wet etching. In other words, without mesa etching and by performing direct oxidation, the degree of surface planarity of oxide film was almost identical to that of the component capping layer. Moreover, the gate metal lithography and lift-off processes can be satisfactorily controlled, and the amount of waste wet etching solution can be reduced.

II. EXPERIMENTAL

The $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ MHEMT structure was grown through a molecular beam epitaxy system on a semi-insulating GaAs substrate. A 300-nm-thick InAlAs barrier layer was grown on a 300-nm-thick buffer layer, followed by a 6.5-nm-thick undoped high-indium-content $In_{0.8}Ga_{0.2}As$ channel layer, a 3.5-nm-thick undoped InAlAs spacer layer, a Si δ-doping (6×10^{12} cm^{-2}) layer, a 7.5-nm-thick undoped $In_{0.52}Al_{0.48}As$ Schottky layer, and a 10-nm-thick $In_{0.53}Ga_{0.47}As$ cap layer with an Si doping density of 5×10^{18} cm^{-3}. The measured electron mobility was 10700 cm^2/Vs, and the sheet electron concentration was 3.32×10^{12} cm^{-2} at room temperature.

Firstly, phosphoric acid-based etching solution was used to define the mesa pattern for reference samples; however, the experimental samples were immediately dipped into the LPCEO growth solution for 100 min to form the LPCEO isolation. More details regarding the preparation of the growth solution are in [7]. Briefly, device isolation is achieved through wet etching or LPCEO isolation individually. Figs. 1(a) and 1(b) present the top-view scanning electron microscopy (SEM) images of the samples with typical mesa wet etching and with LPCEO isolation before ohmic contacts, respectively. To ensure the isolation of individual elements for experimental samples, the oxidation process occurred at a sufficient depth, reaching at least the buffer layer. Thus, the objective of LPCEO isolation between individual active components was achieved. 370-nm-thick Au/Ge/Ni, 84:12:4 by percentage weight (not metal stack), ohmic contacts were formed through evaporation and then patterned by lift-off processes, followed by rapid thermal annealing at 370 °C for 30 s. After removing the InGaAs capping layer and part of the InAlAs layer by using phosphoric acid-based etching solution, 170-nm-thick Au was deposited as the gate. Figs. 2(a) and 2(b) present the cross-sectional structures of the Schottky-gate $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ MHEMT with mesa wet etching and with LPCEO isolation, respectively. The gate dimensions for each finger are 1μm(length) by 100 μm(width).

III. RESULTS AND DISCUSSION

Figures 3(a) and 3(b) demonstrate the measured transconductance g_m and the drain current density I_{DS} as a function of the gate-source bias V_{GS} at a fixed 1 V of drain-source voltage V_{DS} for MHEMTs with mesa wet etching and with LPCEO isolation, respectively. The peak g_m and the threshold voltage were 320 mS/mm (315 mS/mm) and −0.25 V (−0.35 V), respectively, for the reference (experimental) case. The maximal g_m and gate voltage swing (defined by a 10% reduction of maximal gm) were nearly identical for both devices.

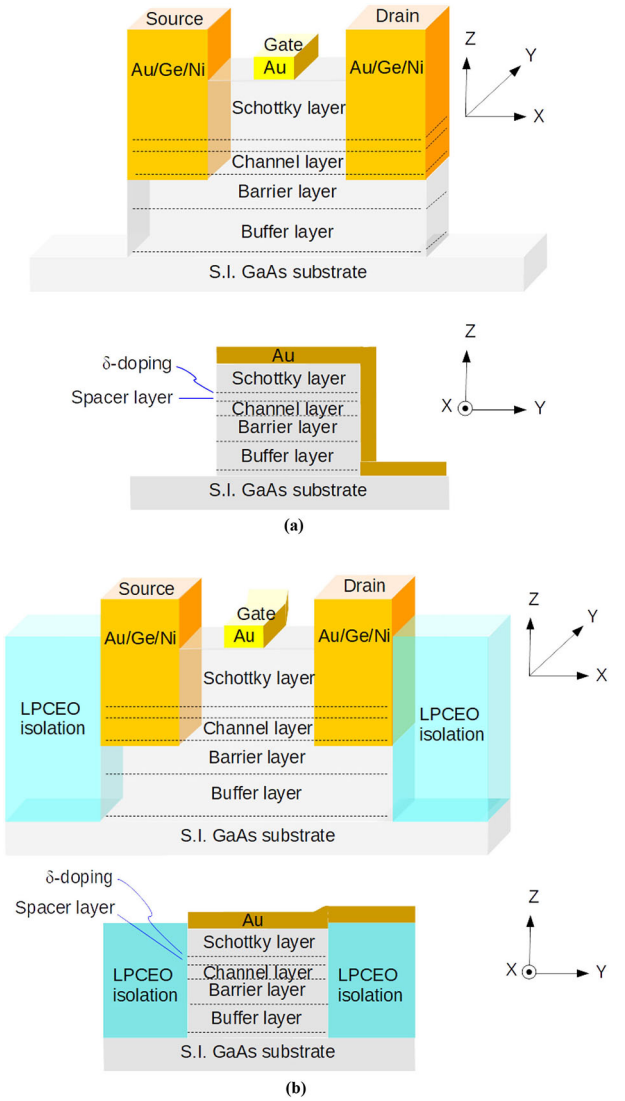


FIGURE 2. Schematics of the Schottky-gate $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ MHEMT (a) with mesa wet etching and (b) with LPCEO isolation.

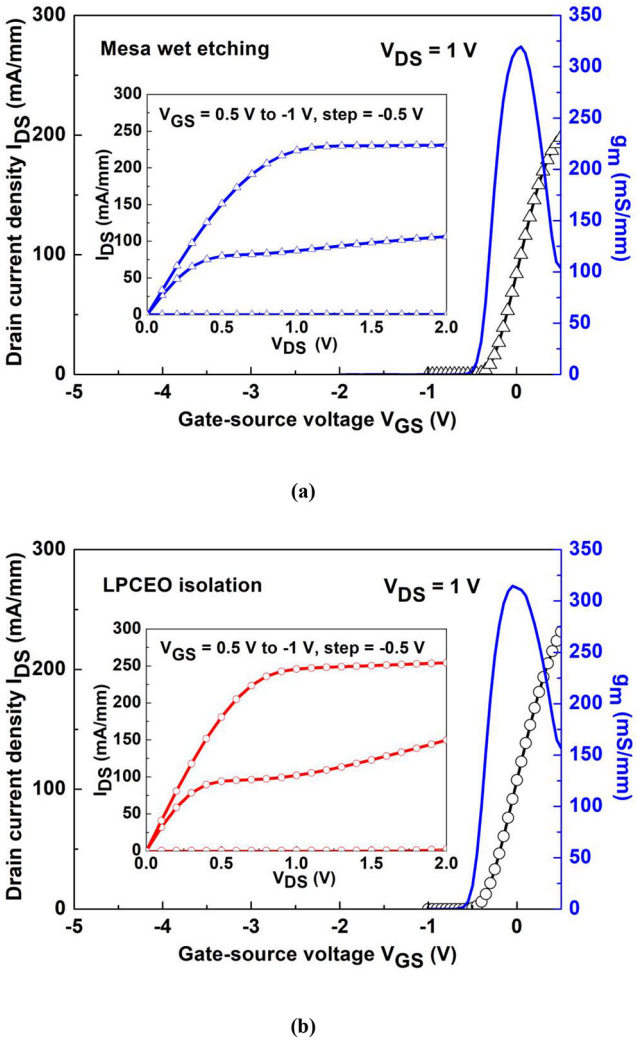


FIGURE 3. g_m and corresponding I_{DS}-V_{DS} characteristics for MHEMTs (a) without and (b) with LPCEO isolation.

The insets depict the corresponding I_{DS}-V_{DS} characteristics. The maximal I_{DS} was 254 mA/mm at V_{DS} = 2 V and V_{GS} = 0.5 V for the experimental case, which was higher than that (231 mA/mm) for the reference case at the same voltages, indicating superior charge control due to the decrease in leakage current. In addition, we observed that 100 min oxidation was necessary to ensure the leakage currents between adjacent mesa active regions were sufficiently low. However, if the oxidation time was 110 nm, the active region became smaller due to the consumption of the semiconductor layers during the lateral oxidation processes of the LPCEO, leading to a decrease of carriers in the channel, accompanied by the degradation of I_{DS} and g_m.

Subthreshold behavior is associated with the MHEMT structure, which determines the true off state of such devices and affects power dissipation within monolithic microwave integrated circuit. Figs. 4(a) and 4(b) display the subthreshold characteristics at V_{DS} = 0.1 V and 1.1 V of $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ MHEMT without and with LPCEO isolation, respectively. Subthreshold swing *SS*, 111 mV/dec to 121 mV/dec, of the experimental sample was superior to that (136-137 mV/dec) of the reference sample. The I_{ON}/I_{OFF} ratio (3.8×10^3 to 1.1×10^3) of the experimental sample was better than that (5.9×10^2 to 2.5×10^2) of the reference one. I_{ON} is defined as I_{DS} at V_{GS} equals threshold voltage+0.5 V, and I_{OFF} is defined as I_{DS} at V_{GS} equals threshold voltage−0.5 V. These results reveal that the LPCEO isolation can suppress *SS* through reducing the surface recombination current of LPCEO-grown oxide near the isolated sidewall of the mesa. In other words, the number of unwanted carriers flowing from the source terminal under the off state was decreased. The superior *SS* or I_{ON}/I_{OFF} ratio is owed to the suppressed leakage current density, and this trend is similar to the results in [11] and [12].

Fig. 5(a) presents a comparison of the two-terminal gate-drain diode characteristics. Fig. 5(b) depicts the magnified section of gate current densities versus reverse bias. The turn-on voltage V_{on} of experimental case, 0.55 V, was slightly

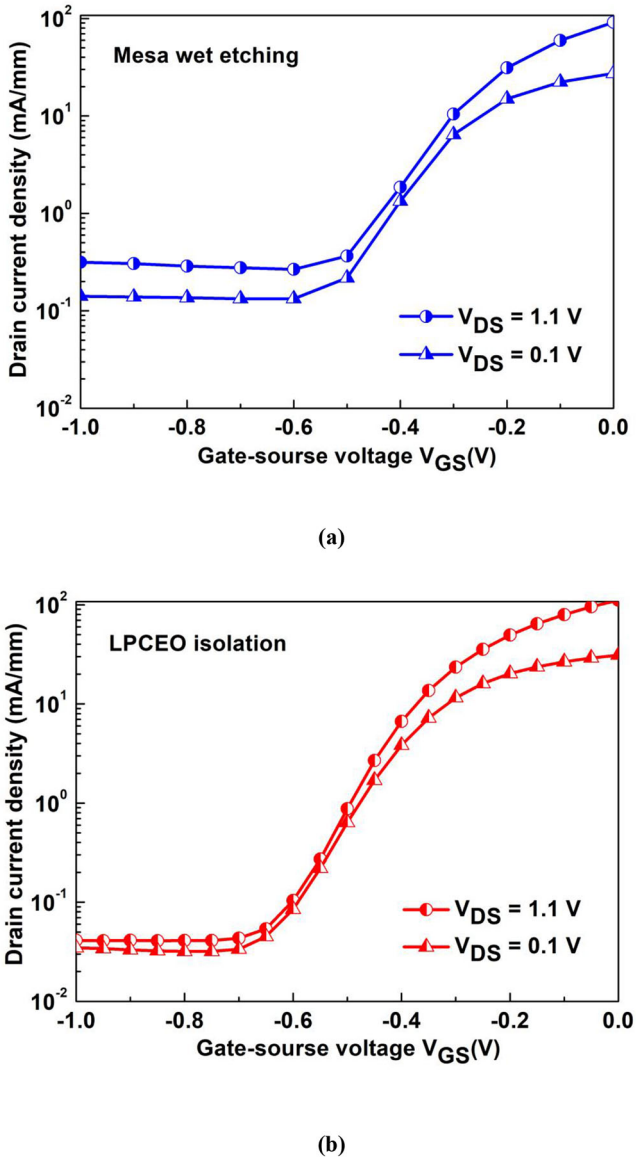


FIGURE 4. Measured subthreshold current density of MHEMTs (a) without and (b) with LPCEO isolation.

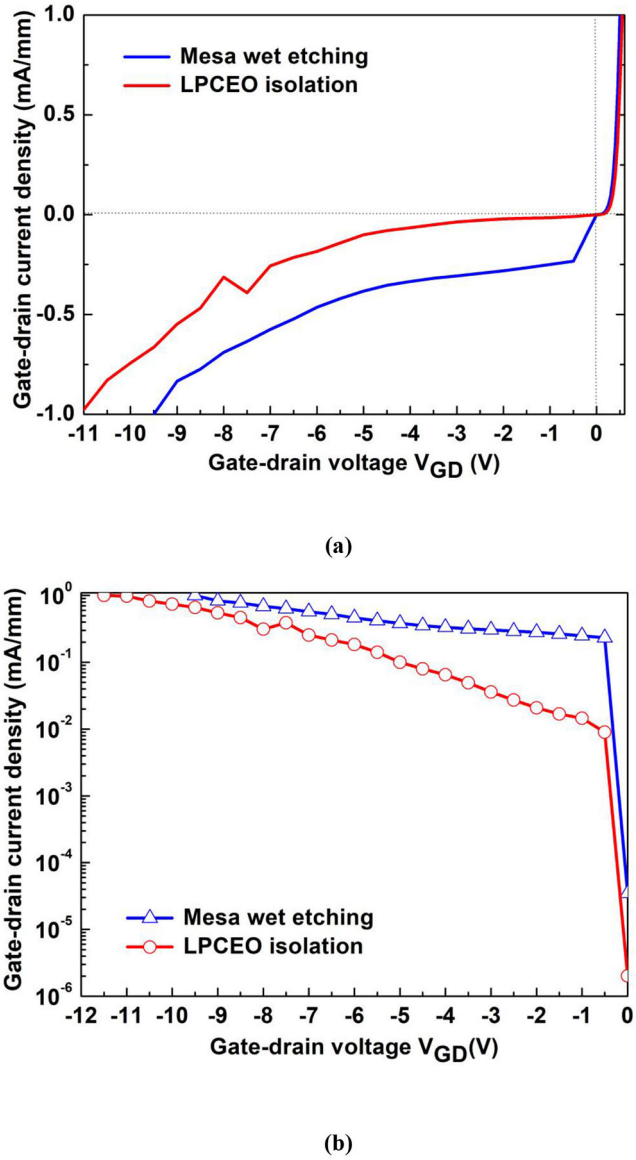


FIGURE 5. (a) Two-terminal gate-drain diode characteristics of both devices. (b) Magnified section of gate current density under reverse bias.

higher than that (0.5 V) of reference case. In the experimental sample, the reverse gate-drain breakdown voltage BV_{GD} was −11.5 V, and the corresponding gate current density was decreased by approximately one order of magnitude, which was superior to that (−9.5 V) of the reference sample because of the LPCEO isolation. V_{on} and BV_{GD} are defined as the bias at which the gate current density is 1 mA/mm. In general, a higher V_{on} accompanies a higher gate voltage swing. For the reference sample, a leakage current persisted between the gate terminal and the exposed InGaAs channel near the mesa sidewall [13], which can produce traps or defects, leading to an increased leakage current. The results demonstrate that the DC performance levels of the proposed MHEMT were not degraded when LPCEO isolation was used.

The gate current densities versus V_{GS} at distinct V_{DS} values were measured to obtain further insights into impact ionization phenomenon in the channel in both devices. Figs. 6(a) and 6(b) reveal that the gate current densities of the Schottky-gate MHEMT without and with LPCEO isolation were −0.6 mA/mm and −0.3 mA/mm at the maximal leakage current density with $V_{DS} = 1.6$ V, respectively. Electrons can achieve higher energy and generate electron-hole pairs through the impact ionization phenomenon, resulting in holes easily being injected into the metal gate [14]. In other words, hot-carrier-induced impact ionization results in a higher leakage density and a lower breakdown voltage. A bell-shaped curve is the typical signature of impact ionization [15], [16], which is triggered when the electrons are sufficiently hot to overcome the band gap. As detailed in Fig. 6(b), the electric

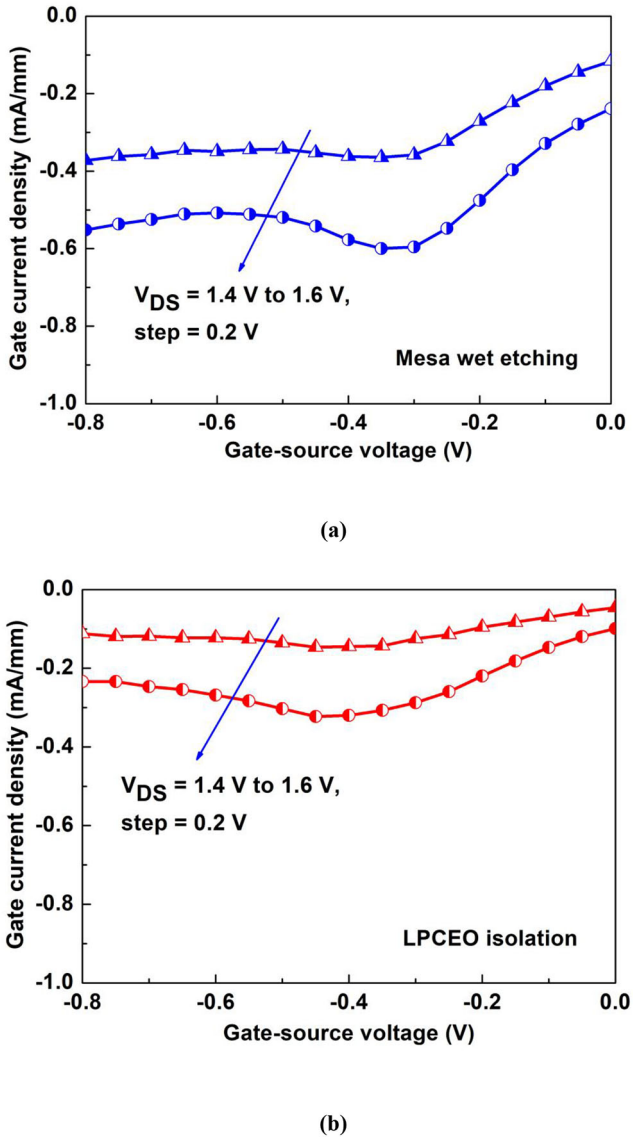


FIGURE 6. Gate current density as a function of V_{GS} at V_{DS} = 1.4 V and 1.6 V for MHEMTs (a) without and (b) with LPCEO isolation.

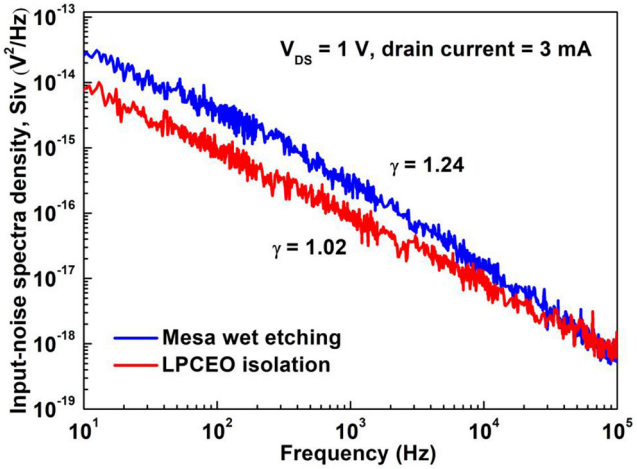


FIGURE 7. Measured flicker noise of MHEMTs with and without LPCEO isolation.

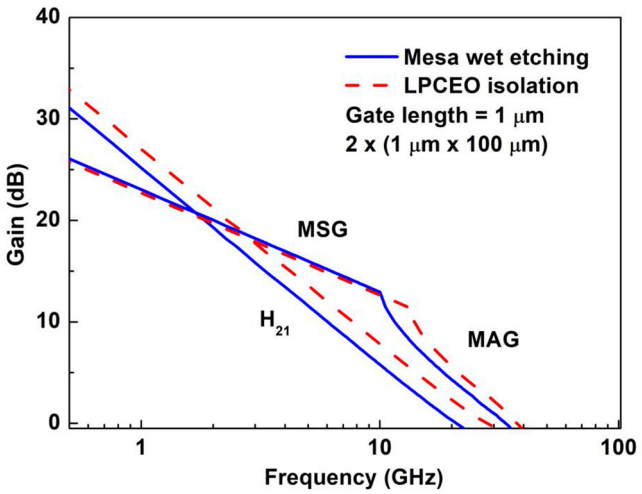


FIGURE 8. Microwave characteristics of both devices at maximum g_m measured from 0.5 GHz to 50 GHz.

field near the gate-drain area at the same voltages is markedly reduced compared with that of the reference sample due to the reduced leakage path of sidewall passivated by the proposed isolation process. Thus, LPCEO isolation results in an effective passivation and a more complete isolation around the active region that further suppresses the leakage current (Figs. 5 and 6).

Generation-recombination noise produced by the recombination centers and traps in the bulk on the mesa sidewall or at the metal/semiconductor interface, is related to low-frequency noise. Fig. 7 presents the low-frequency noise (i.e., flicker noise) of both devices was measured at V_{DS} of 1 V, and the drain current of 3 mA varied from frequencies of 10 to 10^5 Hz. Low-frequency spectral density (S_{iv}) is proportional to the value of $f^{-\gamma}$, where f stands for frequency and γ is the frequency exponent [17]. In the experimental case, S_{iv} was lower than that in the reference case across the range of frequencies, and the related values of γ were fitted as 1.02 and 1.24, respectively. Generally, a larger γ closely corresponded to generation-recombination noise. Because flicker noise was associated with defects within the MHEMTs, lower S_{iv} values imply that the LPCEO isolation was effective in suppressing defects or traps in the proposed devices. Therefore, the oxidized sidewall can satisfy the dangling bonds to eliminate surface or interface traps, with reduced flicker noise.

The unity-current-gain cutoff frequency f_T was obtained by setting the small-signal current gain H_{21} equals to unity. The maximum stable gain MSG, which is the maximum gain obtained from a transistor in combination with external matching impedances under the overall stability factor equals 1 at the operating frequency. The maximum frequency of oscillation f_{max} is defined as the frequency at which the maximum available gain MAG becomes unity. As shown in Fig. 8, the measured f_T and f_{max} values were

TABLE 1. Summary of device performance indicators for high-indium-content Schottky-gate InAlAs/InGaAs MHEMTs with and without LPCEO isolation.

LPCEO isolation	with	without
Maximum I_{DS} (mA/mm)	254	231
Maximum g_m (mS/mm)	315	320
V_{on} (V)	0.55	0.5
BV_{GD} (V)	-11.5	-9.5
SS (mV/dec)	111-121	136-137
I_{ON}/I_{OFF}	3.8×10^3 - 1.1×10^3	5.9×10^2 - 2.5×10^2
Frequency exponent γ	1.02	1.24
f_T	30	23
f_{max}	39	35

30 (23) GHz and 39 (35) GHz, respectively, at the maximum g_m with $V_{DS} = 1$ V for the Schottky-gate MHEMT with LPCEO isolation (vs. the reference MHEMT with mesa wet etching). The gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} were extracted from the S-parameters of the experimental sample ($C_{gs} = 0.334$ pF, $C_{gd} = 0.045$ pF) for comparison with those of the reference sample ($C_{gs} = 0.426$ pF, $C_{gd} = 0.041$ pF). The increased microwave performance levels of the proposed device may have resulted from the increased ratio of g_m to $(C_{gs} + C_{gd})$. Moreover, the reduced surface recombination may have contributed to the microwave performance levels. A similar trend was reported in [4] and [18].

We created 30 samples with and without LPCEO isolation. Under the same manufacturing process and parameters, but with different batches of samples, we chose the best value to determine the potential of the devices, which also conformed to the statistical trend. Regarding microwave characteristics, for the devices without LPCEO isolation, the f_T was distributed between 16 GHz and 23 GHz, and the f_{max} ranged from 26 GHz to 35 GHz. The mean f_T and f_{max} values were 19.8 GHz and 30.1 GHz with standard deviations of 1.4 GHz and 1.9 GHz, respectively. For the devices with LPCEO isolation, the f_T value was distributed between 22 GHz and 30 GHz, and the f_{max} value ranged from 32 GHz to 39 GHz. Mean f_T and f_{max} values were 26.1 GHz and 35.5 GHz with standard deviations of 1.7 GHz and 1.5 GHz, respectively. The best performance levels of the high-indium-content Schottky-gate InAlAs/InGaAs MHEMTs with and without LPCEO isolation in this work are summarized in Table 1. An LPCEO isolation structure is expected to result in reduced subthreshold swing, suppressed gate current density, improved flicker noise, and enhanced high-frequency characteristics. Multiple advantages can be gained, including the production of planarized surfaces, low pollution, and reductions in the subsequent disposal of wet etching solution and costs related to dry etching or ion implantation. Therefore, LPCEO isolation is favorable for subsequent photolithography and metal lift-off processes.

IV. CONCLUSION

The study demonstrated the applicability of the LPCEO technique for achieving planarized isolation in a Schottky-gate $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ MHEMT. Through a low-cost and low-temperature process that does not require expensive machinery, electrical isolation between the components was accomplished. Because of the decrease in lateral defect density caused by wet or dry etching and the further decrease in the gate leakage current, the overall performance of devices, involving suppressed leakage currents, less flicker noise, and enhanced high-frequency performance, can be increased.

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