Received 19 November 2020; accepted 29 December 2020. Date of publication 1 January 2021; date of current version 28 January 2021.
The review of this article was arranged by Editor C. Surya.

Digital Object Identifier 10.1109/JEDS.2020.3048721

Optimization of Photoelectron *In-Situ* Sensing Device in FD-SOI

J. LIU [1], K. XIAO [1], J.-N. DENG [1], A. ZASLAVSKY [2], S. CRISTOLOVEANU [3] (Life Fellow, IEEE), FY. LIU [4], AND J. WAN [1] (Senior Member, IEEE)

1 State Key Laboratory of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai 200433, China
2 School of Engineering, Brown University, Providence, RI 02912, USA
3 IMEP-LAHC, INP-Grenoble/Minatec, 38016 Grenoble, France
4 Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

CORRESPONDING AUTHORS: FY. LIU AND J. WAN (e-mail: liufanyu@ime.ac.cn; jingwan@fudan.edu.cn)

This work was supported by the National Natural Science Foundation of China under Grant 61904032.

ABSTRACT This article presents the optimization of a one-transistor active pixel sensor (1T-APS), known as the photoelectron *in-situ* sensing device (PISD) built in a fully-depleted silicon-on-insulator (FD-SOI) substrate. By employing TCAD simulation, we develop a physics-based model and systematically investigate the impact of six key parameters – gate oxide thickness, buried oxide layer, top Si layer, gate length, length of active region, and substrate doping – on the device's sensitivity and sensing range. Our comprehensive study provides guidance on the design of the PISD with the highest performance.

INDEX TERMS 1T-APS, FD-SOI, PISD, TCAD, sensitivity, sensing range.

I. INTRODUCTION

Decades of extensive research have produced a number of mature and multifunctional image sensing technologies [1]–[3]. In particular, the one-transistor active pixel sensor (1T-APS) occupies an important position in the image sensor family. Due to its small feature size, simplified structure and low power consumption, the 1T-APS promises a number of advantages over other photoelectron image sensors [4], [5]. Therefore, research into and applications of 1T-APS have been attracting much interest [6], [7].

Most traditional image sensors on the market can be classified as either CCD-based or CMOS-based, each with advantages and shortcomings. The CCD sensor provides high efficiency and fill factor, but suffers from charge loss and high power consumption [8]. In addition, random access cannot be achieved in the CCD due to the serial charge transfer mechanism. Conversely, the standard CMOS image sensor combines a photodiode with other transistors to realize random access, photodetection, and other functions, but suffers from a complicated cell structure [9]. To overcome these problems, we have proposed a 1T-APS, named the photoelectron *in-situ* sensing device (PISD) [10], and demonstrated it experimentally in a 22 nm FD-SOI technology [11]. The PISD integrates photo sensing, charge integration, buffer amplification, and random access in a 1T device without charge transfer or additional transistors.

The outstanding performance of the PISD originates fromits innovative operation principle [11], but it also depends on the device design. This work is dedicated to systematically studying the impact of various design parameters on the device performance. The six key design parameters are: the gate oxide thickness T_{OX}, the buried oxide layer (BOX) thickness T_{BOX}, the thickness of top Si layer T_{Si}, gate length L_G, active area length L_A, and substrate doping N_S. By combining TCAD simulation with a simple analytical model, we have studied the effect of these parameters on the sensitivity and sensing range of the device. Our results provide guidance on maximizing the performance of PISD for certain applications.

II. DEVICE STRUCTURE AND OPERATION MECHANISM

Extracted from [11], Fig. 1(a) illustrates the structure of the PISD. It is a conventional N-type FD-SOI MOSFET, with lightly P-type doped substrate and heavily N-type doped source/drain regions. To improve absorption, a large source/drain extension not covered by the contact (L_{gap}) is designed to allow light to reach the substrate, see Fig. 1(a). The device uses deep depletion in substrate for photoelectron conversion

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

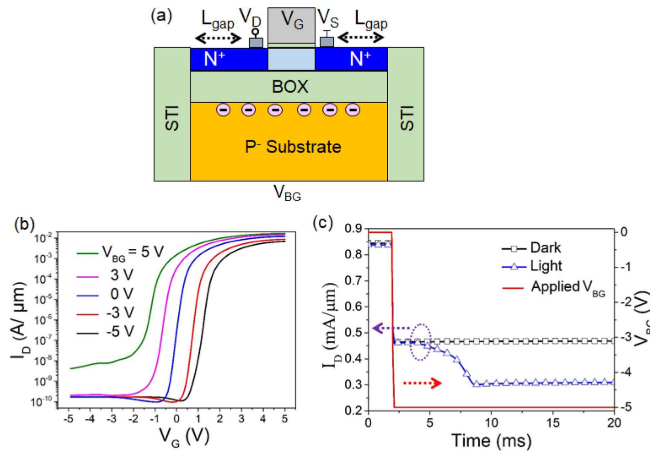

FIGURE 1. (a) The schematic view of PISD structure. (b) Transfer I_D-V_G characteristics under $V_D = 1.8$ V in DC mode for several values of V_{BG}. (c) Evolution of I_D in the dark and under illumination after a $V_{BG} = -5$ V pulse.

and the interface coupling effect in FD-SOI substrate for *in-situ* sensing [10]. The interface coupling effect as a function of V_{BG} is shown in Fig. 1(b). As the backgate voltage V_{BG} is made more negative, the threshold voltage V_{TH} of the top N-type MOSFET increases; whereas a positive V_{BG} reduces V_{TH}. This interface coupling effect is quite well-known and is currently used for V_{TH} tuning in FD-SOI MOSFETs [12]–[14].

The basic operation mechanism of the PISD is as follows. When a negative V_{BG} pulse is applied to the substrate, a deep-depletion region is formed at the BOX/substrate interface. Under illumination, photogenerated electrons in the depletion region are driven by the electric field to accumulate at the BOX/substrate interface. This negative charge increases the V_{TH} and reduces the drain current of the N-type channel through the interface coupling effect, shown in Fig. 1(b), providing a highly sensitive detection mechanism [11] in a single compact device. Experimental confirmation of the mechanism is shown in Fig. 1(c), which compares the evolution of I_D after a $V_{BG} = -5$ V pulse (at $t = 2$ ms) in the dark and under illumination with $\lambda = 520$ nm light at 20 μW/cm^2 intensity turned on between 4 and 9 ms [11].

The purpose of this work is to study the impact of specific parameters on the device performance and provide guidance for further optimization.

III. THE SIMULATION SETUP

The simulation is conducted in the Synopsys Sentaurus platform. Figure 2(a) shows the schematic structure of the PISD, indicating all the structural parameters we will investigate. The total pixel length L_P and width W_P are both fixed at 1 μm, see Fig. 2(a).

When operated as a photodetector, the drain and gate of the N-type FD-SOI MOSFET are biased at a fixed $V_G = V_D = 1.8$ V. An $R_L = 50$ kΩ load resistor, much higher than

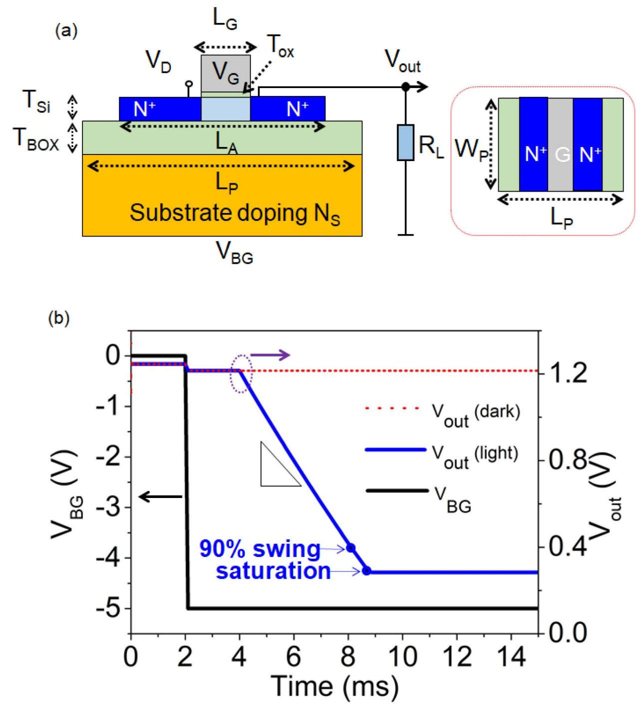

FIGURE 2. (a) Schematic diagram of the simulated device and the key parameters that impact the device performance; inset shows the top view of the device. (b) The evolution of V_{out} after a negative back-gate V_{BG} pulse is applied at time $t = 2$ ms and light is turned on at $t = 4$ ms.

the on-state channel resistance of the MOSFET, is connected to the source electrode. This configuration forms a source follower circuit that sets the output voltage to $V_{out} \cong V_G - V_{TH}$ [15].

To work as a PD, a negative V_{BG} pulse is applied at $t = 2$ ms to form the deep depletion region, as in Fig. 2(b). Exposing the device to illumination at $t = 4$ ms ($\lambda = 520$ nm, 1 mW/cm^2 intensity) generates photoelectrons in the deep-depletion region in the substrate, which increases V_{TH} in the top-channel MOSFET and leads to a corresponding decrease in V_{out}, as demonstrated by the simulation with $V_G = V_D = 1.8$ V in Fig. 2(b). The mechanism can also be understood by considering the BOX and the substrate depletion region capacitances in series. Together, they are equivalent to a thicker BOX, which weakens the impact of V_{BG} on V_{TH}. As the deep-depletion region shrinks due to electron accumulation under the BOX, the role of V_{BG} is enhanced. As soon as the inversion layer underneath the BOX is fully formed, equilibrium is reached and V_{TH} saturates.

According to $V_{out} \cong V_G - V_{TH}$, a fixed V_G and a linearly changing V_{TH} caused by the accumulated photoelectrons will lead to a nearly linearly changing V_{out} until V_{out} saturates after several ms as the density of photoelectrons stored at the BOX/substrate interface reaches its maximum value (full well capacity). The large change of V_{out} with exposure dose reveals two important figures of merit of the PISD: sensitivity (the slope of V_{out} curve as a function of optical exposure) and sensing range (exposure dose that saturates V_{out}), as

TABLE 1. Simulation scheme with parameter variation.

Simulated Device	T_{OX} /nm	T_{BOX} /nm	T_{Si} /nm	L_G /nm	L_A /μm	N_S /cm^{-3}
Device 0	5	20	6	50	1	10^{15}
Device 1	**1-7**	20	6	50	1	10^{15}
Device 2	5	**10-40**	6	50	1	10^{15}
Device 3	5	20	**6-100**	50	1	10^{15}
Device 4	5	20	6	**20-80**	1	10^{15}
Device 5	5	20	6	50	**0.2-1**	10^{15}
Device 6	5	20	6	50	1	**10^{15}-10^{17}**

shown in Fig. 2(b). A good image sensor should ideally exhibit both high sensitivity and a large sensing range.

Since many structural parameters could affect the performance of the PISD, we have chosen to focus on T_{OX}, T_{BOX}, T_{Si}, L_G, L_A, and N_S, all indicated in Fig. 2(a). These six parameters will impact on the deep-depletion effect and interface coupling effect employed in the PISD in various ways. Taking the T_{BOX} and N_S as examples, thinner BOX enhances the interface coupling effect and higher N_S reduces the deep-depletion region. The simulation scheme to study the impact of each parameter is specifically shown in Table 1. In order to understand the physical principles of 1-T APS, we scan the parameter values from the nominal values of the reference device 0 by varying one of the other six parameters (devices 1~6) while keeping the other five fixed at the nominal device 0 values. The nominal device 0 values are set close to the commonly used values in the advanced FD-SOI process to ensure the practical applicability of our simulation. The variation of sensitivity and sensing range of the PISD are then investigated as a function of parameter variation.

In order to gain physical insight into the impact of these parameters, we have also developed simplified models for sensitivity and sensing range, for comparison with the data extracted from simulation.

A. SIMPLIFIED MODEL OF SENSITIVITY

Figure 3 illustrates a simplified capacitance model used for the interface coupling effect which explains how the accumulated photoelectrons under the BOX/substrate interface modulate the V_{TH}. The capacitances C_{OX}, C_{Si}, C_{BOX} and C_{dep} are connected together in series, representing the capacitance per unit area of gate oxide, top silicon layer, buried oxide layer and depletion region, similar to the analysis of V_{TH} in conventional FD-SOI MOSFETs [16].

The accumulation of photoelectrons at the BOX/substrate interface changes the effective back-gate voltage by ΔV_{BG}. The corresponding change V_{TH} in the top channel can be estimated as:

$$\Delta V_{TH} = \Delta V_{BG} \times R \tag{1}$$

where R is essentially the capacitance divider ratio at point A in the equivalent circuit of Fig. 3:

$$R = \frac{\frac{1}{C_{ox}}}{\frac{1}{C_{ox}} + \frac{1}{C_{BOX}} + \frac{1}{C_{Si}}} = \frac{1}{1 + \frac{C_{OX}}{C_{BOX}} + \frac{C_{OX}}{C_{Si}}} \tag{2}$$

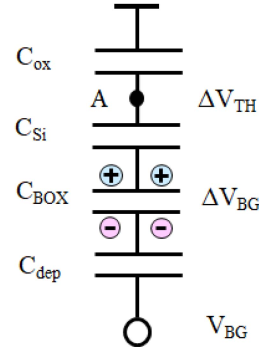

FIGURE 3. A simplified capacitance model for sensitivity calculation.

Substrate depletion capacitance C_{dep} does not appear in R due to the fact that photoelectrons are entirely accumulated by C_{BOX}, meaning that C_{dep} does not affect ΔV_{BG} or ΔV_{TH}. In turn, the ΔV_{BG} caused by the accumulated photoelectrons under the BOX/substrate interface, can be estimated as

$$\Delta V_{BG} = \frac{Q_{ph}}{S_{BOX} \times C_{BOX}} \tag{3}$$

where the S_{BOX} represents the effective area of the BOX capacitor. Considering the variation of the active area length L_A, the S_{BOX} can be described as the product of active area length L_A multiplied by its width W, *i.e.,* $S_{BOX} = L_A \times W$. The Q_{ph} is the charge induced by the accumulated photoelectrons under the BOX/substrate interface. Essentially, Q_{ph} is the product of exposure dose E multiplied by the quantum efficiency QE, *i.e.,* $Q_{ph} = E \times QE$. Combining Eqs. (2) and (3), Eq. (1) can be rewritten as

$$\Delta V_{TH} = \frac{E \times QE}{S_{BOX} \times \left(C_{BOX} + C_{OX} + C_{BOX} \times \frac{C_{OX}}{C_{Si}}\right)} \tag{4}$$

Finally, the sensitivity of the PISD, defined as the variation of V_{TH} per unit exposure dose, can be expressed as

$$\text{Sensitivity} = \frac{\Delta V_{TH}}{E} = \frac{QE}{S_{BOX} \times \left(C_{BOX} + C_{OX} + C_{BOX} \times \frac{C_{OX}}{C_{Si}}\right)} \tag{5}$$

Therefore, Eq. (5) represents a simplified model of the sensitivity and will be used to analyze the simulated sensitivity extracted from the slope of the $V_{out}(E)$ curve.

B. SIMPLIFIED MODEL OF SENSING RANGE

The sensing range is defined as the maximum exposure dose that the PISD can detect, as limited by V_{out} saturation illustrated in Fig. 2(b). It is determined by the corresponding maximum photoelectron charge that can be stored in C_{BOX}, *i.e.,* the full well capacity, roughly given by

$$Q_{max} = V_{BG} \times (S_{BOX} \times C_{BOX}) \tag{6}$$

According to equation (6), any variation in S_{BOX} or C_{BOX} due to changes in structural parameters will impact the sensing range. Thus, Eq. (6) will be used to analyze the sensing

range extracted from the simulation. For comparison purposes, the simulated sensing range is defined as the exposure needed to reduce V_{out} by 90% of its full swing, as shown in Fig. 2(b).

IV. SIMULATION RESULTS

In all six sets of simulations presented in Sections A through F below, the V_{BG} pulse is fixed at –5 V. The substrate depletion region formed by $V_{BG} = -5$ V can be on the order of a micron in a lightly-doped substrate, leading to significant absorption of wavelengths in the visible. Here, we choose the exposure wavelength of 520 nm and intensity of 1 mW/cm^2, modeled as a monochromatic source with an optical generation rate of 2×10^{19} cm^{-3}/s and the complex refractive index model employed for ray-tracing. Instead of utilizing the constant doping materials, the process simulator is employed to provide accurate profiles for all the doped regions. Our simulations use electric field and doping-dependent mobility, as well as SRH thermal generation-recombination with a carrier lifetime of 1 µs for 10^{15}-10^{17} cm^{-3} substrate doping.

A. DEVICE 1: IMPACT OF T_{OX}

The gate oxide layer in the MOSFET is important since it directly controls the on/off status of the device. Generally, thinner T_{OX} with higher capacitance is beneficial for the basic switching characteristics, such as lowering the subthreshold swing and reducing the off-state current. In low-power FD-SOI technology, the 28 nm FD-SOI device with very thin $T_{OX} \cong 2.8$ nm is operated at 2 V for IoT systems [17]. Here, we investigate the variation of sensitivity and sensing range of the PISD under $T_{OX} = 1, 2, 3, 5$ and 10 nm. Figure 4(a) shows the variation of V_{out} as the exposure *dose* (i.e., the product of time and light intensity) increases from 0 to 10 µJ/cm^2. The X axis is converted from the time in Figure 2(b) to the exposure dose to facilitate the calculation of the sensitivity from the slope of the V_{out}–exposure curve. The extracted sensitivity and sensing range are plotted in Fig. 4(b). Since thicker T_{OX} leads to a smaller C_{OX}, this will increase the capacitance divider ratio R factor of Eq. (2). Thus, larger shift of ΔV_{TH} and higher sensitivity are obtained.

On the other hand, the sensing range is nearly constant as the T_{OX} increases. This is because C_{OX} does not directly affect the well capacity Q_{max} according to Eq. (6). Consequently, T_{OX} has no apparent impact on the sensing range of PISD, with the V_{out} curves in Fig. 4(a) reaching saturation almost at the same exposure dose. Thus we find that thicker T_{OX} improves the sensitivity but not the sensing range.

B. DEVICE 2: IMPACT OF T_{BOX}

The buried oxide thickness T_{BOX} directly determines the BOX capacitance C_{BOX}, and thus can significantly impact on the sensing range and sensitivity. Under a $V_{BG} = -5$ V pulse, the T_{BOX} should not be too small to prevent the breakdown of the BOX. Figure 5(a) presents the variation of V_{out}

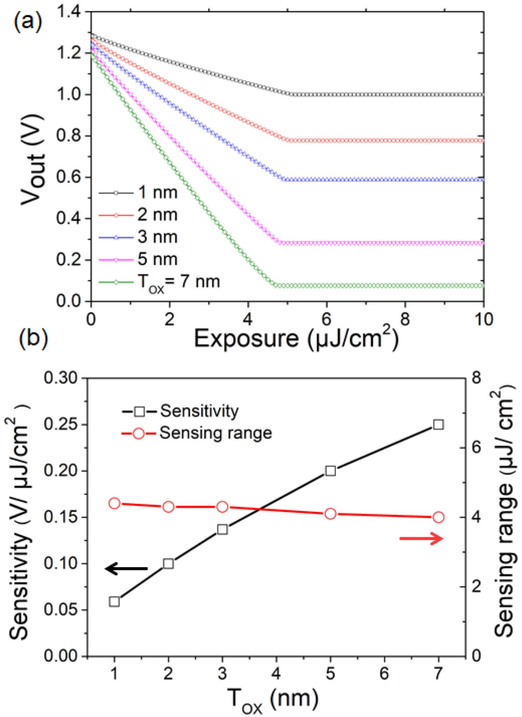

FIGURE 4. (a) V_{out} *vs.* exposure for different T_{OX} values. (b) The relation between sensitivity and sensing range and T_{OX}.

with the T_{BOX} ranging from 10 to 40 nm in 10 nm steps. The results reveal that devices with thicker T_{BOX} get saturated by a lower exposure dose. The sensing range varies from 5.8 to 2.2 µJ/cm^2 as T_{BOX} increases from 10 to 40 nm, since thicker T_{BOX} reduces C_{BOX} and thus leads to a reduction of Q_{max} in accordance with Eq. (6). Thus, increasing T_{BOX} yields a lower sensing range, as shown in Fig. 5(b). It should be noted that the measure of sensing range at $T_{BOX} = 10$ nm is restricted by the low supply voltage of 1.8 V. With a higher supply voltage of 3.3 V, the sensing range can be increased to 7.3 µJ/cm^2, as shown in Figs. 5(a) and (b).

As for the sensitivity, increasing T_{BOX} enhances the ΔV_{BG} according to Eq. (3). However, the voltage-drop ratio R is reduced as well, see Eq. (2). Thus, the impact of T_{BOX} on sensitivity is not significant. According to Eq. (5), increasing the T_{BOX} from 10 to 20 nm can only slightly improve the sensitivity. However, as T_{BOX} is increased beyond 20 nm, C_{BOX} becomes much lower than the C_{OX} for the 1∼7 nm range of T_{OX} we considered. In that case, Eq. (5) shows that the sensitivity is mainly determined by C_{OX} instead of C_{BOX}. As a result, large T_{BOX} values above 20 nm have no apparent impact on the sensitivity.

C. DEVICE 3: IMPACT OF T_{SI}

The top silicon layer can impact the sensitivity of PISD in various ways. On one hand, an increase in T_{Si} weakens the interface coupling effect and reduces the voltage-drop ratio R according to Eq. (3). Furthermore, a very thick Si layer can reduce the number of photons reaching the Si substrate, degrading the quantum efficiency QE in Eq. (5). Thus,

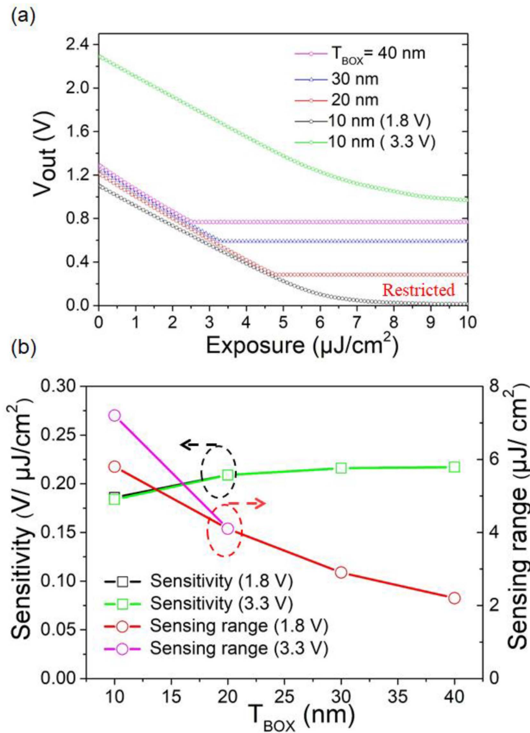

FIGURE 5. (a) The relation between V_{out} and exposure in device with $T_{BOX} = 10 \sim 40$ nm in 10 nm steps, combined with a $T_{BOX} = 10$ nm result for $V_G = V_D = 3.3$ V to show the full variation of V_{out} (green line). (b) Changes in sensitivity and sensing range caused by different thickness of T_{BOX} and supply voltages.

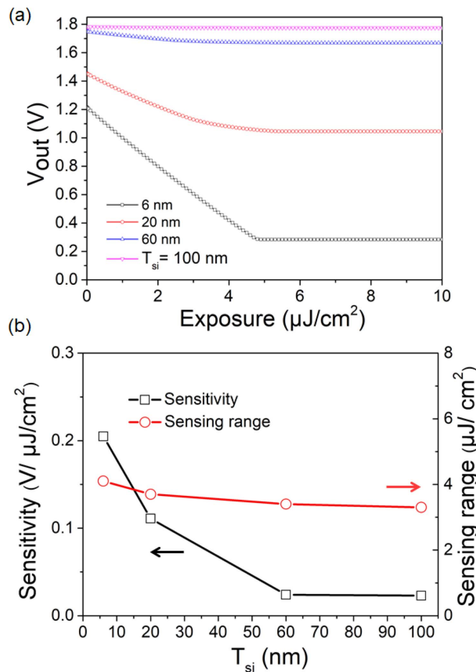

FIGURE 6. (a) V_{out} as a function of exposure for $T_{Si} = 6, 20, 60$ and 100 nm. (b) Sensitivity and sensing range *vs.* T_{Si}.

increasing T_{Si} markedly degrades the sensitivity, which falls markedly from 0.21 V/(μJ/cm^2) to as low as 0.02 V/(μJ/cm^2) as the T_{Si} increases from 6 to 100 nm, see Fig. 6(a).

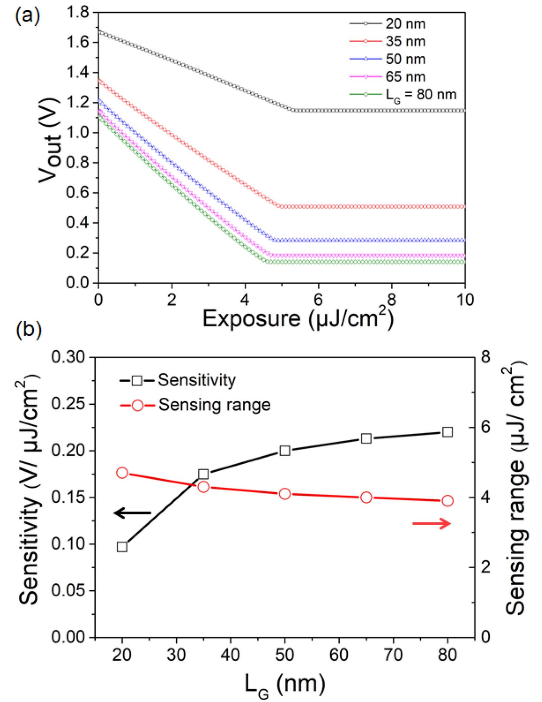

FIGURE 7. (a) V_{out} *vs.* exposure for $L_G = 20 \sim 80$ nm. (b) The variation of sensitivity and sensing range *vs.* L_G.

Conversely, the sensing range shows no apparent change in Fig. 6(b) because the well capacity Q_{max} is unaffected by T_{Si}, as predicted by Eq. (6).

D. DEVICE 4: IMPACT OF L_G

The impact of gate length L_G on the sensitivity is complex. On the one hand, the opaque aluminum gate blocks a portion of the light shining on the device and hence decreases the quantum efficiency QE, so a shorter L_G might be expected to enhance the performance for a fixed $L_P = 1$ μm pixel length. On the other hand, short channel effects (SCEs) can impact the transistor performance, depending on the operating voltage and other parameters. Therefore, a minimum $L_G = 20$ nm is chosen in the simulation to demonstrate the impact of the SCEs. Figure 7 compares the performance of devices with $L_G = 20 \sim 80$ nm with a step of 15 nm. The trends of V_{out} and extracted sensitivity/sensing range are shown in Figs. 7(a) and (b) respectively. Interestingly, the sensitivity exhibits no major changes in long-channel devices ($L_G = 50 \sim 80$ nm), whereas significant degradation is observed in devices with $L_G = 20$ and 35 nm. In short-channel devices, the control of the top channel by V_{BG} is dramatically impacted by charge sharing and fringing fields from source and drain through the BOX [18] that are ignored by our simplified model leading to Eq. (5).

To take the SCEs into consideration, the ΔV_{TH} in the equation (1) should be rewritten as

$$\Delta V_{TH} = \Delta V_{BG} \times R - \Delta V_{THsce}(L_G) \tag{7}$$

where the $\Delta V_{THsce}(L_G)$ presents the variation of ΔV_{TH} caused by the SCEs, as a function of gate length L_G. That

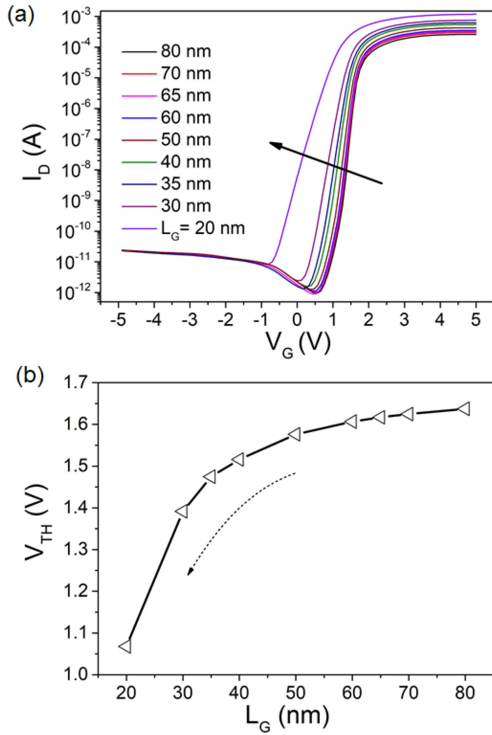

FIGURE 8. (a) I_D-V_G curves and (b) the roll-off of V_{TH} as L_G is decreased from 80 to 20 nm. The device with T_{Si} = 6 nm is simulated in the DC mode with $V_{BG} = -5$ V and $V_D = 0.1$ V with no illumination.

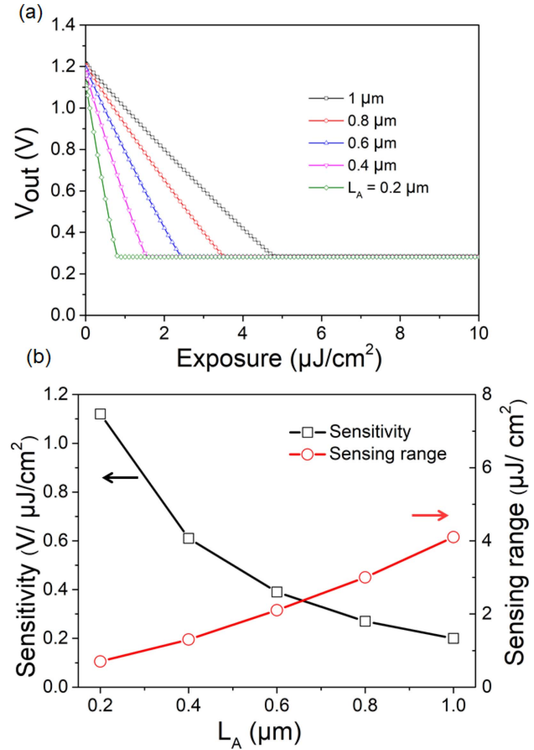

FIGURE 9. (a) V_{out} as a function of exposure when the active length L_A decreases from 1 to 0.2 μm in steps of 0.2 μm. (b) Sensitivity and sensing range *vs.* L_A in the 0.2–1 μm range.

is to say, the ΔV_{TH} of a short-channel device arises from two contributions: while ΔV_{TH} increases due to ΔV_{BG}, it is also reduced by the SCEs. According to the model in Reference [19], at sufficiently short L_G the $\Delta V_{THsce}(L_G)$ term will dominate. In this section, this happens in the devices with $L_G = 30$ and 25 nm, where the ΔV_{TH} is dominated by $\Delta V_{THsce}(L_G)$ rather than the $\Delta V_{BG} \times R$. Thus, while the reduction of L_G can slightly improve *QE*, significant degradation of the interface coupling effect caused by the SCEs still degrades the sensitivity. Changing L_G does not have much impact on the sensing range, see Fig. 7(b).

The short channel effects mentioned above can be observed by the drift of V_{TH} as L_G decreases, see Figs. 8(a) and (b). For long-channel devices, V_{TH} drops slightly, *i.e.*, from 1.64 V to 1.58 V as L_G is reduced from 80 to 50 nm. On the other hand, $\Delta V_{TH} = 0.41$ V as L_G is decreases from 35 to 20 nm, as shown in Fig. 8(b). This steep roll-off of V_{TH} for $L_G < 35$ nm confirms a severe short-channel effect that weakens V_{BG} control of the top channel and hence lowers the sensitivity.

E. DEVICE 5: IMPACT OF L_A

When the length of active region L_A is varied, the sensitivity and sensing range of the device change markedly, as shown in Fig. 9. Figure 9(a) shows that if L_A is reduced from 1 to 0.2 μm while maintaining the same total pixel length of 1 μm, V_{out} changes more abruptly and reaches saturation much earlier. This indicates higher sensitivity and lower sensing range of the PISD with shorter L_A. To understand the mechanism, we compare the distribution of photoelectrons for $L_A = 1$ and 0.2 μm in Figs. 10(a) and (b), respectively. If $L_A = L_P = 1$ μm, as in Fig. 10(a), accumulated photoelectrons are uniformly distributed under the BOX/substrate interface. By contrast, if $L_A = 0.2$ μm, as in Fig. 10(b), the photoelectrons generated over the entire pixel area except for the part covered by opaque gate are collected by the electric field of the top Si channel. As a result, a higher density of photoelectrons appears under the active region, which enhances the sensitivity of the device. This can be also explained from Eq. (5), in which shorter L_A leads to smaller effective area S_{BOX} and enhances the sensitivity. But there is a tradeoff, since smaller L_A and S_{BOX} also reduce the sensing range, see Fig. 9(b).

F. DEVICE 6: IMPACT OF N_S

As mentioned above, the operation mechanism of PISD is based on the deep-depletion effect in the substrate, where the photoelectrons are generated. The width of the depletion region for a given V_{BG} pulse depends on the substrate doping N_S. Figure 11 compares the hole density in the P-type substrate for $N_S = 10^{15}$ and 10^{17} cm^{-3}. Under the same backgate bias pulse of $V_{BG} = -5$ V, the hole density under the BOX/substrate interface in Fig. 11(a) is much lower than (b), which means a deeper depletion region is formed in the substrate with lower N_S. This is confirmed by the vertical hole density distribution profiles shown in

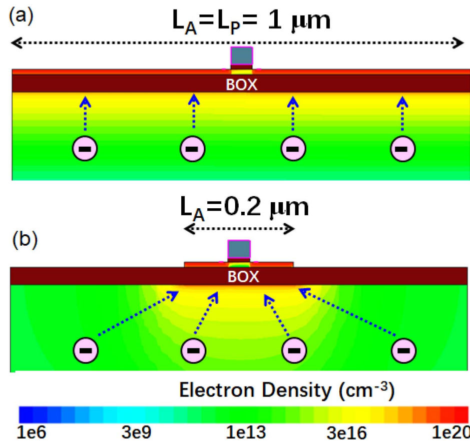

FIGURE 10. (a) Schematic view of saturated photoelectron distribution when (a) $L_A = L_P = 1$ μm and (b) $L_P = 1$ μm while $L_A = 0.22$ μm.

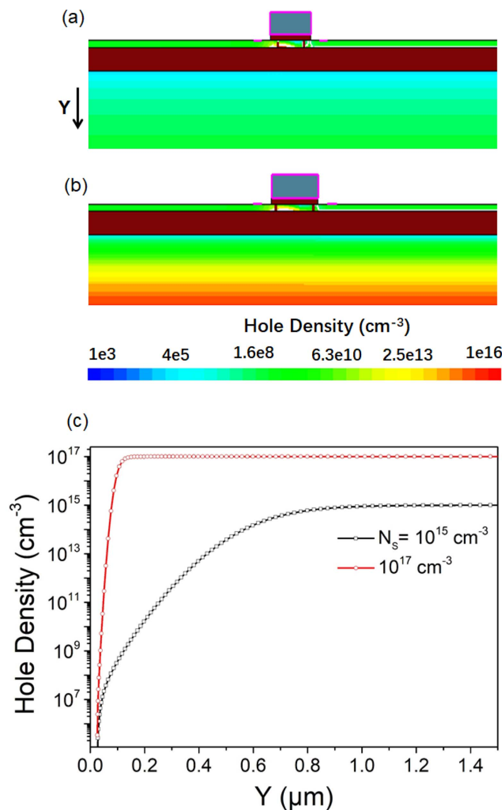

FIGURE 11. Hole density distribution in substrate with (a) 10^{15} cm^{-3} and (b) 10^{17} cm^{-3} P-type doping after saturation under the effect of light. (c) Hole density distribution profile under the BOX in the gate region in the vertical direction for $N_S = 10^{15}$ and 10^{17} cm^{-3}.

Fig. 11(c), which shows that the depth of depletion region in the lightly-doped substrate is 0.5 μm, much larger than the 0.06 μm seen in the more heavily-doped substrate. However, the 50 μm substrate thickness used in the simulations ensures that the substrate will not be fully depleted for any of the considered substrate doping concentrations.

Given a larger depletion region, more photons can be converted into photoelectrons. Thus, lower substrate doping leads to higher QE and higher sensitivity, according to Eq. (5). This is confirmed in Fig. 12(a), where devices with $N_S = 10^{15}$, 10^{16}, and 10^{17} cm^{-3} are compared. As expected, the sensitivity increases from 0.13 to 0.19 V/(μJ/cm^2) as N_S is reduced from 10^{17} to 10^{15} cm^{-3}. It is worth noting that commercial SOI wafers have low substrate doping which is favorable to PISD performance.

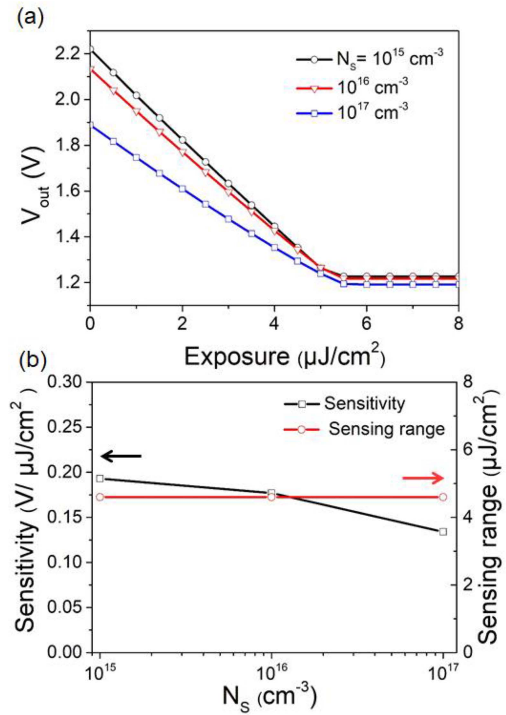

FIGURE 12. (a) V_{out} as a function of exposure *vs.* $N_S = 10^{15}$, 10^{16}, and 10^{17} cm^{-3}. (b) Sensitivity and sensing range *vs.* N_S.

TABLE 2. Simulation results of parameters.

Parameters	Sensitivity	Sensing range
Thicker T_{OX}	Higher	Not much change
Thinner T_{BOX}	Not much change	Higher
Thinner T_{Si}	Higher	Not much change
Longer L_G	Slightly Higher	Slightly lower
Shorter L_A	Higher	Lower
Lower N_S	Slightly Higher	Not much change

However, there is no direct relation between the depth of depleted region and the sensing range according to Eq. (6). Thus, as expected, changing N_S does not affect the sensing range of the device, see Fig. 12(b).

V. CONCLUSION

We have studied the impact of six key design parameters, enumerated in Table 1, on the performance of the PISD device. Our TCAD simulations and simplified capacitance models explain the effect of these parameters on the sensitivity and sensing range. The results are collected in Table 2. To summarize, sensitivity is higher in devices with thick T_{OX}, thin T_{Si}, short L_A and low N_S. Gate length L_G should be kept long enough to avoid short channel effects. To achieve a large sensing range, thin T_{BOX} and long L_A are the main parameters to be tuned.

Combining the advanced 22 nm FD-SOI fabrication process and our simulation results, the ranges of optimized parameters are as follows: thicker $T_{OX} = 5 \sim 7$ nm, thinner $T_{Si} = 6$ nm, longer $L_G = 30 \sim 50$ nm, and lower $N_S = 10^{15}$ cm^{-3} will contribute to the higher sensitivity target. At the same time, thinner $T_{BOX} = 10 \sim 20$ nm and longer $L_A = 1$ μm are conducive to obtaining a larger sensing range.

REFERENCES

[1] S. Xie, A. A. Prouza, and A. Theuwissen, "A CMOS-imager-pixel-based temperature sensor for dark current compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 2, pp. 255–259, Feb. 2020, doi: 10.1109/TCSII.2019.2914588.

[2] E. R. Fossum, "CMOS image sensors and the quanta image sensor," in *Proc. Int. Conf. Opt. MEMS Nanophoton. (OMN)*, Lausanne, Switzerland, Aug. 2018, pp. 1–5, doi: 10.1109/OMN.2018.8454568.

[3] B.-S. Choi *et al.*, "In-pixel aperture CMOS image sensor for 2-D and 3-D imaging," *IEEE Sensors J.*, vol. 18, no. 22, pp. 9163–9168, Nov. 2018, doi: 10.1109/JSEN.2018.2869383.

[4] N. T. Fourches, "Ultimate pixel based on a single transistor with deep trapping gate," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1619–1623, Apr. 2017, doi: 10.1109/TED.2017.2670681.

[5] K. Wang, X. Zhou, M. Zhang, Y. Xu, M. Wong, and H. S. Kwok, "A one-transistor active pixel sensor formed by a vertical photodiode-gated low-temperature polysilicon thin-film transistor," in *Proc. IEEE Int. Conf. Electron Devices Solid State Circuits (EDSSC)*, Shenzhen, China, Jun. 2018, pp. 1–2, doi: 10.1109/EDSSC.2018.8487133.

[6] J. Wan *et al.*, "Novel photodetectors and image sensors based on silicon-on-insulator substrate," in *Proc. Int. Conf. IC Design Technol. (ICICDT)*, Suzhou, China, Jun. 2019, pp. 1–2, doi: 10.1109/ICICDT.2019.8790932.

[7] N. Dagtekin and A. M. Ionescu, "Energy efficient 1-transistor active pixel sensor (APS) with FD SOI tunnel FET," in *Proc. Symp. VLSI Technol. (VLSI Technology)*, Kyoto, Japan, Jun. 2015, pp. T218–T219, doi: 10.1109/VLSIT.2015.7223681.

[8] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997, doi: 10.1109/16.628824.

[9] E. R. Fossum and D. B. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 3, pp. 33–43, May 2014, doi: 10.1109/JEDS.2014.2306412.

[10] M. Arsalan *et al.*, "A highly sensitive photodetector based on deepdepletion effects in SOI transistors," in *Proc. IEEE SOI 3D Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Burlingame, CA, USA, Oct. 2018, pp. 1–3, doi: 10.1109/S3S.2018.8640150.

[11] Y.-F. Cao, M. Arsalan, J. Liu, Y.-L. Jiang, and J. Wan, "A novel one-transistor active pixel sensor with in-situ photoelectron sensing in 22 nm FD-SOI technology," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 738–741, May 2019, doi: 10.1109/LED.2019.2908632.

[12] T. Ouisse, S. Cristoloveanu, T. Elewa, B. Boukriss, and A. Chovet, "Interface coupling effects in thin silicon-on-insulator MOSFET's," *Superlattices Microstruct.*, vol. 8, no. 1, pp. 111–116, Jan. 1990, doi: 10.1016/0749-6036(90)90286-G.

[13] H. K. Lim and J. G. Fossum, "Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983, doi: 10.1109/T-ED.1983.21282.

[14] A. Ohata, S. Cristoloveanu, A. Vandooren, M. Cassé, and F. Daugé, "Coupling effect between the front and back interfaces in thin SOI MOSFETs," *Microelectron. Eng.*, vol. 80, pp. 245–248, Jun. 2005, doi: 10.1016/j.mee.2005.04.075.

[15] D. Frohman-Bentchkowsky and L. Vadasz, "DC analysis of an MOS source follower," *IEEE J. Solid-State Circuits*, vol. 3, no. 3, pp. 306–307, Sep. 1968, doi: 10.1109/JSSC.1968.1049908.

[16] J. P. Mazellier *et al.*, "Threshold voltage in ultra thin FDSOI CMOS: Advanced triple interface model and experimental devices," in *Proc. 9th Int. Conf. Ultimate Integr. Silicon*, Udine, Italy, Mar. 2008, pp. 31–34, doi: 10.1109/ULIS.2008.4527135.

[17] P. Singh, "A 19nW, near-threshold to I/O voltage level shifter in 28nm FD-SOI using 1.8V/28Å device for IoT Systems," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4, doi: 10.1109/ISCAS.2018.8351054.

[18] T. Ernst, C. Tinella, C. Raynaud, and S. Cristoloveanu, "Fringing fields in sub-0.1 μm fully depleted SOI MOSFETs: Optimization of the device architecture," *Solid-State Electron.*, vol. 46, no. 3, pp. 373–378, Mar. 2002, doi: 10.1016/S0038-1101(01)00111-3.

[19] H. Miyamoto *et al.*, "Modeling of short-channel effect for ultra-thin SOI MOSFET on ultra-thin BOX," in *Proc. MEMS Fluidics Bio Syst. Med. Comput. Photon. NSTI Nanotechnol. Conf. Expo*, vol. 2. Washington, DC, USA, Jun. 2014, pp. 471–474.