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Extremely-Low Threshold Voltage FinFET for 5G mmWave Applications

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ABSTRACT An optimized doping process is used to achieve extremely-low threshold voltage (ELVT) FinFETs for low-power mmWave applications based on 12nm node technology platform. With the $V_{TH} \approx 100\text{mV}$ ELVT FinFET shows 15% I_{EFF} improvement at the same V_{DD} compared to its super-low threshold voltage (SLVT) counterpart, while mismatch and reliability performances are comparable. F_T/F_{MAX} of $\sim 305\text{GHz}/\sim 315\text{GHz}$ and comparable Maximum Stable Gain (MSG) to SLVT FinFET gives ELVT FinFET an advantage for mmWave 5G low-power applications. Local oscillator (LO) chain blocks are investigated as a circuit level example to confirm the benefits of ELVT FinFET. An optimized LO transmission Line (TL) driver using ELVT FinFETs results in $\sim 9\%$ and $\sim 8\%$ reduction in V_{DD} and power consumption respectively at the same phase-noise (PN) level as the SLVT based design. If operated at the same V_{DD} of 0.525V ELVT FinFET can improve the VCO Figure of Merit (FOM_{VCO}) by $\sim 2.8\text{dB}$.

INDEX TERMS FinFET, extremely-low threshold voltage, radio frequency, 5G, RF, mmwave, transceiver, voltage-controlled oscillator, oscillator chain.

Rapidly approaching sub-6GHz and mmWave 5G transition will transform our world to an environment in which everyone is connected to everything at all times. This requires innovative design tweaks to implement new low-power, low-cost devices, with high scalability and optimized battery lifetime for a variety of upcoming applications such as Internet of Things (IoT), autonomous vehicles, drones, smart cities, and even more power efficient cell phones [1], [2]. In this framework, Sub-6GHz 5G mobile architectures typically use a standalone hybrid transceiver with separate technologies which operate on the existing 4G bands (700MHz, 2.5GHz, etc.) and additional frequency bands between 3.3GHz and 5GHz while, 5G mmWave implementation uses frequency bands above 24GHz to enable extremely high data rate transmission [3]. This new system specifications will put severe pressure on the industry to adopt new devices to better serve the needs of various sub-sections of 5G mobile transceivers. For some time 28nm bulk CMOS has been the main technology platform for mobile phone transceivers [4], [5]. However, a recent transition to FinFET is enabling more digital content and additional low

power benefits for Analog and RF circuits [6]–[9]. In this context, a new low-power RF FinFET (ELVT) based on GLOBALFOUNDRIES 12nm node technology platform is fully investigated and compared with the existing SLVT FinFET in terms of DC/RF performance. Following sections explain, while the ELVT device can be implemented through minor process integration changes with no additional mask, i.e., minimum extra cost it can deliver better DC and RF performance compared to the SLVT FinFET for specific sub-6GHz and mmWave 5G transceiver applications.

I. DC PERFORMANCE

CMOS SLVT and ELVT transistors are integrated using 12nm node FinFET technology (see Fig. 1) for 1:1 direct comparison. ELVT FinFET is integrated by modifying the channel/halo doping of the existing SLVT FinFET to achieve the required V_{TH} reduction of $\sim 90\text{mV}$ and $\sim 70\text{mV}$ (statistical average) for NFET and PFET respectively. The mentioned threshold voltages are optimized to provide an $IDSAT$ and $IEFF$ boost of $\sim 10\%$ and $\sim 15\%$ at the same $V_{DD} = 0.8\text{V}$, nominal supply voltage for this technology,

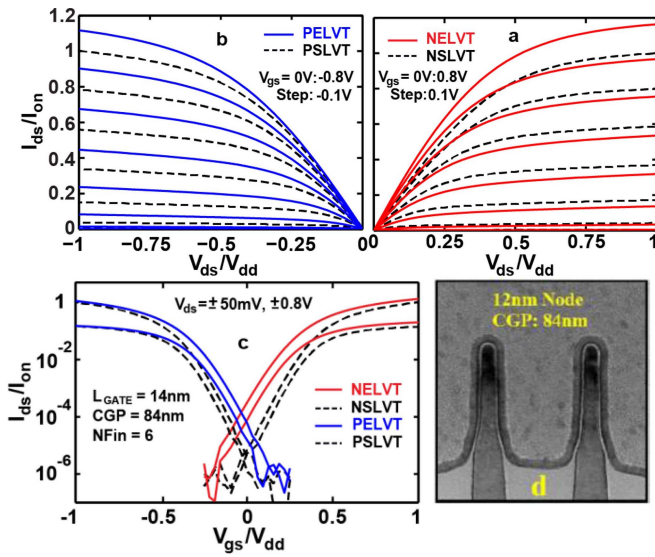


FIGURE 1. a) NFET and b) PFET Normalized output characteristics clearly show the ELVT ID_{SAT} and IE_{FF} boost of $\sim 10\%$ and $\sim 15\%$ c) Transfer characteristics confirm the V_{TH} reduction of $\sim 90mV$ and $\sim 70mV$ for NFET and PFET respectively, while DIBL values are in an adequate range for an Analog/RF transistor c) Cross-sectional TEM images of GLOBALFOUNDRIES 12nm node RF FinFET demonstrates a near perfection Fin profile [6].

TABLE 1. DC FoMs of 6-Fin $L_{GATE} = 14nm$ SLVT/ELVT FinFETs.

Parameter	NFET		PFET	
	SLVT	ELVT	SLVT	ELVT
VTSAT [mV]	181	87	151	77.4
IDSAT [$\mu A/\mu m$]	966	1078	908	1018
IEFF [$\mu A/\mu m$]	533	615	470	550
DIBL [mV]	35.3	57.2	46.2	59.6

for both NFET and PFET devices [10]. Fig. 1 compares the Output and Transfer characteristics of SLVT and ELVT FinFETs to highlight the performance improvements for various bias conditions. DC performance key *FOMs* are summarized in Table 1.

In order to confirm the electrostatic stability of the ELVT FinFET TCAD simulations are performed using Sentaurus device simulator [11]. Simulation results of Fig. 2 along with Table 1 indicate that while the required doping adjustments can provide the targeted on-state performance, the electric field line orientation in the channel shows no major change, i.e., negligible deterioration in device electrostatic conditions. DIBL values for ELVT FinFET are in an adequate range for an RF/mmWave transistor (see Table 1) [12].

II. RELIABILITY

To fully evaluate the reliability of ELVT FinFETs Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) reliability tests have been performed on SLVT and ELVT transistors by means of Constant Voltage Stress (CVS) where the stress was regularly interrupted to monitor the device performance parameters (V_{TH} for BTI and ID_{SAT} for HCI) over a stress time up to 10^4 seconds [13]. Normalized data on Fig. 3 show that BTI

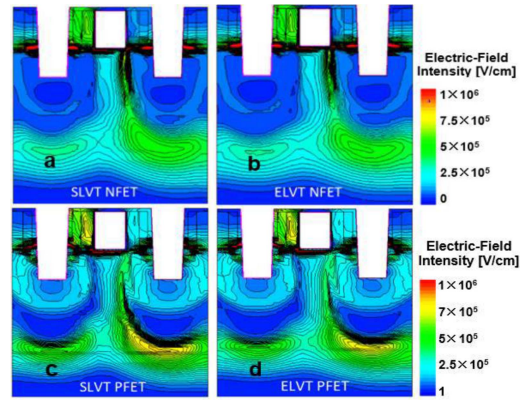


FIGURE 2. TCAD simulation results show the electric field intensity in the channel for a) SLVT NFET, b) ELVT NFET, c) SLVT PFET and d) ELVT PFET. Similarity of electric field line orientations in the channel confirms no major change in the device electrostatic conditions.

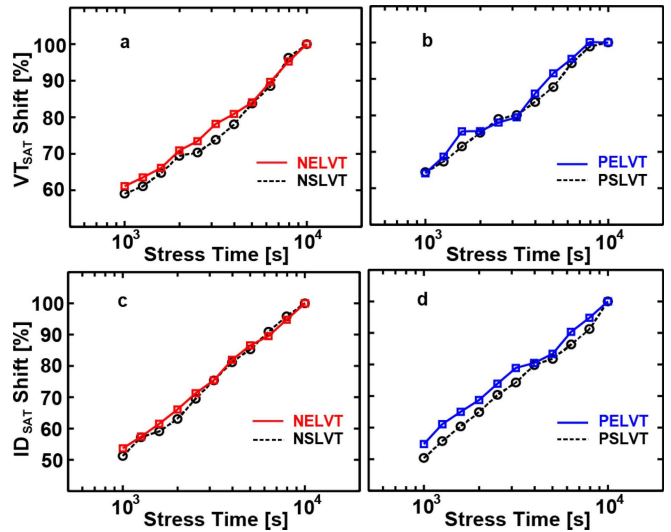


FIGURE 3. Normalized ELVT and SLVT a) NFET and b) PFET BTI show a comparable V_{TSAT} shift over 10^4 seconds stress time, while ELVT NFET c) and d) PFET HCI confirms similar or better ID_{SAT} degradation over the same stress time for 40-Fin, $L_{GATE} = 14nm$ anchor devices.

and HCI degradation trends follow the expected power law dependence over the defined stress time for both NFET and PFET devices [14]. Time slope does not depend on the threshold voltage flavor meaning for BTI and HCI the underlying physical degradation mechanism is similar for both devices. NFET BTI is mostly due to charge trapping in the gate dielectric, while PFET BTI is mostly due to interface degradation [15], while HCI is typically related to the interface degradation for both device types [16]. With regards to absolute level of degradation, the ELVT device shows improved or comparable BTI and HCI degradation compared to the SLVT case for NFET and PFET (see Fig. 3). It is concluded from the presented data that counter-doping has a negligible effect on either the gate vertical electric field that controls BTI or on the lateral electric field in the channel that controls HCI.

TABLE 2. Extracted A_{VT} and A_{β} for SLVT/ELVT 12nm node FinFETs.

	SLVT		ELVT	
	AVT [mV $\times\mu$ m]	A β [μ m \times 5%]	AVT [mV $\times\mu$ m]	A β [μ m \times 5%]
NFET	0.8	0.17	1.2	0.18
PFET	1.1	0.23	1.1	0.22

III. MISMATCH

Precision of analog and RF integrated circuit building blocks is significantly impacted by the mismatch of identically designed transistors in close proximity, therefore the mismatch characteristics of the ELVT device is investigated and benchmarked against the reference SLVT transistor. Specifically, threshold voltage $\Delta V_{T_{SAT}}$ and current factor differences $\Delta\beta$ ($\beta = \mu C_{OX}W/L$) of matched pair of transistors are compared in this context. Equations 1 and 2 are used to extract A_{VT} and A_{β} values from the hardware based on standard deviation trends (σ) of $\Delta V_{T_{SAT}}$ and $\Delta I_{D_{SAT}}/I_{D_{SAT}}$ versus $1/\sqrt{LW}$ for ELVT and SLVT devices with $L_{GATE} = 14$ nm and different number of Fin [17], [18]:

$$\sigma^2(\Delta V_{VT}) = \frac{A_{VT}^2}{W.L} \quad (1)$$

$$\left(\frac{\sigma(\Delta I_D)}{I_D}\right)^2 = \frac{A_{\beta}^2}{W.L} \quad (2)$$

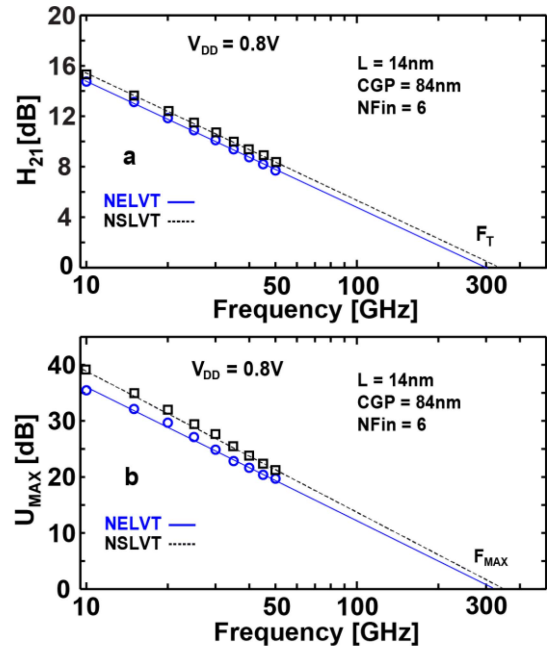
Summarized results in Table 2 indicate comparable mismatch characteristics for SLVT and ELVT transistors. Larger V_{TH} mismatch in ELVT NFET is expected from movement of extra As dopants in the channel. ELVT PFET shows no degradation in mismatch due to less movement of larger BF_2 dopants.

IV. HIGH FREQUENCY PERFORMANCE

In order to quantitatively compare the RF performance of SLVT and ELVT FinFETs the F_T , F_{MAX} , and MSG have been extracted from S-Parameters for both NFET and PFET [19]. S-Parameter measurements are performed in the frequency range of 1-50GHz. Effect of pad and interconnect parasitics has been eliminated using Open-Short de-embedding technique at the M1 metal level to precisely characterize the device intrinsic high frequency behavior [20], [21].

F_T and F_{MAX} values are extrapolated from Unity Current Gain (H_{21}) and Unilateral Power Gain (U_{MAX}) curves respectively using linear regression [22], [23]. Devices are biased in saturation, while Gate bias is adjusted to attain peak transconductance values. Fig. 4 shows example plots of H_{21} and U_{MAX} for 6-Fin SLVT and ELVT NFETs. MSG can be directly calculated from S-Parameters ($|S_{21}|/|S_{12}|$) for a specific frequency at the same bias condition. Extracted RF FOMs are summarized in Table 3 for direct comparison.

F_T is directly proportional to G_M , i.e., number of Fins [19]. Inverse dependency of F_{MAX} on number of Fins is well-known and due to the direct relation of R_{GATE} with number of Fins [8]. ELVT FinFETs show less than $\sim 5\%$ and $\sim 10\%$ F_T and F_{MAX} reduction respectively, when statistical median is taken into account. This behavior can be

**FIGURE 4.** a) Unity Current Gain (H_{21}) and b) Unilateral Power Gain (U_{MAX}) values extracted from S-Parameter measurements up to 50GHz. Linear regression is used to extrapolate the F_T and F_{MAX} values for SLVT and ELVT transistors.**TABLE 3.** Summarized RF FoMs for SLVT/ELVT 12nm node FinFETs.

		SLVT		ELVT	
		6-Fin	10-Fin	6-Fin	10-Fin
NFET	FT [GHz]	332	343	302	335
	FMAX [GHz]	346	298	314	262
	MSG	15.9	15.8	15.6	15.5
PFET	FT [GHz]	282	301	283	297
	FMAX [GHz]	323	256	298	246
	MSG	14.7	15.1	14.9	15.2

explained by the nature of the counter doping process and its effect on G_M and overlap capacitances. ELVT MSG also shows ~ 0.3 dB decrement for NFET, while PFET MSG is in the same range for both devices. Mentioned reductions in RF FOMs are considered negligible for sub-6GHz and mmWave applications targeted by the ELVT FinFET. Fig. 5 shows the normalized full-range F_T and F_{MAX} (sample median) versus gate voltage (V_{GS}) plots for 6-Fin $L_{GATE} = 14$ nm devices (see Fig. 1) for more assessment. Although, peak values are slightly lower for the ELVT FinFET but this device clearly has an advantage at near threshold bias points, which are targeted by low-power applications such as wearable electronics in which battery lifetime is critical.

V. CIRCUIT AND SYSTEM PERFORMANCE

Power consumption has become a critical design metric in many emerging multi standard wireless applications. In variety of 5G mmWave and radar transceivers LO chains are an inevitable part of the Multi-Input-Multi-Output (MIMO) and Multi-Channel Beamforming designs responsible for distributing the signal to several RF blocks. Due to their high

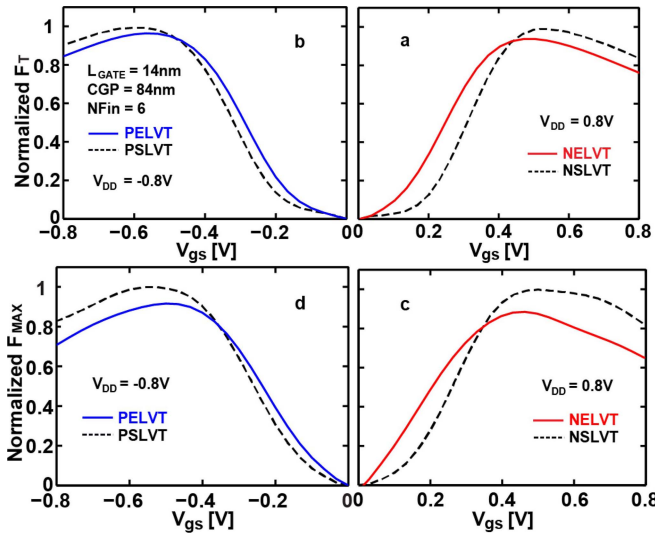


FIGURE 5. Normalized ELVT and SLVT NFET a) and c) and PFET b) and d) show less show ~5% and ~10% degradation in peak F_T and F_{MAX} (sample median) respectively. However, ELVT FinFET shows better performance at near threshold bias points.

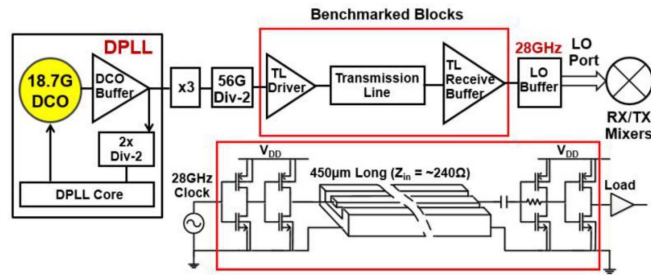


FIGURE 6. Block diagram of the Local-Oscillator chain. Highlighted blocks and contained circuitry are bench marked for 5G (28GHz band).

drive-current requirements LO chains significantly influence the overall power consumption and performance of the system. Therefore, lowering the supply voltage is the most effective technique to reduce the power consumption in such circuits and systems [24], [25].

Fig. 6 shows the block diagram of the studied LO chain. Highlighted block and contained circuitry are bench marked for 5G at 28GHz band. More specifically, performance of transmission line (TL) driver circuits are bench marked using 12nm node SLVT and ELVT Fin FETs. Supply voltage and FOM_{VCO} are evaluated as the points of reference. FOM_{VCO} can be extracted using equation (3) [26]:

$$FOM_{VCO} = \log_{10}(\mathcal{L}_{VCO}(\Delta f)) \times \frac{P}{1mW} \times \left(\frac{\Delta f}{f_0}\right) \quad (3)$$

where \mathcal{L} is the phase noise, Δf is offset frequency, P is dissipated power and f_0 is the centre frequency. In the performed simulations i) the input is a square-wave signal at $f_0 = 28GHz$, ii) TL model is extracted using EMX electromagnetics software [27] for a TL with the length of $450\mu m$ and the same input impedance ($Z_{in} \approx 240\Omega$), for both

TABLE 4. 28GHz TL driver performance summary and comparison.

	SLVT TL Driver	ELVT TL Driver
Supply Voltage [V]	0.575	0.525
Input Impedance [Ω]	238	241
PN at 100k [cBc/Hz]	-113.7	-113.7
PN at 1M [cBc/Hz]	-123.5	-123.5
PN at 10M [cBc/Hz]	-133.2	-133.2
PN at 100M [cBc/Hz]	-142.9	-142.8
Power [mW]	2.3	2.1
FOM_{VCO} [dB]	-228.32	-228.55

TABLE 5. 28GHz TL driver performance summary and comparison.

	SLVT TL Driver	ELVT TL Driver	$\Delta = ELVT - SLVT$
Supply Voltage [V]	0.525	0.525	0
Input Impedance [Ω]	238	241	4
PN at 100k [cBc/Hz]	-129.4	-133.2	-3.8
PN at 1M [cBc/Hz]	-139	-142.8	-3.8
PN at 10M [cBc/Hz]	-147.5	-150.8	-3.8
PN at 100M [cBc/Hz]	-151.7	-154.5	-2.8
Power [mW]	1.7	2.1	0.4
FOM_{VCO} [dB]	-225.76	-228.55	-2.79

ELVT and SLVT based designs and iii) the average dissipation power of all LO chains are compared at the operating frequency of 28GHz. Two scenarios of constant phase noise and constant supply voltage are considered to fairly benchmark the performance of the ELVT based TL driver against its SLVT counterpart.

A. CONSTANT PHASE NOISE

In this experiment the supply voltages for both SLVT/ELVT TL drivers are adjusted so both drivers can operate at the same phase noise level. Results show that the ELVT based driver can operate at ~9% smaller supply voltage while consuming ~8% less power than SLVT based design in order to deliver the same FOM_{VCO} . All the input variables and the TL driver performance metrics are summarized in Table 4. This results confirm the ELVT FinFET can provide the same RF performance at the same phase noise level with lower supply voltage than the SLVT FinFET.

B. CONSTANT SUPPLY VOLTAGE

In this experiment both SLVT and ELVT TL drivers are set to operate with the same supply voltage of 0.525V. Results show that ELVT driver can improve the FOM_{VCO} by ~2.8dB at the offset frequency of 1MHz with 3.8dBc/Hz smaller phase noise. However, to achieve these improvements a trade off with power consumption needs to be made. All the input variables and the TL driver performance metrics are summarized in Table 5. These results confirm that the ELVT FinFET is targeting low-voltage high-performance applications, which require good phase noise in an RF transceiver. FOM_{VCO} versus offset frequency for different supply voltages are plotted on Fig. 7 for more clarification. At the nominal supply voltage of 0.8V for the 12nm technology node both SLVT and ELVT FinFETs deliver the same

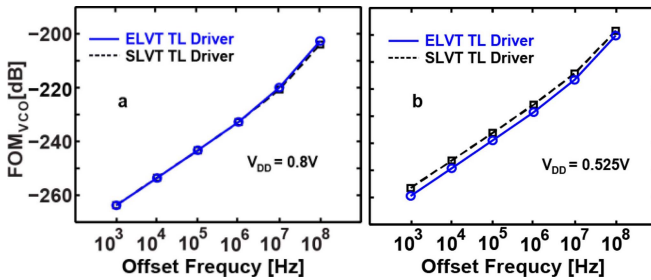


FIGURE 7. FOM_{VCO} versus offset frequency for a) 12nm node FinFET technology nominal supply of 0.8V and b) 0.525V supply voltage.

performance while the ELVT performance advantage is evident at smaller supply voltages.

VI. CONCLUSION

ELVT FinFETs are implemented on 12nm node technology platform modification of channel/halo doping without additional masks, i.e., cost. With V_{TH} reductions of $\sim 90\text{mV}/\sim 70\text{mV}$ for NFET/PFET respectively ELVT FinFETs can deliver $\sim 15\%$ higher IEFF compared to SLVT FinFETs, while DIBL remains in an acceptable range for an RF transistor. Slightly smaller peak F_T (5%) and F_{MAX} (10%) values are compensated with higher numbers at near V_{TH} bias points. Benchmarked LO chain blocks (TL driver) at 28GHz confirm the benefits of ELVT FinFETs. Results show i) $\sim 9\%$ and $\sim 8\%$ reduction in V_{DD} and power consumption respectively at the same PN level as the SLVT based design and ii) $\sim 2.8\text{dB}$ improvement in FOM_{VCO} if operated at $V_{DD} = 0.525\text{V}$ ELVT FinFET with $3.8\text{dBc}/\text{Hz}$ at $f_{OFFSET} = 1\text{MHz}$. These findings confirm that ELVT FinFET can target 5G applications such as networks with many portable receivers which rely on batteries with limited capacity.

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