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AlInGaN/GaN HEMTs With High Johnson's Figure-of-Merit on Low Resistivity Silicon Substrate

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ABSTRACT This work demonstrates high-performance AlInGaN/AlN/GaN high electron mobility transistors grown on 150 mm p-type low resistivity (resistivity∼ 20-100 Ω-cm) silicon substrate with state-of-the-art Johnson's figure-of-merit (JFOM). Current gain cut-off frequency (f_T) of 83 GHz and 63 GHz and power gain cut-off frequency (f_{max}) of 95 GHz and 77 GHz with a three-terminal off-state breakdown voltage of 69 V and 127 V, resulting in a high JFOM of 5.7 THz-V and 8.1 THz-V are achieved on the devices with a gate length of 0.16 μm and gate to drain distance of 2 μm and 4 μm, respectively. The f_T and J-FOM are comparable or better than the reported values obtained on high resistivity silicon and SiC substrates for devices with similar gate length. On the other hand, GaN-on-Si HEMT structure on the LR-Si substrate exhibits lower power gain and power added efficiency due to strong capacitive coupling effects. TCAD large signal output power simulation indicates significant improvements in output power by minimizing the defects and free charge carriers in the GaN buffer even in the presence of the parasitic channel conduction and conductive silicon substrate. We further propose a modified equivalent circuit model of the parasitic conduction to take into account the conductivity of the GaN and AlGaN buffer.

INDEX TERMS AlInGaN, GaN-on-Si, HEMT, JFOM.

I. INTRODUCTION

Over the past decade, III-nitride high electron mobility transistors (HEMTs) have been demonstrating outstanding power and frequency performance, which outperforms their Si and GaAs counterparts in the high power switching application domain. Current gain cut-off frequency (f_T) of 300 GHz and breakdown voltage of over 2,000 V have been demonstrated [1], [2]. Nevertheless, the overall performances of III-nitride HEMTs are still far from their theoretical limits mostly due to the unavailability of a native substrate. The GaN-based HEMTs are typically grown on SiC, sapphire or Si substrate. GaN-on-Si HEMT is recognized as one of the promising technologies for high power and high-frequency applications due to the merits of low cost and large substrate size in comparison with sapphire and SiC substrates. However, challenges, such as higher defect density and relatively 'lossy' silicon substrate at very high-frequency operation, still hinder their wide deployments in the market. High resistivity (HR) ($\geq$ 5 kΩ-cm) silicon substrates are generally used for RF devices to reduce the parasitic loading effects due to the conductive silicon substrate. However, the growth on high resistivity Si substrate is much more difficult than low resistivity substrate because of its lower mechanical strength, which gives rise to large wafer bow and

TABLE 1. Summary of GaN HEMTs on different substrates with their JFOM.

Sub.	Barrier	Lg (μm)	f_T (GHz)	BV (V)	JFOM (THZ-V)	Ref.
HR Si	AlGaN	0.15	63	132	8.3	8
SiC	AlInN	0.08	114	95	10.8	9
SiC	AlInGaN	0.04	230	14	3.2	10
SiC	AlInGaN	0.066	220	20	4.4	11
LR Si	AlGaN	0.3	28	60	1.7	4
LR Si	AlGaN	0.3	55	N/A	N/A	5
LR Si	AlInGaN	0.16	83	69	5.7	This work
LR SI	AlInGaN	0.16	63	127	8.1	This work

easy wafer breakage, resulting in low production yield. This issue becomes even severe with increasing substrate size. In addition, the RF substrate loss is a function of both the operating frequency and temperature. Chandrasekar et al. recently quantitatively showed that the HR-Si substrate exhibits noticeable temperature dependence above 150 °C. Whereas, LR-Si substrate remains insensitive to temperature even at 200 °C. Furthermore, GaN-on-LR-silicon exhibits similar substrate loss as HR-Si for frequency < 12 GHz and therefore, could be a promising substrate for high power and high-frequency wireless communication applications in the S and X bands [3]. The realization of RF-GaN HEMTs on the LR-Si substrate has been already reported by several groups [4], [5]. For example, Eblabla *et al.* obtained f_T of 55 GHz and f_{max} as high as 121 GHz in a 0.3 μm gate AlGaN/GaN HEMTs on LR-Si substrate. However, in most cases, the resultant Johnson's figure-of-merit (JFOM) is either very low or not even reported. The performances of transistors of different technologies are generally evaluated by their respective figure-of-merits. The Johnson's figure-of-merit is one of them [6]. JFOM evaluates the merits of a transistor to be used in high power and high-frequency applications. Therefore, JFOM is an extremely important parameter of a transistor for real-life applications. Table 1 presents a summary of some of the best reported GaN HEMTs with their JFOM on different substrates. As can be seen, AlGaN/GaN HEMTs exhibiting a JFOM over 8 THz-V, have been obtained on HR-Si [7], [8]. Whereas, JFOM over 10 THz-V is also achieved on AlInN/GaN HEMTs [9]. Although AlInGaN/GaN HEMTs are reported to have very high f_T of over 200 GHz and f_{max} of 400 GHz, only a few reports are showing high JFOMs [10], [11]. Table 1 further indicates that GaN-on-HR-Si HEMTs have started to show comparable high- frequency performance with those on SiC substrate due to the significant improvements in the GaN-on-Si epitaxy. Nevertheless, similar performance is yet to be achieved on cost-effective large size LR-Si substrates.

In this work, we report RF device performance of AlInGaN/GaN HEMT with a high JFOM of over 8 THz-V on LR-Si, which is comparable to those of GaN HEMTs grown on HR-Si and SiC substrates and therefore, it may pave the way for cost effective GaN-on-Si HEMTs for RF applications.

II. MATERIAL AND DEVICES

A. MATERIAL GROWTH

The AlInGaN/AlN/GaN heterostructure studied in this work was grown on a 150 mm p-type boron-doped LR silicon (111) substrate by metal-organic chemical vapor deposition in an Aixtron closed couple showerhead (CCS) reactor. The resistivity of the silicon substrate was in the range of 20-100 Ω-cm. The growth was started with approximately 250 nm AlN nucleation layer followed by a 1 μm step graded AlGaN buffer layer with Al composition of 80%, 50% and 20%. A 1.8 μm GaN buffer layer was then grown, followed by a 100 nm GaN channel layer. There was also a 100 nm GaN transition layer in between the buffer and the channel for carrier gas switching. Finally, a 1 nm AlN spacer layer, 8.5 nm AlInGaN barrier layer, and a 2 nm GaN cap layer were grown successively. The composition of the AlInGaN barrier layer was determined to be 73% of Al, 8% of In, and 19% of Ga by x-ray photoelectron spectroscopy (XPS) and further confirmed by energy-dispersive x-ray spectroscopy (EDX) and cross-section high-resolution transmission electron microscopy (HRTEM), conducted earlier on the calibration samples.

Usually, in case of unintentionally C-doped GaN heterostructure, the buffer and the channel are grown with the same Ga precursor, i.e., trimethylgallium (TMG), at almost the same growth temperature of 1040 C. In that case, the carbon incorporation level would be the same in the buffer and channel. Different carrier gases and a higher V/III ratio can be used for the growth of GaN channel and buffer layers to lower the C incorporation in the channel. However, in a device quality GaN heterostructure, the growth conditions of the buffer and channel layers can not be varied significantly for lowering C incorporation, as this would otherwise affect the surface morphology, interface roughness, growth time, and the overall quality. We have therefore used a different strategy, where the thick GaN buffer layer was grown with conventional TMG precursor in H_2 ambient. Whereas, triethylgallium (TEG) was used to grow the 100 nm GaN channel layer in N_2 ambient. A 100 nm GaN transition layer was grown with TMG in N_2 ambient in between the buffer and channel layers. The carbon concentration as measured by secondary ion mass spectroscopy in the GaN buffer, the transition layer and the channel are $4x10^{17}$ cm^{-3}, $2x10^{17}$ cm^{-3} and $6x10^{16}$ cm^{-3}, respectively. It means more than 85% reduction in residual carbon is achieved in the GaN channel, without affecting the surface morphology, interface roughness, and the overall quality of the GaN layer. Hall-effect measurements with van der Pauw configuration show high electron mobility of 1,920 cm^2/V.s with a two-dimensional electron gas (2DEG) density of $1.2x10^{13}$ cm^{-2}, resulting in sheet resistance of only 270 Ω/□.

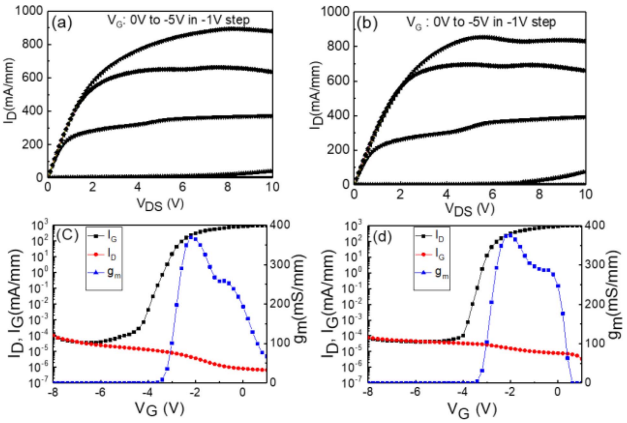

FIGURE 1. DC I_D-V_{DS} characteristics of device (a) A and (b) B. I_D-V_G and transconductance characteristics of device (c) A and (d) B.

B. DEVICE FABRICATION

The device fabrication was started with Ar+ implantation for mesa isolation. Ti/Al/Ni/Au (25/125/45/55 nm) metal stack for source/drain ohmic contacts were deposited using an electron beam for Ti, Al and Ni and thermal evaporation for Au, followed by rapid thermal annealing (RTA) at 875 °C for 40 sec in N_2 ambient. A tri-layer photoresist of ZEP/LOR/ZEP was used to define the T-gate by e-beam lithography, followed by metal deposition of Ni/Au (30/300 nm) as Schottky gate contact. A 200 nm of SiNx layer was deposited by using plasma-enhanced chemical vapor deposition. Finally, a metal stack of Ni/Au was deposited on contact via as pad metal for RF measurements. The devices feature a 0.16 um gate with gate-source and gate-drain spacing of 1 μm and 2/4 μm, respectively. The devices with gate to drain distance of 2 μm and 4 μm will be henceforth referred to as device A and device B, respectively.

III. RESULTS AND DISCUSSION

A. DC CHARACTERISTICS

Fig. 1 shows the DC output characteristics of devices A and B. Both of the devices exhibit similar DC output characteristics except the three-terminal off-state breakdown voltage as expected. A drain current (I_{DSS}) of 893 mA/mm and 854 mA/mm, peak extrinsic transconductance (g_m) of 370 mS/mm and 375 mS/mm, and R_{on} of 0.175 mΩ-cm^2 and 0.259 mΩ-cm^2 are measured on device A and B, respectively. Both of the devices show a threshold voltage of -2.8 V and well behaved pinch-off characteristics. The off-state gate leakage current at V_{GS}= 8 V and V_{DS}= 5 V is on the order of 10^{-4} mA/mm, resulting in an I_{on}/I_{off} ratio of 10^7. The I_{on}/I_{off} ratio of 10^7 is comparable to those of GaN HEMTs grown on HR-Si or SiC substrates [12], [13].

Achieving a high breakdown voltage is crucial to obtain high JFOM. The three-terminal off-state breakdown characteristics of device A and B are shown in Fig. 2. We define breakdown when the off-state drain leakage current reaches 1mA/mm. As can be seen from Fig. 2, device A and B exhibit

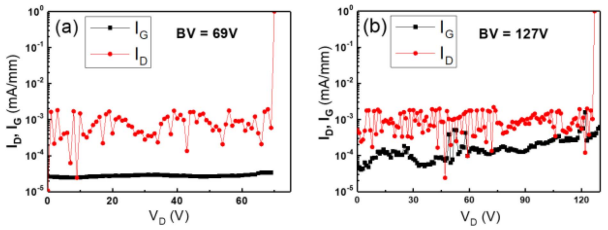

FIGURE 2. Three terminal off-state breakdown characteristics of the device (a) A and (b) B, respectively, at $V_{GS} = -10$ V.

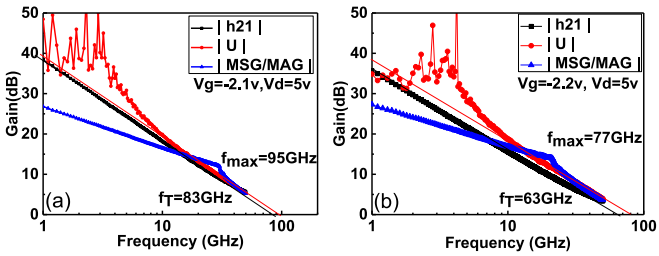

FIGURE 3. RF characteristics of device (a) A and (b) B, respectively.

off-state breakdown at 69 V and 129 V with 2 μm and 4 μm gate to drain distance, respectively. The gate leakage current of devices A and B are still low even at 100 V and 140 V, respectively. This implies that the observed breakdown is not due to gate leakage, but the source induced breakdown [14]. Further improvement in breakdown voltage can be obtained by suppressing the buffer leakage current [15].

B. RF CHARACTERISTICS

On-wafer s-parameter measurements from 0.1 GHz to 50 GHz were performed on devices A and B. Standard short-open-load-through calibration processes were carried out before the measurements. Open and short patterns on the wafers were used to de-embed the parasitic effects, such as pad capacitance and inductance. The deduced current gain (h_{21}), Mason's unilateral gain (U), and maximum stable gain (MSG)/maximum available gain (MAG) of devices A and B are shown in Fig. 3. (a) and (b), respectively. The current gain cut-off frequency (f_T) and power gain cut-off frequency (f_{max}) were extracted by extrapolating h_{21} and U with −20dB/decade roll-off. The maximum current gain (h_{21}) and MSG/MAG were obtained at $V_{GS} = -2.1$ V and −2.2 V and $V_{DS} = 5$ V for devices A and B, respectively, i.e., around the bias for maximum extrinsic transconductance. The current gain cut-off frequency of 83 GHz and 63 GHz and power gain cut-off frequency of 95 GHz and 77 GHz with a high J-FOM of 5.7 THz-V and 8.1 THz-V are achieved on device A and B, respectively.

The extracted small-signal parameters from cold FET and hot FET models are summarized in Table 2.

As all the parameters related to C_{gs} in devices A and B are assumed to be identical, the gate-source capacitance of both the devices should be the same. However, the extracted C_{gs} of device B is slightly higher than that of device A. This

TABLE 2. Small signal parameters of Device A and B.

Extrinsic parameters Device A/B	C_{pgs} (fF/mm)	27.5/8	R_s (Ω.mm)	0.5/0.58
	C_{pds} (fF/mm)	223/225	R_g (Ω.mm)	1.44/1.74
	R_d (Ω.mm)	0.92/1.44		
Intrinsic parameters Device A/B	Intrinsic g_m ($g_{m,i}$)(mS/mm)	403/354	C_{ds} (fF/mm)	643/213
	C_{gs} (fF/mm)	688/831	R_i (Ω.mm)	1.78/2.06
	C_{gd} (fF/mm)	198/117	$1/g_o$ (Ω.mm)	29.8/82.4

could be attributed to slightly different L_g (gate length) and Lgs (gate to source distance) in device A and B because of process variation.

It is worth to note that f_{max} usually increases with gate-to-drain distance (Lgd) as C_{gd} should decrease with increasing L_{gd}. On deceive A and B, small-signal C_{gd} indeed decreases from 198 fF/mm to 117 fF/mm when the L_{gd} increases from 2 μm the 4 μm. However, device B, which has 4 μm L_{gd}, exhibits a lower f_{max} than device A in this study. The lower than expected f_{max} on device B could be attributed mainly to its 24% lower f_T than device A (because of lower intrinsic g_m and higher C_{gs}) and partly due to a slight increase in R_i and R_g.

C. EFFECTS OF RESIDUAL CARBON ON F_T

One of the features of our devices in this study is the TEG grown GaN channel in N_2 ambient, which shows more than 85 % reduction in residual carbon concentration in the GaN channel than the GaN buffer. Substitutional C (C_N) at N-site with an energy level of 0.9 eV above the valence band maxima has been identified as one of the common sources of both DC and RF performance degradation in GaN HEMTs [16]. Therefore, an improvement in dynamic behavior and RF performance is expected due to the reduction in the acceptor-like C_N in the vicinity of the heterointerface and the channel, as indicated by several reports [17]. Unfortunately, the background carbon cannot be removed completely, as the organometallic precursors are the source of this C impurity in MOCVD grown GaN. Therefore, having an idea of the lower and upper limits of C concentration in the GaN channel may be helpful in perfecting GaN HEMTs. Keeping the above viewpoint in mind, we have further simulated the effects of

residual C concentration on the current gain cut-off frequency and obtained a quantitative value of the upper and lower limits of C impurity in the channel. Silvaco Atlas 2D device simulator is used to simulate the effects of the acceptor-like C-traps on f_T.

Fig. 4 shows f_T as a function of trap density (N_{trap}) in the GaN channel. As can be seen, f_T decreases with increasing trap density in the channel region. The reduction in current gain is substantial when the trap density exceeds $1x10^{17}$ cm^{-3}. Whereas, there is an insignificant improvement in f_T for N_{trap} below $1x10^{16}$ cm^{-3}. This observed dependency of f_T on the defect density in Fig. 4 can be explained by parasitic charge modulation as proposed by Nguyen *et al.* [18]

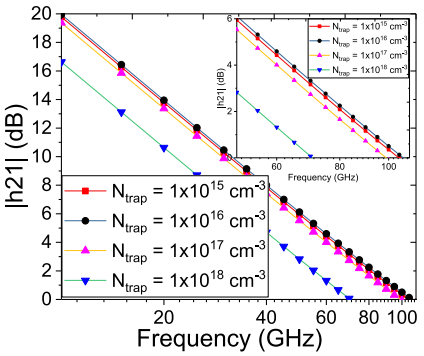

FIGURE 4. TCAD simulation showing dependency of current gain cut-off frequency on the trap density in GaN channel. The inset shows a magnified portion of fig. 4 for better visuals.

and Foisy *et al.* [19]. The current gain cut-off frequency can be expressed as follows, $f_T = g_m/2\pi C_G$, where, $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ and $I_{DS} = V_{sat}.Q_T$, V_{sat} is electron saturation velocity and Q_T is the total charge in the channel. The input signal at the gate modulates the 2DEG in the channel and thus the drain current. However, in a real HEMT, the total charge Q_T consists of the charge by the channel electrons (Q_n) and parasitic charges, such as those in the interface states and traps/defects ($Q_{parasitic}$). These parasitic charges respond to high-frequency input signal but they do not contribute to the drain current. Therefore, only a fraction of the total charge contributes to the drain current. This prompts the modulation efficiencyγ, which is defined as $\frac{\partial Q_n}{\partial Q_T}$ and $I_{DS} = V_{sat}.Q_n$. Therefore, $g_m = V_{sat}\frac{\partial Q_n}{\partial V_{GS}}$ and $f_T = \frac{V_{sat}}{2\pi C_G}\left(\frac{\partial Q_T}{\partial V_{GS}}\right)\gamma$. The modulation efficiency represents the ability to produce an incremental change in drain current by a small change in the gate voltage. As the trap density in the channel increases due to the increase in C concentration, the ratio of Q_n/Q_T decreases. Hence, the modulation efficiency also decreases. As a result, f_T decreases with the increase in trap density Apart from g_m, the device simulation also indicates (not shown here) a gradual increase of C_G as N_{trap} increases and could be detrimental at high C doping concentration in the channel. Around 5% increase of C_G is observed when N_{trap} increases from $1x10^{16}$ cm^{-3} to $1x10^{18}$ $cm^{-}3$. Therefore, as indicated by the 2D device simulation, the trap density in the channel should be in the lower order of $10^{16}/cm^3$ or below to avoid the effect of parasitic charge modulation on current gain cut-off frequency.

IV. LARGE SIGNAL RF POWER PERFORMANCE

A. LARGE SIGNAL POWER PERFORMANCE

The large-signal RF continuous wave power measurements of the AlInGaN/GaN on LR-Si and HR-Si are shown in Fig. 5 (a) for direct comparison. As shown in the figure, AlInGaN/GaN HEMT on LR-Si exhibits operating power gain of 14.07 dB, power added efficiency (PAE) of 14.22% and a saturated output power of 22.41 dBm at 10 GHz, resulting in an output power density of 1.38 W/mm. Whereas,

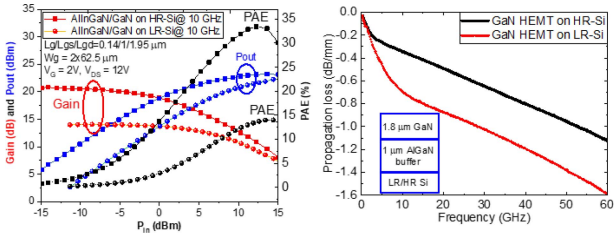

FIGURE 5. ***(a) RF power performance of AlInGaN/GaN HEMT grown on LR Si substrate (b)*** **Transmission loss of CPW lines of GaN heterostructures on LR (<100 Ω-cm) and HR (>5000 Ω-cm) silicon substrate.**

AlInGaN/GaN HEMT on HR-Si with identical epilayers exhibits operating power gain of 20.74 dB, power added efficiency (PAE) of 33.46% and a saturated output power of 23.22 dBm at 10 GHz, resulting in an output power density of 1.73 W/mm.

The maximum power density obtained in this work is lower than the best reported GaN-on-HR-Si HEMTs. This may be due to the unoptimized device design for large signal power performances. For instance, Dumka et al. obtained over 65% PAE in a 0.25 μm T-gate GaN on HR-Si HEMTs, having a field plate in the high field source-drain region [20]. Jardel *et al.* reported Pout of 6.6 W/mm with PAE of 51% at 10 GHz in a multi-finger 8 x 0.75 μm GaN on Si HEMTs [21]. Nonetheless, our intension of this part is to compare RF power performances of GaN HEMT grown on LR and HR silicon substrates on the same scale. It is shown that HEMTs with same epistructure on LR-Si do not exhibit comparable large signal performance with those on HR-Si, even with excellent DC and small signal performances. However, the result shown in Fig. 5. (a) may help to identify the performance limiting factors and thereby finding a solution to overcome those limitations.

B. PARASITIC LOADING EFFECTS

The degraded large signal performance of the GaN-HEMT on the LR-Si substrate is further verified by continuous wave large-signal RF power measurement. As discussed in the introduction, the capacitive coupling due to lossy silicon substrate could be serious at the high operating frequency. Fig. 5. (b) shows transmission losses extracted from coplanar waveguide (CPW) transmission lines, fabricated on representative samples with the same epitaxial GaN buffer layers, both on LR and HR silicon substrates for comparison. As can be seen, the GaN-on-LR-Si exhibits higher transmission loss as compared to its HR-Si counterpart. This is opposite to a recent study by Chandrasekar *et al.* where they have predicted that the LR-Si substrate may even have lower substrate loss for frequency up to 12 GHz [3]. As indicated in the figure, a distinct increase in transmission loss is evident for the measured operating frequency up to 60 GHz. GaN-on-HR-Si and GaN-on-LR-Si exhibit a transmission loss of 0.35 dB/mm and 0.69 dB/mm at 10 GHz, respectively. The loss increases up to 0.8 dB/mm at 40 GHz for the GaN-on-HR-Si sample, whereas it is as high as 1.19 dB/mm in the case of GaN-on-LR-Si.

Moreover, as shown in Fig. 5. (a), the power gain and PAE of the GaN HEMT-on LR-Si are 32% and 57% lower than that of GaN HEMT-on-HR-Si, respectively. This is consistent with the model proposed by Xiao *et al.* [22]. They have proposed a series RC network between the source and the drain, representing the parasitic loading effects due to the conductive substrate resistance (Rsub) and capacitance (Csub) at mm-wave frequency. They have explicitly shown that parasitic loading effects at 12 GHz may degrade power gain up to 27% and PAE as high as 48% along with the output power.

It is worth to note that parasitic conduction is present in GaN HEMT grown on both HR-Si and LR-Si. However, the effect is more severe in LR-Si as the high conductivity of the substrate is added on top of the defects already present in the epilayers.

C. PHYSICAL ORIGIN

The physical origin of this parasitic conduction is still under debate [23]. For instance, several authors have reported Ga/Al diffusion into the silicon substrate in the order of 10^{16} cm^{-3} to 10^{18} cm^{-3} with up to 3 μm roll-off into the silicon substrate [24]. The Ga/Al atoms into the Si substrate act as acceptors and form a p-type conductive layer at the top surface of the substrate. On the other hand, silicon in non-polar material whereas, AlN is highly polar. This difference in polarization charge generates a high density of electron inversion channel at the AlN/Si interface as high as 10^{13} cm^{-2} [25]. Furthermore, the highly defective AlN nucleation layer is also identified as the source of parasitic channel conduction in GaN-on-Si devices [26].

D. POSSIBLE SOLUTIONS

It is clear at this point that GaN-HEMTs grown on LR-Si can achieve comparable DC and small signal performances as the GaN HEMTs grown on HR-Si. However, the same is not true in the case of large signal performance due to the formation of parasitic channel at the buffer/Si interface. In order to avail all the benefits of LR-Si as discussed in the introduction section, one possible solution could be to use standard back-side processing technique where, the silicon substrate is selectively removed from the region beneath the active channel [27]. This will effectively eliminate the electron inversion channel at the AlN/Si interface as well as the conductive p-type region due to the diffusion of Ga/Al into the Si-substrate. However, the leaky AlN nucleation layers will be still there as a source of parasitic channel and may degrade the power performance to some extent. We have further performed 2D TCAD device simulations to investigate the effects of the parasitic channel on the large signal output power. In order to mimic the parasitic loading effects, an electron inversion layer at the AlN/Si interface, acceptor-like trap of 2x10^{16} cm^{-3} in the silicon substrate distributed uniformly up to 2 μm from the AlN/Si

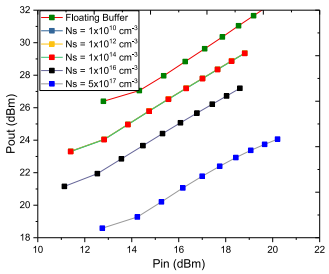

FIGURE 6. **2D device simulation of large-signal output power of a typical GaN HEMT grown on LR-Si including parasitic loading effects. Pout for Ns = $1x10^{14}$ cm^{-3}, $1x10^{12}$ cm^{-3}, and $1x10^{10}$ cm^{-3} overlap on each other as there is no noticeable change in Pout thereafter.**

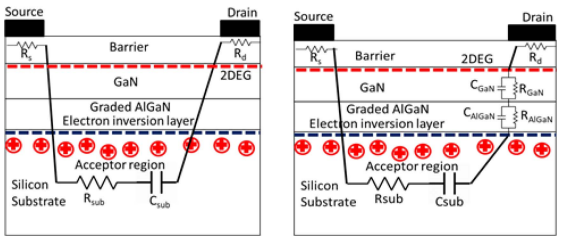

FIGURE 7. **Small signal equivalent circuit model of parasitic loading effects without (left) and with (right) taking into account the defects and free charge carriers in the GaN and AlGaN buffer.**

interface, and donor-like trap concentration of $1x10^{10}$ to $1x10^{17}cm^{-3}$ in the GaN and AlGaN buffer were considered in the simulation. The substrate resistivity was set to 1 Ω-cm. As can be seen in Fig. 6, the large signal simulated Pout at 10 GHz significantly varies with the conductivity of the GaN buffer, while all other parameters are the same. For instance, Pout increases from 20 dBm to 26 dBm at an input power of 15 dBm when the free carrier concentration in the GaN buffer decreases from $5x10^{17}$ cm^{-3} to 10^{14} cm^{-3}. However, there is no noticeable change in Pout thereafter. Further increase in Pout can be seen when there is no free carrier in the buffer (denoted as floating buffer). Therefore, the effects of substrate resistivity and the parasitic channel can significantly be minimized just by controlling the resistivity and the quality of the GaN buffer.

Fig. 7 (left) schematically represents the formation of this parasitic channel along with an equivalent circuit model. As proposed by Xiao et al., the R_{sub} and C_{sub} in series between the source and drain (along with source and drain series resistances) takes into account the parasitic loading effects [22]. All other components of the equivalent circuit are not shown in the figure for simplicity. A complete equivalent circuit model of a typical GaN transistor can be found elsewhere [22]. As shown in Fig. 6, the 2D simulation suggests that a defect-free (and hence insignificant number of free carriers) GaN buffer acts as a floating layer isolating the active channel from the most defective AlN/Si interface and highly conductive silicon substrate. Therefore, we propose a modified equivalent circuit model of the parasitic loading effects, where the parasitic channel conduction includes the defects and free carriers in the GaN and AlGaN buffers as shown in Fig. 7 (right). The additional capacitance (C_{GaN}, C_{AlGaN}) and the resistance (R_{GaN}, R_{AlGaN}) in Fig. 7 (right) represent the bound charges due to the defect charges and free mobile charges in the respective epitaxial layers. We argue that the parasitic conduction channel formed at the very bottom of the epitaxial layers affects the large signal performance at high drain voltage due to the finite conductivity of the top AlGaN and GaN layers as well as through sidewall conduction to some extent.

V. CONCLUSION

AlInGaN/AlN/GaN HEMTs on a low resistivity silicon substrate have been demonstrated with comparable small-signal performance as those grown on HR-Si and SiC substrates. f_T of 83 GHz and 63 GHz and f_{max} of 95 GHz and 77 GHz with a three-terminal off-state breakdown voltage of 69 V and 127 V are achieved on the devices with a gate length of 0.16 μm and gate to drain distance of 2 μm and 4 μm, respectively. The combination of f_T and breakdown voltage results in a record JFOM of 8.1 THz-V. In-depth analysis suggests that superior electron-transport property and lower residual carbon impurity in the GaN channel are the keys to achieve state-of-the-art device performance on GaN-on-Si HEMTs. However, GaN-on-Si HEMTs on the LR-Si substrate exhibit higher transmission loss due to strong capacitive coupling effects making it difficult to obtain comparative large-signal power performance as those on the HR-Si substrate. 2D device simulation indicates significant improvements in large signal output power by minimizing the defects and free charge carriers in the GaN buffer even in the presence of the parasitic channel conduction and conductive silicon substrate. A modified small signal equivalent circuit model of the parasitic conduction taking into account the conductivity of both the GaN and AlGaN buffer is also proposed. It is concluded that a different epitaxial layer design should be adopted to minimize the large-signal power loss of GaN HEMTs on LR-Si substrate. Nonetheless, this report of GaN-on-LR Si HEMTs with record JFOM of 8.1 THz-V shows a promising low-cost alternative for S and X band applications.

REFERENCES

[1] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT with 300-GHz fmax," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 195–197, Mar. 2010.

[2] O. S. Koksaldi *et al.*, "N-polar GaN HEMTs exhibiting record breakdown voltage over 2000 V and low dynamic on-resistance," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1014–1017, Jul. 2018.

[3] H. Chandrasekar *et al.*, "Quantifying temperature-dependent substrate loss in GaN-on-Si RF technology," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1681–1687, Apr. 2019.

[4] S. Arulkumaran *et al.*, "Direct current and microwave characteristics of sub-micron AlGaN/GaN high-electron-mobility transistors on 8-inch Si (111) substrate," *Jpn J. Appl. Phys.*, vol. 51, Oct. 2012, Art. no. 111001.

[5] A. Eblabla, X. Li, I. Thayne, D. J. Wallis, I. Guiney, and K. Elgaid, "High performance GaN high electron mobility transistors on low resistivity silicon for X-band applications," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 899–901, Sep. 2015.

[6] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989.
[7] H. S. Yoon *et al.*, "Microwave low-noise performance of 0.17 μm gate-length AlGaN/GaN HEMTs on SiC with wide head double-deck T-shaped gate," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1407–1410, Nov. 2016.
[8] K. Ranjan, S. Arulkumaran, G. I. Ng, and S. Vicknesh, "High Johnson's figure of merit (8.32 THz· V) in 0.15-μm conventional T-gate AlGaN/GaN HEMTs on silicon," *Appl. Phys. Exp.*, vol. 7, no. 4, 2014, Art. no. 044102.
[9] M. L. Schuette *et al.*, "Gate-recessed integrated E/D GaN HEMT technology with f T/fmax> 300 GHz," *IEEE Electron Device Lett.*, vol. 34, no. 6, pp. 741–743, Jun. 2013.
[10] R. Wang *et al.*, "Quaternary barrier InAlGaN HEMTs with fT/fmax of 230/300 GHz," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 378–380, Mar. 2013.
[11] R. Wang *et al.*, "220-GHz quaternary barrier InAlGaN/AlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1215–1217, Sep. 2011.
[12] S. Huang *et al.*, "High-f-MAX high Johnson's figure-of-merit 0.2-μm gate AlGaN/GaN HEMTs on silicon substrate with AlN/SiNx passivation," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 315–317, Mar. 2014.
[13] Y.-K. Lin *et al.*, "High-performance GAN moshemts fabricated with ALD AL 2 O 3 dielectric and NBE gate recess technology for high frequency power applications," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 771–774, Jun. 2017.
[14] C.-W. Tsou, C.-Y. Lin, Y.-W. Lian, and S. S. Hsu, "101-GHz InAlN/GaN HEMTs on silicon with high Johnson's figure-of-merit," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2675–2678, Aug. 2015.
[15] S. L. Zhao *et al.*, "Analysis of the breakdown characterization method in GaN-Based HEMTs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1517–1527, Feb. 2016.
[16] M. Singh, M. J. Uren, T. Martin, S. Karboyan, H. Chandrasekar, and M. Kuball, "'Kink' in AlGaN/GaN-HEMTs: Floating buffer model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3746–3753, Sep. 2018.
[17] J. Bergsten *et al.*, "Electron trapping in extended defects in microwave AlGaN/GaN HEMTs with carbon-doped buffers," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2446–2453, Jun. 2018.
[18] L. D. Nguyen, L. E. Larson, and U. K. Mishra, "Ultra-high speed modulation-doped field-effect transistors: A tutorial review," *Proc. IEEE*, vol. 80, no. 4, pp. 494–518, Apr. 1992.
[19] M. C. Foisy, P. J. Tasker, B. Hughes, and L. F. Eastman, "The role of inefficient charge modulations in limiting the current-gain cutoff frequency of the MODFET," *IEEE Trans. Electron Devices*, vol. ED-35, no. 7, pp. 871–878, Jul. 1988.
[20] D. C. Dumka and P. Saunier, "GaN on Si HEMT with 65% power added efficiency at 10 GHz," *Electron. Lett.*, vol. 46, no. 13, pp. 946–947, Jun. 2010.
[21] O. Jardel *et al.*, "Electrical performances of AlInN/GaN HEMTs. A comparison with AlGaN/GaN HEMTs with similar technological process," *Int. J. Microw. Wireless Technol.*, vol. 3, pp. 301–309, Apr. 2011.
[22] D. Xiao *et al.*, "Detailed analysis of parasitic loading effects on power performance of GaN-on-silicon HEMTs," *Solid-State Electron.*, vol. 53, no. 2, pp. 185–189, Feb. 2009.
[23] H. Chandrasekar, "Substrate effects in GaN-on-silicon RF device technology," *Int. J. High Speed Electron. Syst.*, vol. 28, no. 1, 2019, Art. no. 1940001.
[24] L. Wei *et al.*, "Al diffusion at AlN/Si interface and its suppression through substrate nitridation," *Appl. Phys. Lett.*, vol. 116, no. 23, 2020, Art. no. 232105.
[25] T. T. Luong *et al.*, "RF loss mechanisms in GaN-based high-electron-mobility-transistor on silicon: Role of an inversion channel at the AlN/Si interface," *Physica Status Solidi (A)*, vol. 214, no. 7, 2017, Art. no. 1600944.
[26] F. Berber, D. W. Johnson, K. M. Sundqvist, E. L. Piner, G. H. Huff, and H. R. Harris, "RF dielectric loss due to MOCVD aluminum nitride on high resistivity silicon," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1465–1470, May 2017.
[27] L. Pattison, T. Boles, N. Tuffy, and G. Lopes, "Improving GaN on Si power amplifiers through reduction of parasitic conduction layer," in *Proc. 9th Eur. Microw. Integr. Circuit Conf.*, 2014, pp. 92–95.