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Enhance the ESD Ability of UHV 300-V Circular LDMOS Components by Embedded SCRs and the Robustness P-Body Well

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ABSTRACT The ultra-high voltage (UHV) Lateral-diffused MOSFET (LDMOS) transistor has been widely used in power circuit applications and also used as an electrostatic discharge (ESD) self-protection device. However, the ESD ability of an UHV LDMOS is generally worse than that of low- and high-voltage (HV) devices, which means this UHV LDMOS device can be easily failed under an ESD event. Then, the method of embedded a silicon-controlled rectifier (SCR) into the HV LDMOS has been used in the HV circuit as an ESD protection technique. But when this architecture is applied to UHV devices, will its ESD capability be as good as in HV devices? A novel SCR with a P-body well architecture is proposed, which can effectively enhance the ESD ability of the UHV nLDMOS device when the drain side is embedded this new structure. The proposed structure can greatly improve the ESD capability of the device without adding any extra process step (& photomask), layout area and affecting the basic breakdown voltage. Finally, the proposed structure of the PPP-arranged type with the P-body well can greatly increase the ESD (FOM) ability which I_{t2} and HBM ability can be increased by 68.7% and 22.2% (72.9%), respectively, as compared with the conventional SCR PPP-arranged type.

INDEX TERMS Electrostatic discharges (ESD), human body model (HBM), power MOSFET, silicon controlled rectifier (SCR), transmission line pulse system, ultra-high voltage (UHV).

I. INTRODUCTION

In recent years, the progress of an ultra-high voltage (UHV) process technology has developed vigorously, UHV LDMOS power devices have scaled from discrete components to integrated circuits and has been widely used in power electronics, switching-mode power supply (SMPS), and power management circuits [1]–[3]. However, the ESD damage has been seriously impacted when UHV LDMOS components (supply voltage higher than 100V) integrated into smart power integrated circuits (PICs). When the ESD event occurred in an UHV device, because the power dissipation of an UHV device is greater than that of low-voltage (LV) and high-voltage (HV) devices, the heat generated by the excessive power of the UHV device is difficult to dissipate, which may easily cause this UHV device to failure, thereby reducing the reliability of the circuit. Therefore, an SCR device with the low impedance and low holding voltage (clamp voltage) has been proposed to reduce the power dissipation and improved the ESD ability. The embedded SCR technique has been widely used in the LV (supply voltage lower than 5V) and HV (supply voltage higher than 5V but lower than 100V) integrated circuits due to its superior ESD ability [4]–[8]. Because the layout area of an HV device is much larger than that of an LV device, some literatures have embedded the SCR into the drain side of an HV LDMOS, which not only fixes the layout area, but also improves the ESD capability [9]–[14]. Moreover, a literature showed that the area of an UHV device is much larger than that of LV and HV devices, and the ESD capability is more fragile and still need improvement [15].

The conventional architecture is to form a parasitic SCR in the nLDMOS by embedded a P^+ heavily doped layer in

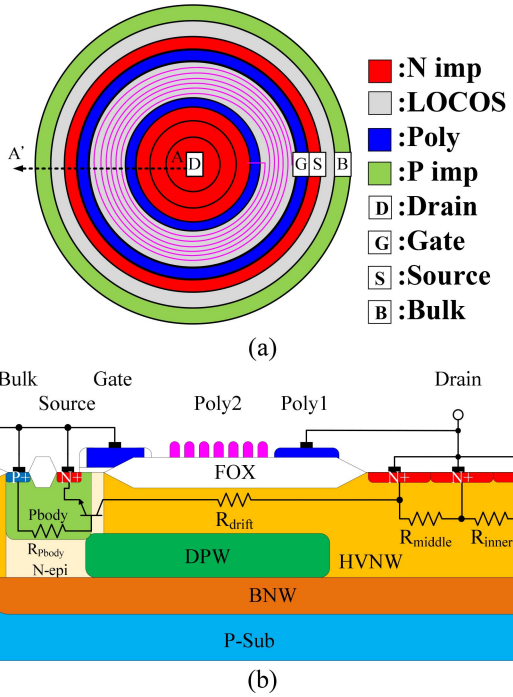


FIGURE 1. **(a) Layout diagram and (b) cross-sectional view of the circular nLDMOS Reference DUT.**

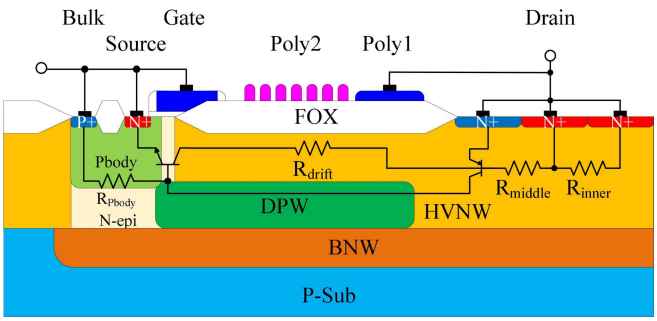


FIGURE 2. **Cross sectional view of the conventional architecture of an nLDMOS with the drain side embedded SCR (example for the NNP-arranged type).**

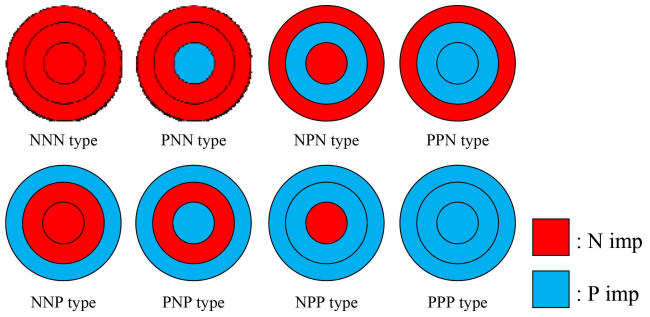


FIGURE 3. **Eight kinds of drain side magnifying layout diagrams of an nLDMOS with embedded SCR.**

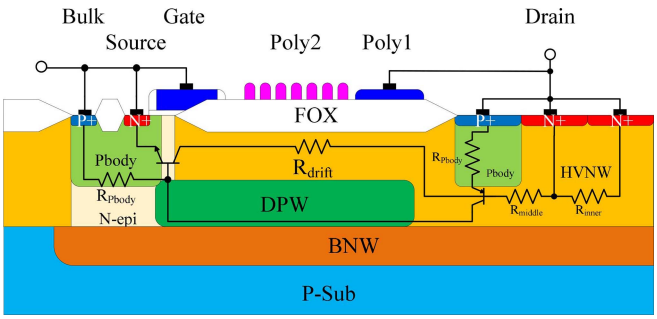


FIGURE 4. **Cross sectional view of the novel architecture of an nLDMOS with the drain side embedded SCR and the P-body layer (example for the NNP-arranged type with the embedded P-body well).**

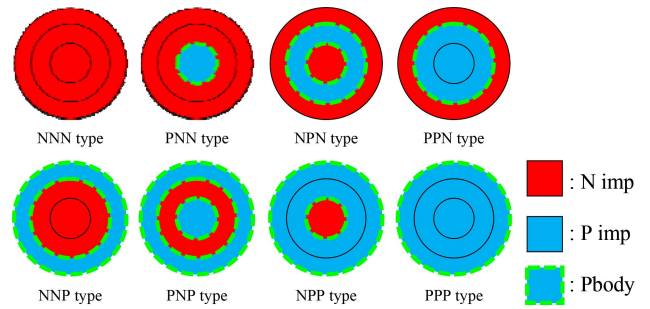


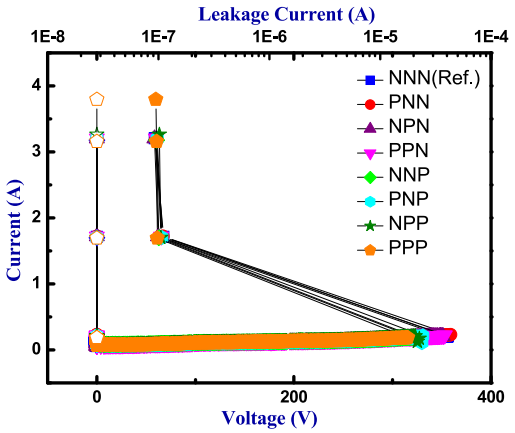
FIGURE 5. **Eight kinds of drain side magnifying layout diagrams of an nLDMOS with embedded SCR and the P-body well.**

the drain side. Therefore, a literature showed that the HBM capability improvement of an UHV JFET device [16], but can the application of this architecture to improve the poor ESD capability of the UHV nLDMOS device? Or is there a more novel architecture? In this article, an effective method to enhance the ESD per unit area ability has been proposed and investigated. By embedded a low-doped P-body layer under the anode P^+ heavy-doped layer of the parasitic SCR compared with the traditional parasitic SCR application of the UHV device have discussed. In order to judge the traditional and novel SCR architecture, the figure of merit (FOM) is used to judge the ESD and Latchup (LU) capabilities of the unit area of the devices under test (DUTs). By calculating the product of the holding voltage and the secondary breakdown current divided by the cell area of the DUT, the overall ESD/LU capability of the unit area of the DUTs can be investigated. Finally, the breakdown voltage, trigger voltage, holding voltage, secondary breakdown current and human-body model (HBM) capability had been measured by a semiconductor parameter analyzer, a 100-ns transmission-line pulsing (TLP) and human-body model (HBM) testing systems to evaluate the ESD ability after embedded the SCR and P-body layer in the UHV nLDMOS related devices.

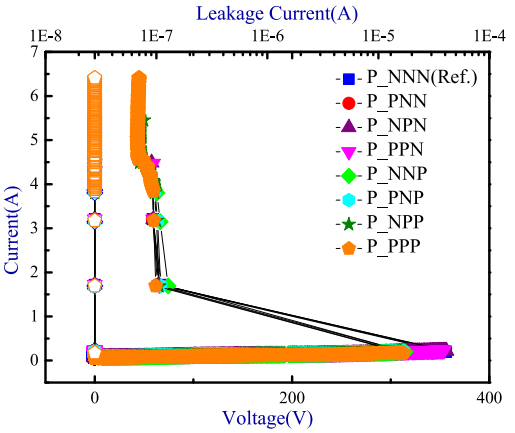
II. DEVICE STRUCTURES AND LAYOUT

A. REFERENCE DEVICE OF THE UHV CIRCULAR NLDMOS

Layout diagram and cross-sectional view (along the line A-A' of Fig. 1(a)) of an UHV nLDMOS reference DUT (Ref. DUT) are shown in Fig. 1. The traditional LV and HV LDMOS layout type use a rectangular shape, however, under an ultra-high operating voltage, in order to avoid high electric fields concentrated at the rectangular corners, the layout



(a)



(b)

FIGURE 6. TLP I-V Curves of circular UHV nLDMOS related DUTs (a) before embedded P-body well and (b) after embedded P-body well.

shape of the DUT is changed to a circular type as shown in Fig. 1(a). A circular layout can make the electric field distribution uniformly and avoid the sharp effects of the high electric field at the end points of the DUT to cause device failure [17]. In order to maintain the high breakdown voltage of the UHV DUT, the long drift region has a lightly doped HV N-Well (HVNW) layer and a RESURF structure formed by a Deep P-Well (DPW) and a P-body well, as shown in Fig. 1(b). The device configuration in this work is formed by a gate-grounded nLDMOSFET (GGnLDMOS) connection. When an ESD event occurred, the ESD current is discharged through the parasitic BJT of the device. Samples of this work are fabricated via a TSMC 0.5-μm 300-V BCD process with the channel length (4-μm), channel width (408.2-μm) and drift region length (29-μm).

B. CONVENTIONAL ARCHITECTURE OF THE UHV CIRCULAR NLDMOS

In order to improve the ESD capability of the device, the first group of DUTs (conventional group) formed a conventional parasitic SCR structure by embedded a P^+ heavily doped layer in the drain side of the UHV nLDMOS reference DUT shown in Fig. 2. The drain-side layout has divided the drain side into three concentric circles, which named respectively the inner regime, the middle regime and the outer regime. By adjusting the location of the P^+ heavy doped layer, the arrangement (named outward from the drain circle center) is classified into eight kinds: NNN- (the Ref. DUT), PNN-, NPN-, PPN-, NPN-, PNP-, NPP-, and PPP-type as shown in Fig. 3. Meanwhile, the corresponding trigger voltage (V_{t1}), holding voltage (V_h), secondary breakdown current (I_{t2}) and human body model (HBM) data of these different arrangement DUTs could be evaluated.

C. PROPOSED ARCHITECTURE OF THE UHV CIRCULAR NLDMOS

Generally speaking, due to the parasitic SCR path, the ESD capability of the device can be greatly improved. However, a large internal resistance of an UHV device makes the ESD capability of the traditional parasitic SCR architecture does not match the expectation as that applied to LV and HV devices. Furthermore, the normal operating voltage of this UHV device is high enough and the LDMOS device has a very low on-resistance with an embedded SCR architecture, which lowers the holding voltage and increases the risk of latchup effect. Therefore, the second group (novel group) of the DUTs embedded a low-doped P-body layer under the drain side P^+ heavy-doped layer to form a concentration gradient mechanism at the drain side through the P-body well, and the P-body resistance (R_{Pbody}) can also increase the on-resistance of the DUT to reduce the peak of an ESD current. And because this P-body layer existed in the original DUT, which improved the ESD capability and holding voltage without adding any extra process step (& photomask) or layout area. The novel SCR architecture and new drain side layout types are shown in Figs. 4 and 5, respectively. Same as before, after these UHV LDMOS devices have inserted the P-body layer under the parasitic SCR, seven new DUTs can further explore the impact of this embedded P-body layer on the corresponding V_{t1}, V_h, I_{t2} and HBM values.

III. RESULTS AND DISCUSSION

To investigate the ESD behavior and robustness of the conventional and purpose architecture, the TLP and HBM measurements were carried out at package level. The TLP system has calibrated before measuring to eliminate the system series resistances. The TLP system used a 100-ns short pulse width square wave and has a short rise/fall time of $<$10-ns to measure the voltage and current transient response of the square wave through the DUT. And, the HBM system is based on MIL-STD-883G method 3015.7. The failure criteria setting of the DUTs is that the leakage current of the pin under test is fixed at $\pm$ 1μA and if the voltage change is over $\pm$30% before and after the ESD zapping, then this pin is judged as failing at this zapped level.

After rigorous breakdown voltage, TLP and HBM tests, the experimental results of these UHV nLDMOS related

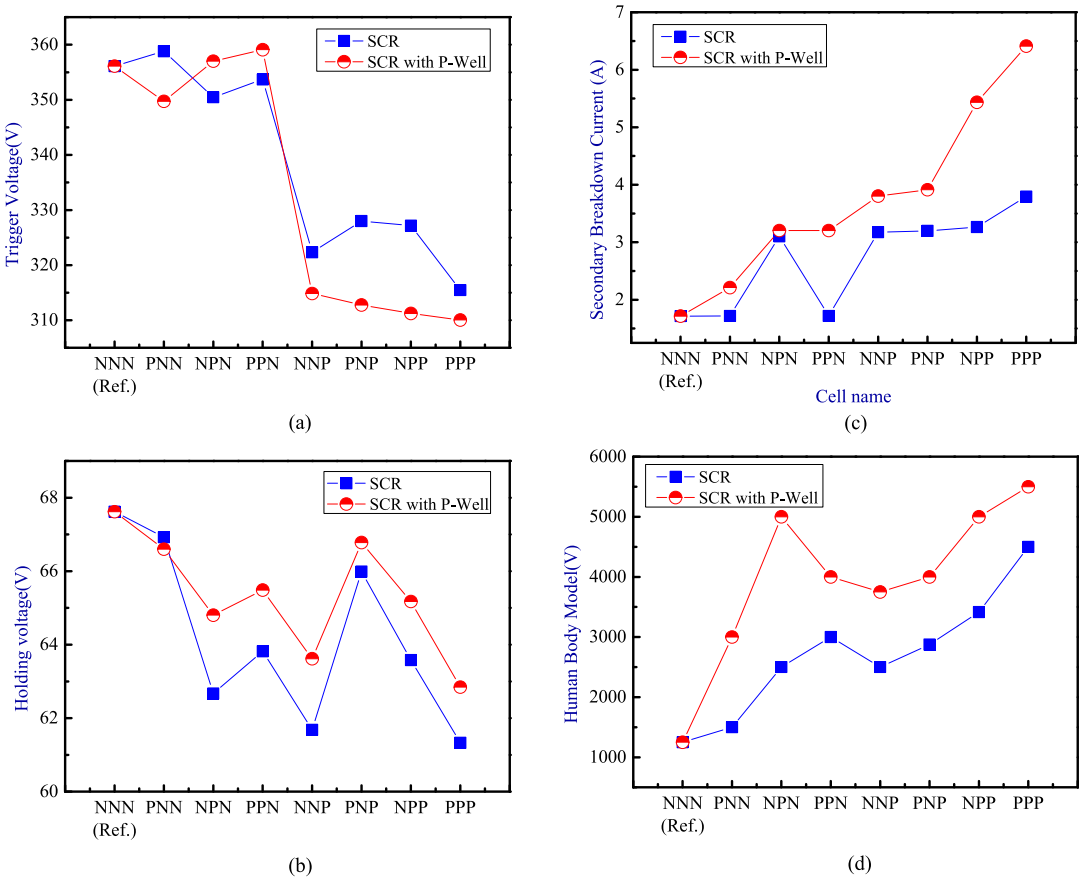


FIGURE 7. Trend charts of circular UHV nLDMOS related DUTs (a) V_{t1}, (b) V_h, (c) I_{t2} and (d) HBM values.

TABLE 1. Devices list and snapback key parameters of nLDMOS-SCRs and nLDMOS-SCRs with the P-body well.

Sample Types		V_{t1} (V)	V_h (V)	I_{t2} (A)	HBM (V)	V_{BK} (V)	FOM (μA×V /μm²)
nLDMOS		356.12	67.62	1.71	1250	388.97	6706.66
Conven. SCR	PNN	358.82	66.93	1.72	1500	385.79	6677.05
	NPN	350.47	62.67	3.10	2500	385.97	11268.25
	PPN	353.70	63.82	1.72	3000	387.40	6366.79
	NNP	322.34	61.68	3.18	2500	388.10	11597.78
	PNP	328.01	65.99	3.20	2875	386.65	12247.94
	NPP	327.17	63.58	3.27	3416	385.48	12058.78
	PPP	315.47	61.33	3.80	4500	385.11	13517.35
Novel SCR with P-body well	PNN	349.73	66.60	2.21	3000	384.84	8536.93
	NPN	357.02	64.80	3.20	5000	387.98	12027.07
	PPN	359.09	65.49	3.21	4000	385.58	12193.13
	NNP	314.85	63.62	3.80	3750	386.49	13931.71
	PNP	312.77	66.78	3.91	4000	380.79	15144.61
	NPP	311.24	65.18	5.43	5000	385.48	20528.12
	PPP	310.05	62.85	6.41	5500	385.55	23374.04

DUTs are shown and listed in Figs. 6–7 and Table 1. According to the measurement results, when the outer regime is P^+ heavily doped layer, the DUTs have a lower V_{t1} due to the path of the parasitic SCR is the shortest, which makes the behavior of the parasitic SCR more obvious and affects the V_{t1}. After being embedded the P-body well, due to the increase of the P-type regime, the parasitic SCR has a larger active area. Consequently, the behavior of the parasitic SCR will be more obvious than that without the embedded P-body layer, so the V_{t1} value will decrease. Since the parasitic SCR active path has added the R_{Pbody} resistance, which increased the holding voltage of the DUT, thereby improving the LU immunity of the DUT compare to traditional parasitic SCR architecture. However, from Table 1, it shows that the V_{BK}'s values variations do not exceed 1.5% after adding the P-body layer. When the traditional parasitic SCR architecture is applied to UHV DUTs, since the operating voltage of the DUT is greater than that of the LV and HV devices, even if the parasitic SCR is applied to UHV nLDMOS, the improvement of ESD ability is limited.

However, by the proposed architecture, the drain-side anode P^+ heavy doped layer embedded a low-doped P-body well, a concentration gradient has formed at the drain end. This physical mechanism can reduce the peak value of the electric field, also greatly increase the active area of the parasitic SCR, thereby making the behavior of the parasitic SCR more obvious to improve the ESD and FOM (LU immunity included) capabilities of the DUT. Meanwhile, this novel SCR architecture without affecting the breakdown voltage of the DUT although it added the P-body well at the drain

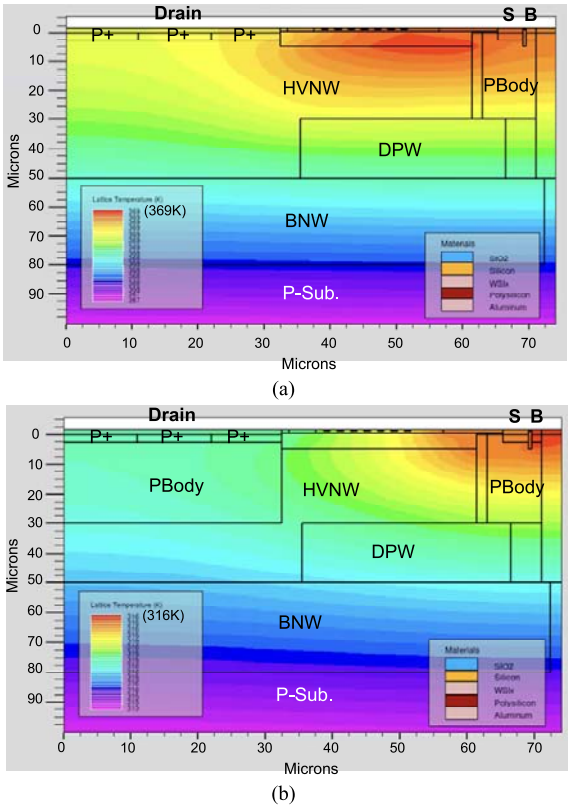


FIGURE 8. Lattice temperature distribution of (a) the nLDMOS-PPP type device and (b) the nLDMOS-PPP with drain-side P-body type device (under the same drain(anode)-side 1×E-7 A/cm^2 current injection).

side, so the proposed architecture will not reduce the basic characteristics of the DUTs.

Next, the Silvaco EDA software was used to simulate a two-dimensional lattice temperature distribution. Fig. 8 shows that the two-dimensional lattice temperature distribution of the UHV nLDMOS-PPP type (Conventional embedded SCR) and the nLDMOS-PPP with P-body type (Novel embedded SCR) devices under the same drain(anode)-side condition at 1×10^{-7}A/cm^2 current injection and other electrodes were grounded. Obviously, the highest lattice temperature can be reached 369 K for the UHV nLDMOS-PPP type (Conventional embedded SCR) device, while the nLDMOS-PPP with P-body type (Novel embedded SCR) device can only reach 316 K. Therefore, the ESD ability of this newly proposed device is better than those of the UHV nLDMOS-PPP type (Conventional SCR) device. Finally, it can be concluded that this low-doped P-body well added under the drain-side embedded SCR can effectively reduce current hot spot (lattice temperature), thereby the I_{t2} and HBM capabilities of the UHV DUTs are greatly enhanced.

IV. CONCLUSION

For an UHV nLDMOS Ref. DUT with poor ESD ability (I_{t2} 1.71-A, HBM 1250-V), a novel SCR architecture which embedded a low-doped P-body well under the traditional anode of parasitic SCR (P^+ heavily doped layer) at the drain side of the UHV nLDMOS device is investigated. The ESD ability increased due to the embedded P-body layer at the drain side of a conventional architecture that formed a concentration gradient to reduce the peak electric field, and also increased the SCR active area. According to the measurement results, this novel SCR architecture can effectively increase the DUT maximum sustaining current (I_{t2}) when a P^+ heavily doped layer has embedded at the outer regime. The DUT with the best FOM device (PPP-arranged type) increased the I_{t2} value from 3.8-A to 6.41-A (increased about 68.7%), and the HBM capability increased from 4500-V to 5500-V (increased about 22.2%) as compared with the conventional SCR structure. Meanwhile, this novel SCR architecture also slightly increased the maximum sustaining current of N^+ heavily doped layer embedded at outer regime (for example the PPN-arranged type) from 1.72-A to 3.21-A (increased 86.6%), and HBM ability from 3000-V to 4000-V (increased 33.3%) as compared with the conventional SCR structure.

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