Analysis of Trap and Recovery Characteristics Based on Low-Frequency Noise for E-Mode GaN HEMTs Under Electrostatic Discharge Stress

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ABSTRACT The ESD effects on the E-mode AlGaN/GaN high-electron mobility transistors (HEMTs) with p-GaN gate are investigated under repetitive TLP pulses. Firstly, the degradation and recovery of output, transfer characteristics, gate-leakage characteristics and low-frequency noises (LFN) are analyzed in detail before and after reverse electrostatic discharge (ESD) stress. The experimental results show that the electrical characteristics of the devices gradually degraded as the transmission line pulse (TLP) pules increased. Subsequently, the LFN measurements are performed over the frequency range of 1 Hz–10 KHz by increasing TLP pulses. Finally, the recovery tendency of *DC* (direct current) characteristics and trap density are studied and discussed after resting the device at room temperature for 1 to 3 months. These results physically confirm that the mechanism of the performance degradation and recovery of the devices could be attributed to the trapping and releasing processes of electrons in the p-GaN layer and AlGaN barrier layer of AlGaN/GaN HEMTs, which change the electric field distribution under the gate.

INDEX TERMS AlGaN/GaN, high-electron-mobility transistor (HEMT), recovery, reverse ESD stress, low-frequency noise (LFN).

I. INTRODUCTION

During the past decade, Gallium nitride (GaN) has attracted great attention due to its impressive properties like wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm) and low dielectric constant (9). Moreover, the large two-dimensional (2-D) electron gas concentration confined by a larger conduction band discontinuity between GaN and AlGaN and the presence of polarization fields enhances the carrier mobility (1500-2000 cm^{-2}/V) in AlGaN/GaN material system [1]. As a result, the high two-dimensional electron gas (2DEG) density (10^{13} cm^{-2}), high electron peak velocity (3×10^7 cm/s) and high electron saturation velocity (1.5×10^7 cm/s) constitute important advantages of AlGaN/GaN hetero-junction with respect to their silicon (Si) and GaAs counterpart [2]–[4]. GaN-based high-electron mobility transistors (HEMTs) are emerging as a key technology for high frequency, high power, and high temperature applications [5]–[9].

In GaN-based AlGaN/GaN HEMTs, the 2DEG forms in the AlGaN/GaN hetero-junction natively without gate bias voltage. Which result in GaN HEMTs are normally-on switches (Depletion mode HEMTs, DHEMTs). However, the devices are required to exhibit a normally-off operation in most applications. In response to this, the p-doped gates (p-gate) is adopted as one of the key technological solutions to achieve normally-off Enhancement-mode HEMTs (E-HEMTs) [10]–[12].

Despite the cost of AlGaN/GaN HEMT has significantly reduced, electrostatic discharge (ESD) related reliability still represents a great threat to its widespread use though GaN

has demonstrated a high breakdown field of 3.3 MV/cm. As the market is growing, the long-term reliability issues of GaN HEMTs have been widely investigated in the literature. Among the issues, the device capability to survive the fast transients and high injection conditions, such as ESD, is very critical. For instance, Tazzoli *et al.* reported ESD robustness of HEMTs with 100-ns transmission line pulse (TLP), and showed that the HEMT failure is triggered by gate-source diode degradation [13]. Rossetto *et al.* reported field- and power-dependent failure in GaN HEMT under OFF- and ON-state, respectively. And the scanning electron microscopy was extensively used to achieve a complete description of the failure processes [5]. Kuzmík *et al.* compared the effects of drain-source TLP tests performed with gate grounded or floating, and prove that damage is due to current filamentation and high density electron flow [14], [15]. On the other hand, Fernández *et al.* [10] investigated the snapback behavior in AlGaN/GaN HEMTs. The role of the Schottky gate and MESA is investigated using special test structures. Besides, the influence of piezoelectric field, carrier trapping, and self-heating on ESD behavior are studied [1], [16], [17]. Due to the respectable noise performance, GaN HEMT technology are attracting a significant interest not only for power applications, but also for low-noise amplifications [18]–[21].

However, those investigations only present a comprehensive experimental study of the ESD behavior of the GaN HEMT. Despite p-GaN HEMTs are commercially available, the root cause for the ESD robustness and degradation remains unknown. Moreover, to the best of our knowledge, no detailed analysis of the degradation and recovery characteristics of E-mode GaN HEMTs with p-GaN gate under reverse ESD stress has been presented so far in the literature. In our previous research, the effect of TLP stress on an E-mode GaN HEMTs with p-GaN gate which are manufactured by Panasonic was investigated under high reverse voltage (-200 V) [22]. The permanent degradation of the device was observed and the characteristics of devices shows no signs of recovery.

The aim of this article is to investigate the degradation and recovery characteristics of AlGaN/GaN HEMTs with p-GaN gate under reduced repetitive TLP voltage of -80 V to intentionally slow down the device degradation, which means not cause permanent damage to the DUTs. Besides, their failure mechanisms are qualitatively analyzed based on the low-frequency noises (LFN) method. The results may provide useful guidelines for E-mode GaN HEMTs applications.

II. EXPERIMENTAL

The Devices Under Test (DUTs) employed in this work were commercially available single-chip, lateral 48 A–150 V E-mode AlGaN/GaN power switching HEMTs from EPC Inc. The device has a typical on-state resistance of 7 mΩ and a thermally stable threshold voltage of 1.4 V. The AlGaN/GaN hetero-structure of DUTs consists of an AlGaN barrier layer, a GaN transition layer, and a GaN buffer layer. The schematic and test structures of the typical DUT are
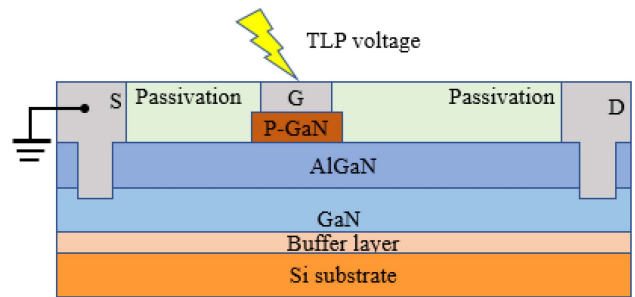

FIGURE 1. Schematic view of the studied AlGaN/GaN HEMT. Artwork not in scale.
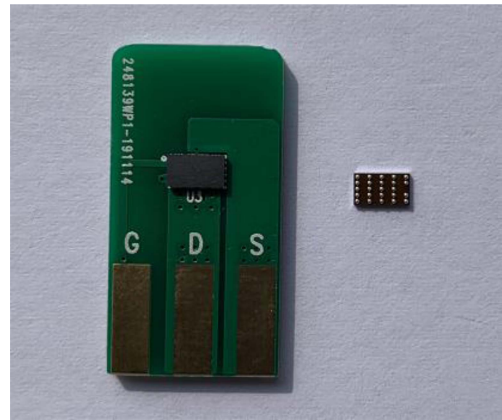

FIGURE 2. Photograph of the studied AlGaN/GaN HEMT in PCB package and the backside of the single-chip.
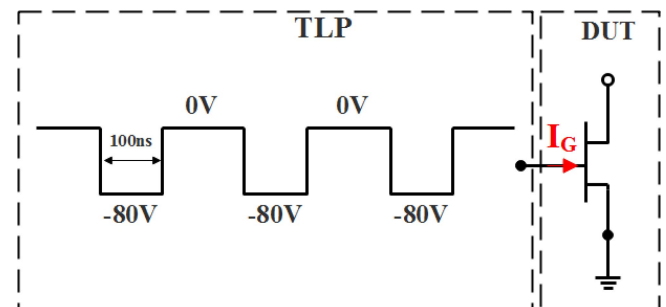

FIGURE 3. Schematic diagrams of the proposed experiment setup.

shown in Fig. 1. For the purpose of testing convenience, the PCB package is adopted as photographed in Fig. 2 (compare to the single-chip DUT) to achieve the TO-247 package type. Furthermore, the DUTs are tested in the same package before and after repetitive ESD stress. The schematic of the experiment setup used for the tests is reported in Fig. 3. To understand the true influence of ESD stress on device degradation, the reverse 100 ns pulse stress was applied to the gate of DUTs by time-domain reflection TLP custom system (TDR-TLP). The test structures used in this work are with the drain under floating and source grounded condition. *DC* (direct current) characteristics are measured under various configurations using a semiconductor characterization system (Model: Agilent B1505A) at room temperature. The
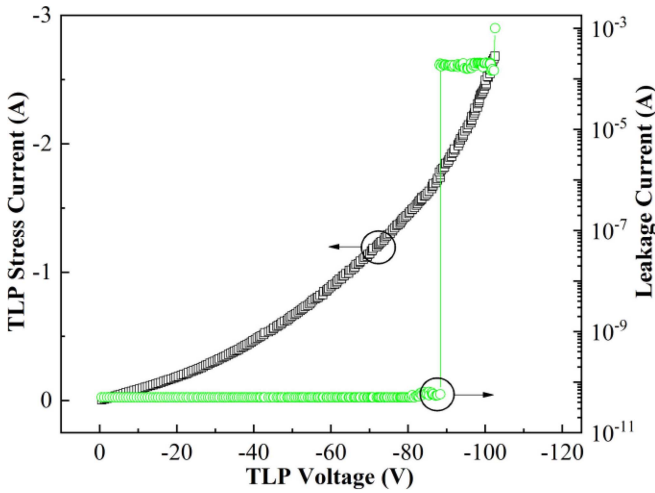
FIGURE 4. Degradation in gate-to-source TLP stress current and leakage current of DUTs under TLP stress (100ns) at gate.

FIGURE 5. Output characteristics $I_d - V_{ds}$ of AlGaN/GaN HEMTs before/after repetitive TLP pulses.

LFN performances are characterized by an SR785 dynamic signal analyzer, while filter and amplifier units are provided by Proplus 9812B. To improve the efficiency and accuracy of the test, the recovery characteristics are measured after resting the DUTs for 1 month and 3 months. New devices from the same batch have been utilized for different test groups to avoid accumulated degradation.

The gate-to-source TLP stress current and leakage current degrades of DUTs with each TLP pulse applied at the gate as shown in Fig. 4. An increasing reverse TLP voltage stress is applied to the gate of DUT. The leakage current ($I_{leakage}$) were obtained during breaks with the *DC* voltage of 0.5 V, which was purposed to trace the degradation of the devices. As shown in Fig. 4, a steeply rising of $I_{leakage}$ from 5.7×10^{-11} to 2×10^{-4} A is observed within the reverse TLP voltage stress of −87 V which indicates that the gate of the DUT had been broken down. To investigate the degradation and recovery characteristics of DUTs, the results in our following experiments were obtained at reduced TLP voltage of −80 V to intentionally slow down the device degradation during the repetitive TLP operation, which means not cause permanent damage to the DUTs.

III. RESULTS AND DISCUSSION

Drain-to-source current (I_d) was found to be an important parameter for monitoring the health of HEMTs under ESD conditions. In order to study the degrade of electrical parameters during TLP stress, we have then made a complete *DC* electrical characterization at selected TLP steps. Typical $I_d - V_{ds}$ curves with drain-source voltage (V_{ds}) ranging from 0 to 5.5 V, obtained before and after different TLP stress of 0, 20 and 400 pulses, are reported in Fig. 5. As can be noticed, the curves are measured at gate-source voltage (V_{gs}) values ranging from 2 to 4.5 V. The I_d values obviously decrease with the increase of TLP pulses at the same V_{gs}. For instance, the typical I_d value decreases from 27.27 A to 0.069 A after 400 TLP pulses at $V_{gs} = 2.5$ V
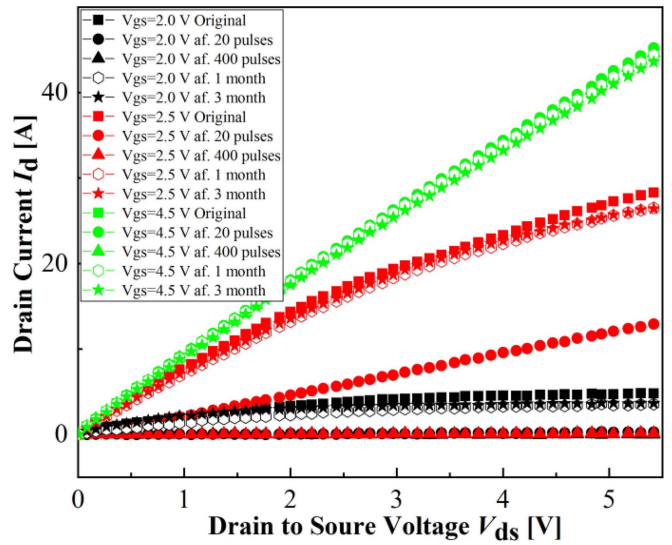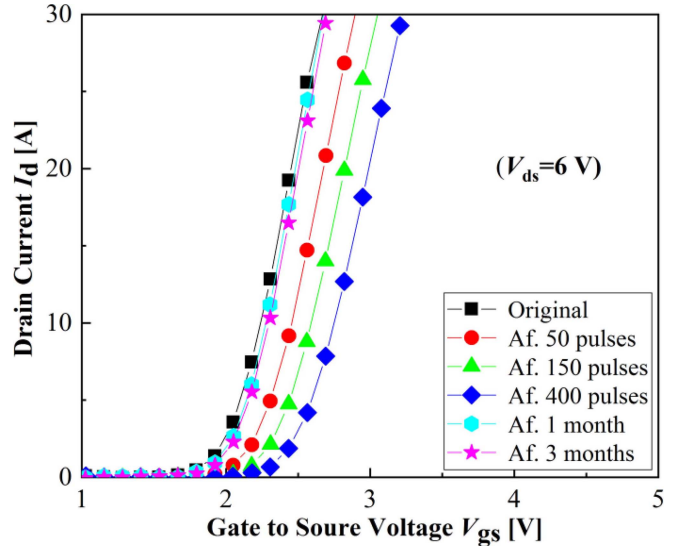

FIGURE 6. Transfer characteristics $I_d - V_{gs}$ of AlGaN/GaN HEMTs before/after repetitive TLP pulses.

and $V_{ds} = 5$ V. After resting the DUTs for 1 month at room temperature, the output characteristics of the devices shows an obvious trend of recovery. The I_d value increases from 0.069 A to 25.609 A with $V_{gs} = 2.5$ V and $V_{ds} = 5$ V, which is almost recovery to the original state of the DUTs. The TLP dependent transfer characteristics and transconductance (g_m) characteristics are obtained, Fig. 6 and Fig. 7 show the typical $I_d - V_{gs}$ and $g_m - V_{gs}$ characteristics of the DUT with V_{gs} values ranging from 0 to 5 V, respectively. As can be observed, the $I_d - V_{gs}$ and $g_m - V_{gs}$ curves of the DUT obviously demonstrate a positive shift (≈ 0.6 V) and a max g_m slight decrease (≈ 6.56 S) after 400 TLP pulses, which indicating that the modulation of the gate has weakened and electrons have been depleted in the channel of the DUT
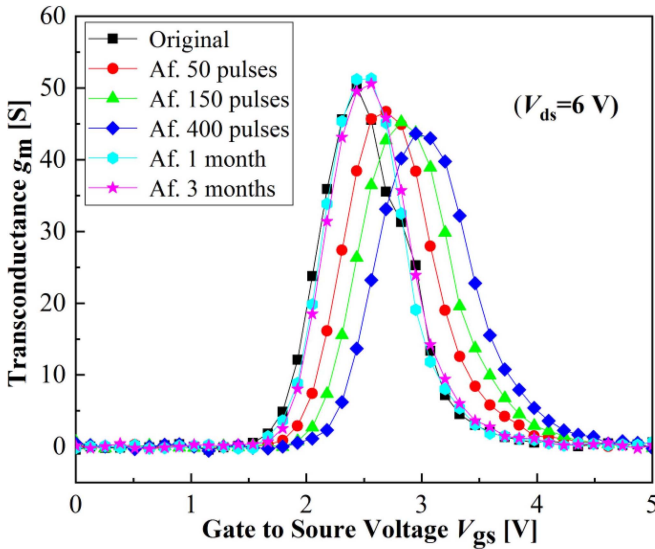
FIGURE 7. Transconductance characteristics $g_m - V_{gs}$ of AlGaN/GaN HEMTs before/after repetitive TLP pulses.
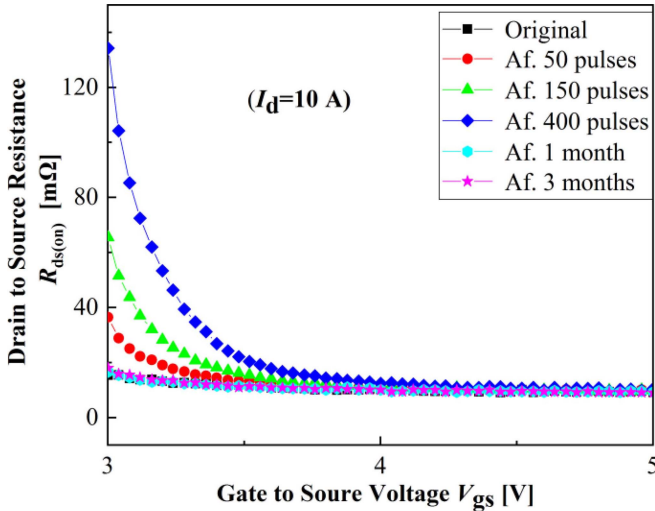

FIGURE 8. Drain-to-Source on resistance characteristics $R_{ds(on)} - V_{gs}$ of AlGaN/GaN HEMTs before/after repetitive TLP pulses.

FIGURE 9. Gate-to-source leakage current characteristics $I_{gss} - V_{gs}$ of AlGaN/GaN HEMTs before/after repetitive TLP pulses.

FIGURE 10. Drain-to-source leakage current characteristics $I_{dss} - V_{ds}$ of AlGaN/GaN HEMTs before/after repetitive TLP pulses.

induced by repetitive TLP pulses. We can therefore suggest that, during the TLP pulses, the degradation takes place under the gate region. After resting the DUTs for 1 month at room temperature, the transfer characteristics and transconductance characteristics of the devices show a similar trend of recovery with output characteristics.

Fig. 8 summarizes the typical TLP dependent $R_{ds(on)} - V_{gs}$ characteristics of the DUTs. The drain-source resistance ($R_{ds(on)}$) values increase with the increase of TLP pulses and show recovery features after 1 month of resting at room temperature, which is in excellent agreement with the previous results in this article. The increase and recovery of $R_{ds(on)}$ is a result of the threshold voltage (V_{th}) shift as shown in Fig. 6. Meanwhile, in order to investigate the effect of TLP pulses on the p-GaN layer and channel of DUT, the gate to
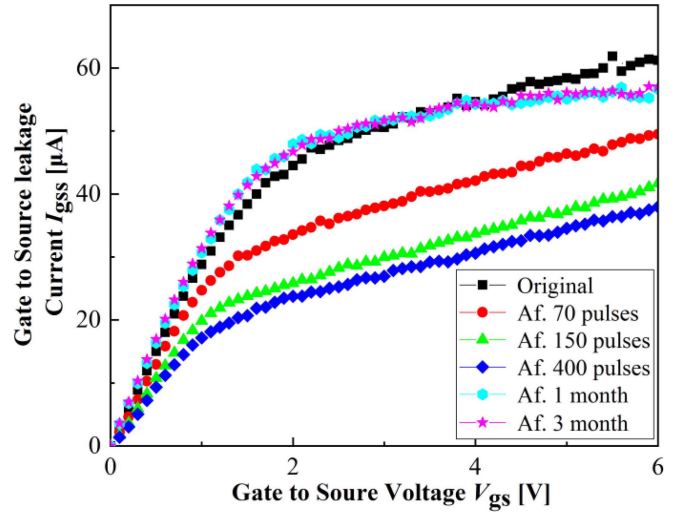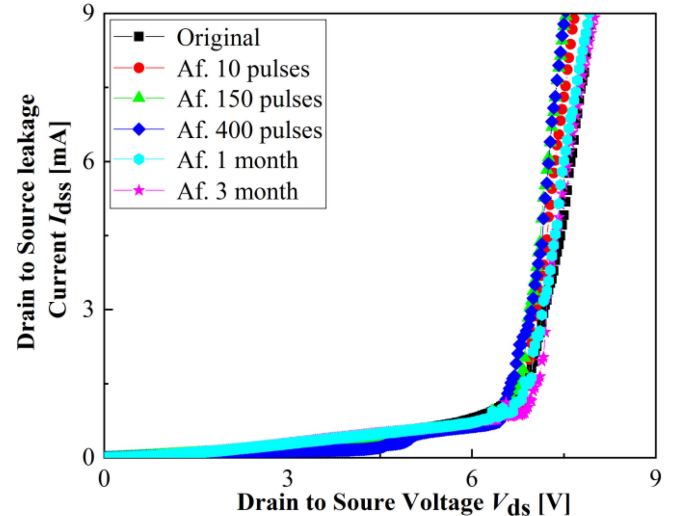
source leakage current ($I_{gss} - V_{gs}$) and drain to source leakage current ($I_{dss} - V_{ds}$) characteristics of the device within the positive V_{gs} are also monitored and shown in Fig. 9 and 10, respectively. The leakage current after 400 TLP pulses decrease from 61.2 µA to 37.9 µA at the measured voltage of +6 V, and recovery to 56.6 µA after 1 month of resting. However, the $I_{dss} - V_{ds}$ characteristics show a slight increase after 400 TLP pulses, which indicates that the TLP stress causes no actual damage to the channel of the DUT, but increase the number of conducting carriers in the channel when the DUT is in off-state. After 1 month of resting, it shows a similar trend of recovery with previous results. Moreover, in general no further recovery tendency in the DC characteristics is observed, even if the samples are kept resting for more than 3 months, which is shown in Fig. 5 to Fig. 10.
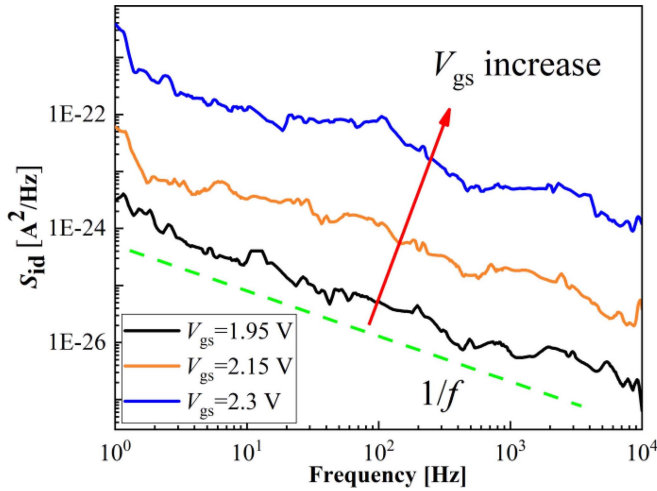
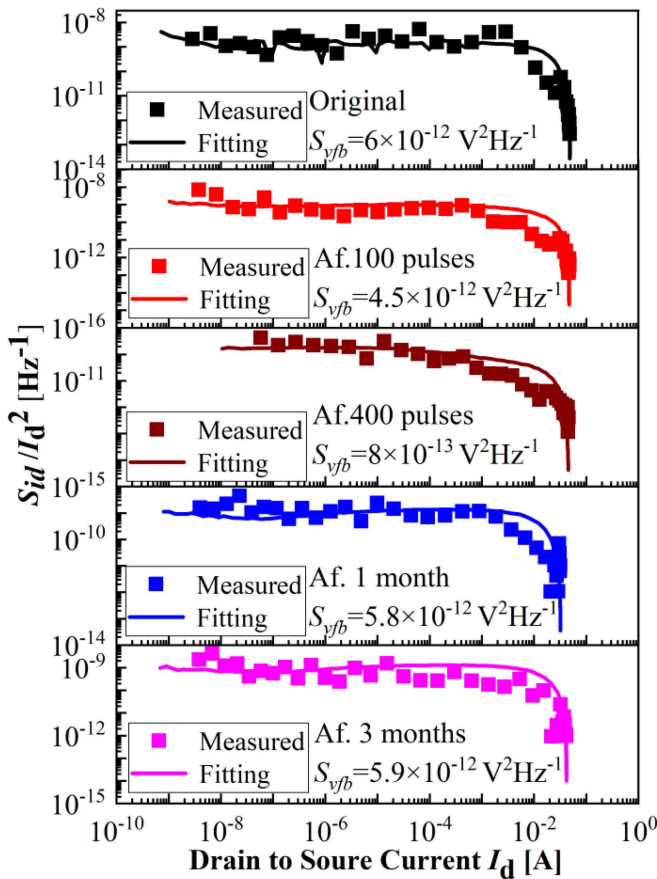**FIGURE 11.** Drain current noise power spectral densities versus frequency for the original devices.

FIGURE 12. The S_{id}/I_d^2 at 10 Hz versus I_d for the original devices and devices after repetitive TLP pulses.

LFN measurements were proven to be an efficient tool to characterize the defects and the density of interface states existing in microelectronic devices, are widely used for reliability assessment of technologies [23], [24]. Signatures of the current or voltage spectral densities bring information about the crystal purity (1/f noise source) of the devices [25].

To further analyze the effect of repetitive TLP stress on the DUTs, the typical LFN spectrum are plotted in Fig. 11, which is obtained under various V_{gs} at $V_{ds} = 0.1$ V. For the original DUT, the drain current noise power spectrum densities (S_{id}) clearly show a pure 1/f- type spectrum with the frequency (Č) in the range of 1 Hz to 10 kHz, as shown in Fig. 11. There are two principal mechanisms to determine the origin of LFN, consist of carrier number fluctuation (ΔN) theory and mobility fluctuation ($\Delta \mu$) theory. According to the classic carrier number fluctuation (ΔN) theory (McWhorter model), the 1/f noise is induced by the fluctuations of interfacial charges, which are related to the trapping and de-trapping processes of free mobile carriers in the grain boundary and border traps close to the channel interface [26], [27]. The normalized drain current noises spectral versus I_d taken at 10 Hz before and after repetitive TLP pulses are plotted in Fig. 12. Based on McWhorter model, the drain current noise can be evaluated as [26]:

$$\frac{S_{id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{vfb} \tag{1}$$

where g_m is the device transconductance, S_{vfb} is the input-referred flat-band spectral noise density.

For a pure ΔN model, S_{vfb} can be expressed by:

$$S_{vfb} = \frac{q^2 kT\lambda N_t}{WLfC_b^2} \tag{2}$$

where $\lambda = 0.5$ is the tunneling attenuation coefficient for AlGaN, W and L are the gate width and length, respectively. C_b is the AlGaN barrier capacitance and N_t is the trap density includes traps in the grain boundaries, interface traps, and the traps in the p-GaN layer, which is mainly attributed to the traps distributed near the p-GaN/AlGaN/GaN heterointerface [26], [27].

According to Eq. (1) and (2), S_{vfb} and N_t can be extracted. Without knowing the values of W and L, the N_t of original DUT is assumed to N_{t0}. The extracted N_t decreases by about an order of magnitude from N_{t0} to $0.13N_{t0}$ for DUTs after 400 TLP pulses. Moreover, the N_t recover to $0.97N_{t0}$ after 1 month of rest and eventually return to $0.98N_{t0}$ after 3 months of resting, almost recovery to the original state, which is in excellent agreement with the previous *DC* characteristics as shown in Fig. 5 to Fig. 10.

As presented in Fig. 13 and 14, The physical mechanism responsible for the degradation of AlGaN/GaN HEMTs under repetitive TLP stress is explained as follows [28]. There are several kinds of acceptor-like defects acting as traps are located in the p-GaN region and AlGaN barrier layer of the device as shown in Fig. 13 (a) and (b) [29]. As for the devices after repetitive TLP stress, the large negative gate voltage results in the electron injection to the p-GaN layer and AlGaN barrier layer from the gate [30], [31]. Note that the injection of the electrons from the gate to the channel is well suppressed by the heterobarrier at AlGaN/GaN heterojunction [32]. The electrons could be filling the acceptor-like traps, which is marked with red circles
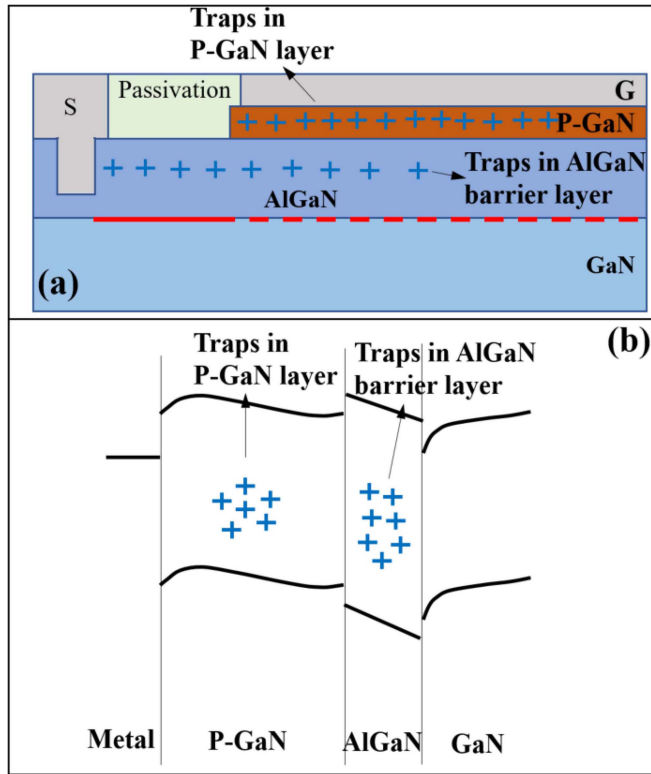
FIGURE 13. (a) 2DEG and traps in the p-GaN layer and AlGaN barrier layer for the original AlGaN/GaN HEMTs, (b) Energy-band diagram of 2DEG and traps in the p-GaN layer and AlGaN barrier layer for the original AlGaN/GaN HEMTs.

FIGURE 14. (a) Electron injection process for the AlGaN/GaN HEMTs during repetitive TLP pulses, (b) Energy-band diagram of electron injection process for the AlGaN/GaN HEMTs during repetitive TLP pulses.

and arrows. The injected electrons in the p-GaN layer and AlGaN barrier layer induce an electrostatic effect, that results from the negative charge accumulated at the acceptor-like traps, which eventually results in the depletion of electrons in the 2DEG. This conductivity modulation results in a significant decrease of the drain current. Afterwards, the electric field distribution under the gate is changed due to change in the traps occupancy as shown in Fig. 14, and it is supported by the extracted N_t results as shown in Fig.12. This also leads to the degradation of DC characteristics as shown in Fig. 5 to Fig. 9. Besides, the accumulated holes in the channel lead to a slight increase of I_{dss}, as illustrated in Fig. 10. After 1 month of resting, the electrons captured by the traps are nearly all released and the electric field distribution almost returns to the original state, which results in the recovery features as shown in Fig. 5 to Fig. 10 and Fig. 12. The DC characteristics are basically stable even if the samples are kept resting more than 3 months owing to almost no electrons are retaining on the traps after 1 month of resting.

IV. CONCLUSION

In summary, The ESD effect on conduction and low frequency noise characteristics in the E-mode AlGaN/GaN HEMTs with p-GaN gate are investigated under repe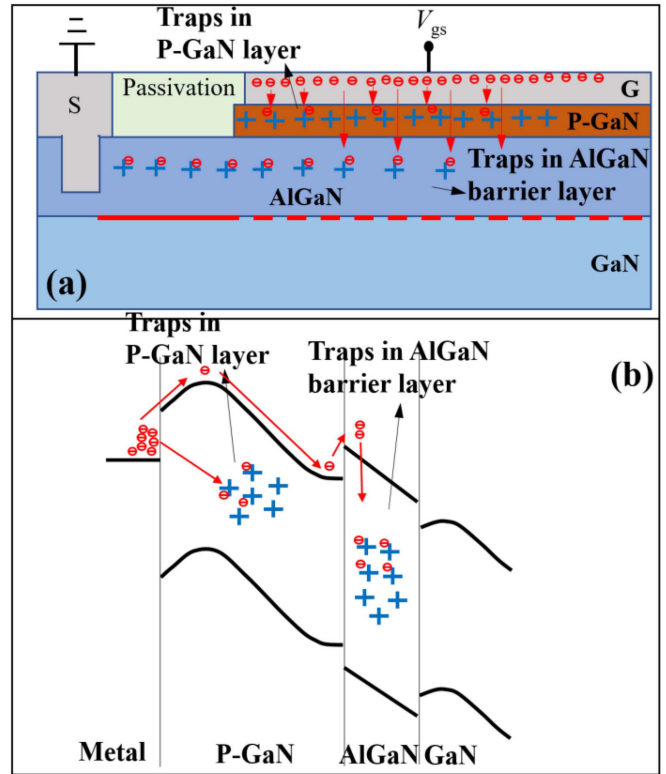titive TLP pulses. The degradation and recovery behavior are examined. The ESD stress leads to the degradation of DC characteristics of the devices, such as the positive shift of the threshold voltage and transconductance peak value, and $R_{ds(on)}$ increases obviously. In addition, based on the LFN method, measured low frequency noises show a pure $1/f$ type spectrum, the trap density appears an obvious decrease for the devices after repetitive TLP pulses. After a period of time of resting, the trap density and DC characteristics of the device show a similar recovery tendency. The corresponding physical mechanism could be attributed to the trapping and releasing processes of electrons in the p-GaN layer and AlGaN barrier layer, which change the electric field distribution under the gate. Due to the sensitivity of III–V compounds to the ESD phenomena, the results of this article would significantly benefit the design and application of E-mode GaN power devices, especially when the devices applied to harsh conditions such as automotive and power conversion fields.

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