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Assessment of Linear, Hexagonal, and Octagonal Cell Topologies for 650 V 4H-SiC Inversion-Channel Planar-Gate Power JBSFETs Fabricated With 27 nm Gate Oxide Thickness

ADITI AGARWAL (Graduate Student Member, IEEE), KIJEONG HAN, AND B. J. BALIGA (Life Fellow, IEEE)

Electrical and Computer Engineering Department, North Carolina State University, Raleigh, NC 27695, USA

CORRESPONDING AUTHOR: A. AGARWAL (e-mail: aagarw12@ncsu.edu)

ABSTRACT A 27 nm gate oxide thickness has been successfully used for manufacturing high performance 650V 4H-SiC planar-gate, inversion-channel power JBSFETs in a 6-inch commercial foundry with three (Linear, Hexagonal, and Octagonal) cell topologies. The 27 nm gate oxide thickness allows operation of these JBSFETs at a gate bias of 15 V compared with 20 V used in previous reports for devices with 55 nm gate oxide thickness. The width for the Schottky contact was varied to optimize the performance of the JBS diode in the third quadrant for each cell topology. An on-state voltage drop of 2.5 V or less was achieved in the third quadrant for all the cell topologies by current flow through the integrated JBS diode, satisfying the objective of effectively by-passing the MOSFET body diode. The best breakdown voltage was achieved using the Octagonal cell topology with a half-cell Schottky contact width of 1.1 μm. It had a breakdown voltage of 850 V with a low leakage current of less than 5 nA at 650 V. The Linear cell (with half-cell Schottky contact width of 1.0 μm) and the Octagonal cell (with half-cell Schottky contact width of 2.8 μm) had blocking voltages of 800 V. The hexagonal cell topology (with half-cell Schottky contact width of 1.5 μm) had the worst blocking voltage of 715 V. Numerical simulation results are provided to show that the leakage current in all cell topologies begins to increase when the electric field at the Schottky contact exceeds 1.5 MV/cm. The lowest specific on-resistance was obtained with the hexagonal cell topology but its gate-drain charge was 2× larger than the conventional Linear cell design. The Octagonal cell topology with half-cell Schottky contact width of 1.1 μm had the same specific on-resistance as the Linear cell case with 2× smaller gate-drain charge. This work demonstrates for the first time that excellent High-Frequency Figures-of-Merit can be achieved with a reduced gate drive voltage of 15 V for 650 V SiC JBSFETs by using a smaller gate oxide thickness of 27 nm and the Octagonal cell topology.

INDEX TERMS Silicon carbide, 4H-SiC, inversion, JBSFET, cell topology, linear, hexagonal, octagonal, gate oxide thickness.

I. INTRODUCTION

Silicon carbide (SiC) power MOSFET products have been established over a broad range of voltage ratings [1]. In early years, a majority of the effort focused on 1.2 kV devices to replace silicon IGBTs [2], [3], [4]. More recent effort has targeted devices with voltage ratings of 1.7-3.3 kV [5], [6], [7], [8], [9]. These MOSFETs rely up on the conventional Linear cell topology. Various cell topologies have been compared for 1.2 kV rated SiC planar-gate power MOSFETs without the integrated JBS diode [10], [11]. The previous publications by our group on various cell topologies for 600 V SiC MOSFETs [12] had a 50 nm gate oxide and did not include devices with integrated JBS diodes. 600 V linear cell SiC power MOSFETs with 27 nm gate oxide were demonstrated to exhibit favorable characteristics when operated with IGBT compatible 15 V gate drive [13].

Most pertinent to this article, various cell topologies were compared for 1.2 kV SiC planar-gate accumulation-channel JBSFETs with a gate oxide thickness of 55 nm using 20 V gate drive [14]. The previously published papers on SiC JBSFETs discussed above have utilized the standard 50 nm gate oxide thickness with a gate drive voltage of 20 V, and they did not examine the influence of the cell topology for a 650 V MOSFET structure with an integrated JBS diode. In this article, the characteristics of 650 V SiC JBSFETs with various cell topologies are compared for the first time with a gate oxide thickness of 27 nm and gate drive voltage of 15 V. The quantitative performance of 650 V, 27 nm gate oxide JBSFETs is different than that obtained and reported for 27 nm gate oxide 600 V MOSFETs and 1.2 kV JBSFETs. The new experimental information provided in this article will allow readers to assess the quantitative performance of various cell topologies for 650 V JBSFETs with 27 nm gate oxide. These devices can be operated using low cost 15 V gate drivers that are commonly used in high volume for Si power MOSFETs and IGBTs.

An electric field of 5.6 MV/cm is produced in the on-state with a gate bias of 15 V with 27 nm oxide thickness. Reliability tests performed by a leading SiC power MOSFET manufacturer reported a lifetime of 2×10^4 years at 175 °C for this oxide electric field in 2012 [15]. Similar tests by them reported a lifetime of over 200 years at 150 °C for this electric field in 2018 [16]. These results indicate that the gate bias conditions used in this article are acceptable from a reliability stand point. It has been already shown that the electric field in the gate oxide under 600 V blocking condition is only 3.2 MV/cm even for the 27 nm gate oxide case [13]. This is well below the 4 MV/cm reliability criterion used for this mode.

It has been shown that connecting a SiC JBS diode in anti-parallel with the SiC power MOSFET produces reduction in power losses in applications by preventing conduction through the body diode of the MOSFET [17]. However, this additional separate component in its own package adds to the space and cost of the power electronics. The integration of the JBS diode into the 1.2 kV SiC planar-gate linear-cell MOSFET chip, to form the JBSFET structure, was first demonstrated in 2016 [18]. Optimization of the integrated JBS diode in a separate region of the chip and within the MOSFET cell was subsequently discussed and shown to reduce the net SiC chip area and hence its manufacturing cost [19]. Integration of the JBS diode with a 1.2 kV linear-cell planar-gate SiC MOSFET was reported to reduce the peak reverse-recovery current and reverse-recovery charge [20]. A trench-gate linear-cell SiC JBSFET fabricated with a complex process was also reported in 2017 with low specific on-resistance [21].

The avalanche ruggedness and reliability of 650 V JBSFETs was reported in 2018 with a hexagonal layout for the JBS diode not integrated into the MOSFET cell structure [22]. The device had a specific on-resistance of 6.4 mΩ-cm^2 at a gate bias of 20 V in the first quadrant. The JBS diode had a voltage drop of 3.2 V at 10 A, corresponding to a current density of 80 A/cm^2, in the third quadrant. This voltage drop is too large to fully suppress conduction via the body diode especially at elevated temperatures. Most recently, 600 V JBSFETs were reported with a specific on-resistance of 5.6 mΩ-cm^2 at a gate bias of 20 V and an integrated JBS diode with a voltage drop of 2.6 V at 10 A, corresponding to a current density of 217 A/cm^2, in the third quadrant [23].

An understanding of the relative performance of SiC JBSFETs with various cell topologies is valuable for the optimization of this technology at the 650 V rating level. This article reports the characteristics of 650 V SiC JBSFETs fabricated using 27 nm gate oxide thickness with three cell topologies (Linear, Hexagonal and Octagonal) for the first time. It is demonstrated that the gate drive voltage for 650 V SiC JBSFETs can be reduced from 20 V used for previously reported devices to 15 V by decreasing the gate oxide thickness to 27 nm. A gate drive voltage of 15 V is compatible with widely available, low-cost, gate drivers used for silicon IGBTs. In addition, this article provides experimental data for three (Linear, Hexagonal, and Octagonal) cell topologies with the reduced 27 nm gate oxide thickness for the first time at the 650 V rating.

II. STRUCTURAL AND FABRICATION INFORMATION

In order to achieve the desired 650 V rating, 6 μm thick, n-type epitaxial layers with doping concentration of 2.4×10^{16} cm^{-3} were specified on 4H-SiC 6-inch N$^+$ substrates as starting material. The JBSFETs were manufactured at the X-Fab foundry using the NCSU engineered PRESiCE^{TM} process with 11 mask layers [24]. The hybrid-JTE edge termination was applied to all the devices because it provides an edge breakdown voltage close to the ideal parallel-plane case [25]. The hybrid-JTE edge termination did not determine the leakage current or breakdown voltage for the JBSFETs described in this article.

The cross-sections of the cells in the JBSFETs with different cell topologies are similar with the common features shown in Fig. 1. The JBS diode is integrated into the power MOSFET cell by opening a gap in the P$^+$ shielding region at the center of the opening in the polysilicon gate electrode. A P$^+$ contact ion-implant is utilized in the power MOSFET cells to make a good ohmic contact to the P$^+$ shielding region as shown in the figure. This P$^+$ contact region is utilized in the JBS diode to suppress high leakage current during blocking large voltages [26], [27]. The JFET region doping concentration is enhanced to 5.4×10^{16} cm^{-3} for improving the MOSFET on-resistance [28]. This enhanced doping is also applied to the region below the Schottky contact to reduce its series resistance. Fig. 1(b) shows the doping concentration of all the regions along a horizontal cutline parallel to AA' slightly below the gate region. Fig. 1(c) shows the post-implant doping profile in the vertical direction for the P-Base and P$^+$ regions.

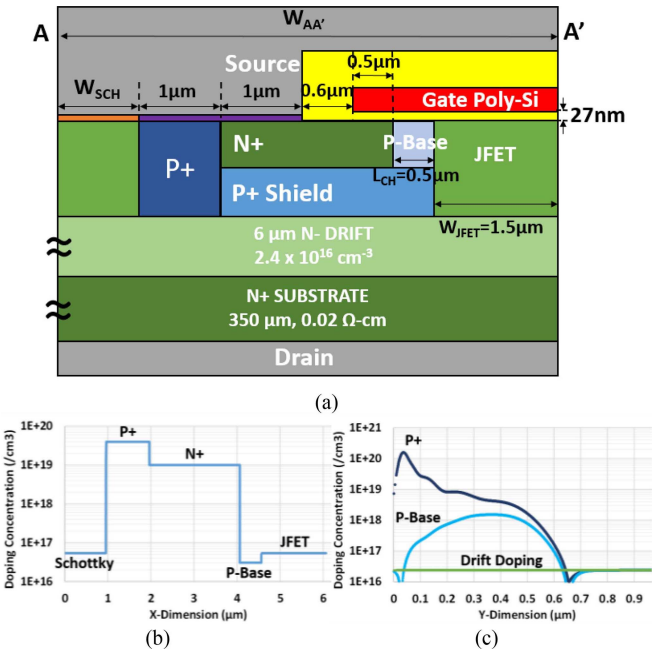

FIGURE 1. **(a) Cross-section of the 650 V, inversion-channel, JBSFETs (b) Doping profile along a horizontal cutline parallel to AA' below the gate region (c) Doping profile along a vertical cutline through the P-Base and P+ regions.**

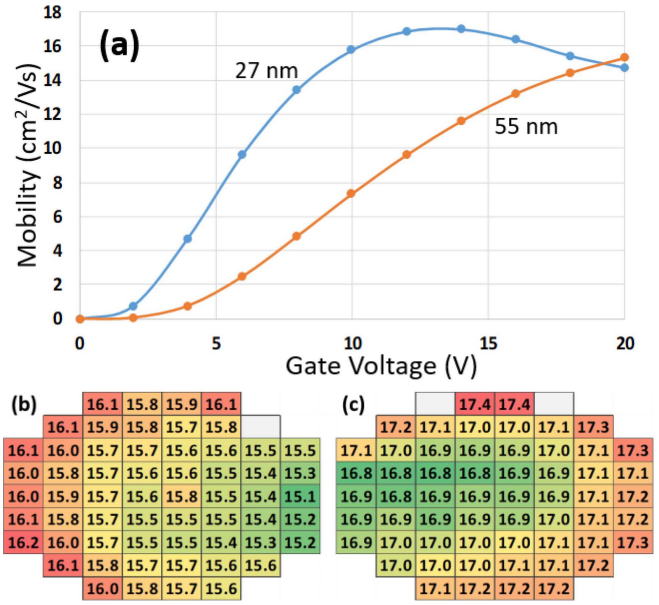

FIGURE 2. **(a) Inversion-layer mobility measured using FATFET test structure for the 27 nm and 55 nm gate oxide thickness cases at drain bias of 0.1 V, (b) measured mobility for 60 test structures on the wafer for 55 nm gate oxide at V_{gs} of 20 V (c) measured mobility for 60 test structures on the wafer for 27 nm gate oxide at V_{gs} of 15 V.**

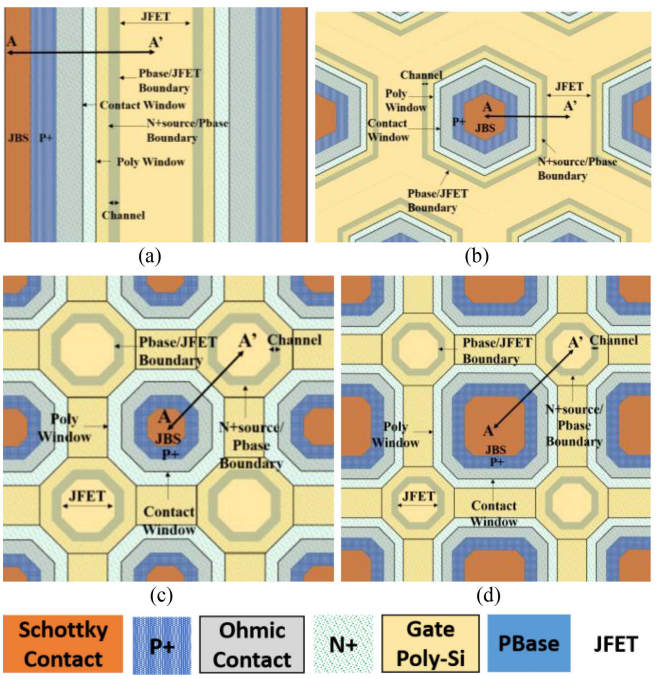

FIGURE 3. **Layout designs for the four 650 V JBSFET cell designs: (a) Linear with W_{SCH} = 1 μm; (b) Hexagonal with W_{SCH} = 1.5 μm; (c) Octagonal with W_{SCH} = 1.1 μm; (d) Octagonal with W_{SCH} = 2.8 μm. Boundaries for the various regions are labelled for each case. The greenish-grey regions delineate the channel portion. Orange regions are the Schottky contact area.**

The P-base surface concentration was optimized to obtain a threshold voltage of 2-2.5 V with the reduced gate oxide thickness of 27 nm. The gate oxide was thermally grown followed by NO annealing to improve channel mobility. The oxide thickness was measured using an MOS capacitor test element located on the wafers.

The inversion-channel mobility, measured using a FATFET structure included with the manufactured devices at drain bias of 0.1 V, for the 27 nm gate oxide case can be compared with the previously used 55 nm gate oxide case in Fig. 2(a). The on-resistance of a power MOSFET is determined by the channel mobility at the gate drive voltage. From the measured data, it can be seen that the inversion-layer mobility peaks at a value of 17 cm^2/V-s at a gate bias of 15 V for the 27 nm gate oxide case, which is slightly better than a value of 15.5 cm^2/V-s at a gate bias of 20 V measured for the 55 nm gate oxide case. This result minimizes the channel resistance contribution even with a reduced gate bias of 15 V for the 27 nm gate oxide thickness. However, the mobility values are very close at the same gate oxide electric field for both oxide thicknesses. Fig. 2(b) shows the measured channel mobility wafer-maps for the 55 nm gate oxide at a gate bias of 20 V and 27 nm gate oxide case at gate bias of 15 V. The values are uniform across the wafer.

The three types of cell topologies (Linear, Hexagonal, Octagonal) for 650 V SiC JBSFETs examined in this study are illustrated in Fig. 3. Two design variations for the Octagonal case were included for comparison. The cross-section shown in Fig. 1 is applicable for all of these topologies along the line A-A' marked in Fig. 3 for each case. The same channel length (0.5 µm) was obtained for all the devices by designing the mask boundaries for the P^+ shielding region (also the edge for the P-base region) and N^+ source region. The most commonly used cell topology

TABLE 1. 650 V JBSFET cell design information.

	Linear	Hexagonal	Oct_A	Oct_B
$W_{A\text{-}A'}$ [μm]	6.1	6.6	5.9	7.6
W_{SCH} [μm]	1.0	1.5	1.1	2.8
Channel Density [μm^{-1}]	0.164	0.211	0.193	0.116
JFET Density	0.246	0.403	0.109	0.065
JBS Diode Density	0.164	0.052	0.054	0.167
Schottky Area [cm^2]	0.00738	0.00234	0.00243	0.007515
MOSFET Area [cm^2]	0.03762	0.04266	0.04257	0.037485
JFET Area [cm^2]	0.01107	0.01814	0.00491	0.002925
Gate Poly-Si Area [cm^2]	0.0185	0.0276	0.0226	0.0175
Gate Overlap Area [cm^2]	0.0074	0.01097	0.0177	0.0145
# Cells	172	29822	65637	39452
Cell Area [cm^2]	$2.62x10^{-4}$	$1.51x10^{-6}$	$6.86x10^{-7}$	$1.14x10^{-6}$

TABLE 2. 650 V JBSFET static parameter data.

	Linear	Hexagonal	Oct_A	Oct_B
$R_{on,sp}$* [avg] (mΩ-cm^2)	6.4	5.3	6.9	10.5
$R_{on,sp}$* [best] (mΩ-cm^2)	4.7	4.7	6.3	9.3
V_{th} @1mA (V)	2.1	2.1	2.3	2.5
3rd Quadrant V_f @10A (V)	2.1	2.5	2.5	2.1
BV [avg] @100μA (V)	820	715	850	790

*$R_{on,sp}$ measured at I_d=1 A, V_{gs}=15 V, includes $R_{sub,sp}$ (~0.7 mΩ-cm^2)

is the Linear case with the Schottky contact formed along the length of the Linear cells. In the Hexagonal cell, the Schottky contact is placed in the middle of the Hexagonal opening in the polysilicon gate electrode. For the Octagonal cell topology, the Schottky contact is located in the polysilicon window between the Octagonal shaped polysilicon gates. A larger Schottky contact width W_{SCH} of 2.8 μm was used in the Oct_B cell design to reduce the JBS diode on-state voltage drop in the third quadrant. However, this design reduces the channel density resulting in a larger specific on-resistance for the JBSFET and it increases the leakage current due to larger W_{SCH}.

The width of the Schottky contact within the JBSFET cell design alters the cell pitch. This dimension impacts not only the specific on-resistance but also the gate-drain capacitance and gate-charge. The channel and JFET density are useful parameters when analyzing these electrical characteristics. The channel density (width of channel in μm per μm^2 of cell area) and the JFET density (ratio of JFET region area to cell area) can be compared for the different cell designs using Table 1. The Hexagonal and Oct_A cell designs have 1.29× and 1.18× larger channel density than the Linear cell. The Oct_B cell has smaller channel density by a factor of 0.71×. The JFET density for the Hexagonal cell design is 1.64× larger than the Linear cell design. In contrast, the Oct_A and Oct_B cell designs have JFET density of 0.44× and 0.26× of the Linear cell case. The JBS diode density (the Schottky contact area divided by the cell area) is also provided in Table 1. The JBS diode density for the Hexagonal cell design is 0.32× of the Linear cell case. The JBS diode density for the Oct_A and Oct_B cell designs are 0.33× and 1.02× of the Linear cell. Total Schottky, MOSFET, JFET and gate poly-Si areas are also given for each cell type. Gate overlap area given in Table 1 is the total area where the gate poly-Si overlaps with N^+ or P-base. Number of cells in the active area and area of each cell is also given in Table 1 for all cell designs. Note that each linear cell extends along the entire width of the active area. These differences will be used in Section V to understand the measured results for the different cell topologies.

III. MEASUREMENT PROCEDURE

The 650 V SiC JBSFETs with different cell topologies were measured on the 6 inch wafer using a semi-automated Signatone probe station. A multi-prong high current probe was used to contact the source pad on the devices with a separate Kelvin probe to remove the contributions from the long wires connected to the test equipment. A Keysight B1505A curve tracer was used to obtain the breakdown voltage at a typical current of 100 μA used in SiC power MOSFET datasheets. The blocking i-v characteristics were measured to obtain the leakage current. The on-resistance was measured using a gate bias of 15 V due to the reduced gate oxide thickness. The threshold voltage was obtained at a drain current of 1 mA from the transfer characteristics with drain bias of 0.1 V. In addition, the input, output, and gate-drain capacitances were measured up to a drain bias of 400 V. The gate charge characteristics were acquired using gate drive voltage of 15 V, a drain current of 10 A, and drain voltage of 300 V as a measure of switching performance. Unlike the previous publications on 650 V JBSFETs, statistical distributions of key device parameters were obtained using 60 devices for each cell topology. The average value for the measured characteristic and its best value are reported for each cell topology in the next section.

IV. MEASURED DEVICE CHARACTERISTICS

The typical measured device characteristics for the 650 V SiC JBSFETs with different cell topologies are compared in this section. The average values based on the statistical data for the static parameters are given in Table 2. The best values are also provided in the table because they are often reported in previous publications. The parameters relevant for switching performance are provided in Table 3.

A. BLOCKING CHARACTERISTICS

The typical SiC JBSFET blocking characteristics are shown in Fig. 4 for the four cell designs. The baseline, commonly used Linear cell design has a breakdown voltage of 820 V. It is worth noting that the leakage current for this case begins to increase at about 260 V. The Hexagonal cell topology

TABLE 3. 650 V JBSFET dynamic parameter data.

	Linear	Hexagonal	Oct_A	Oct_B
$C_{iss,sp}$ @400V (nF/cm^2)	26.8	29.0	51.8	46.0
$C_{oss,sp}$ @400V (nF/cm^2)	2.20	2.20	2.22	2.24
$C_{rss,sp}$ @400V (nF/cm^2)	0.32	0.65	0.11	0.07
$Q_{gd,sp}$ (nC/cm^2)	333	667	178	156
$Q_{g,sp}$ @ V_g=15V (nC/cm^2)	978	1600	1078	911

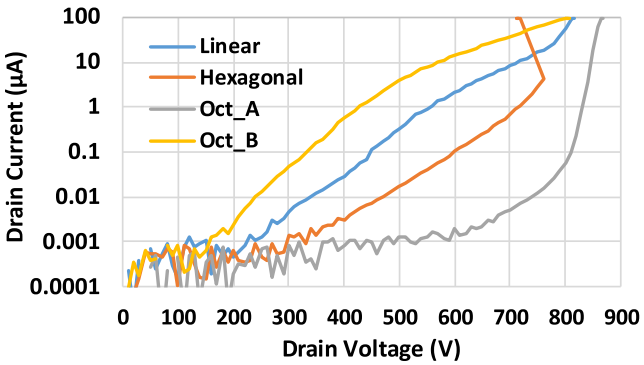

FIGURE 4. SiC JBSFET blocking characteristics measured for the four cell designs with zero gate bias.

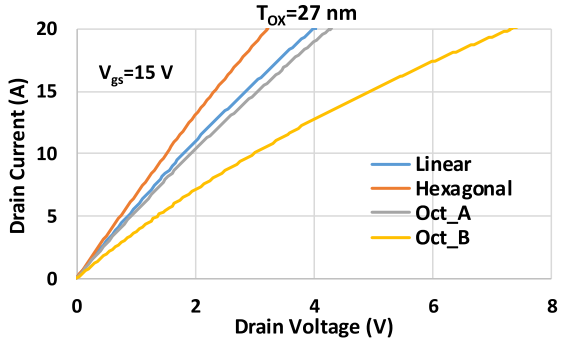

FIGURE 5. SiC JBSFET on-state characteristics measured for the 650 V devices with various cell designs at 15 V gate bias.

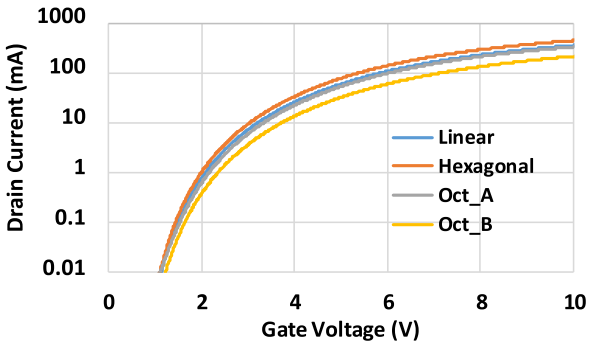

FIGURE 6. SiC JBSFET transfer characteristics measured using drain bias of 0.1 V for the four cell designs.

exhibits a snap back in its blocking characteristics with breakdown voltage of 715 V. In this case, the leakage current begins to increase at about 320 V. The Octagonal cell design Oct_A has the best blocking characteristics with a breakdown voltage of 850 V. Its leakage current remains very low with values below 10 nA at 650 V. The Octagonal cell Oct_B has a breakdown voltage of 790 V and its leakage current begins to increases at 200 V. It can be seen that all the cell topologies meet the criterion of supporting 650 V. The differences in the leakage current behavior for the different cell topologies are discussed n Section V.

B. ON-STATE CHARACTERISTICS

The measured on-state i-v characteristics for the 650 V SiC JBSFETs with the four cell designs are shown in Fig. 5 up to a drain current of 20 A. They were obtained using a gate bias of 15 V due to the reduced 27 nm gate oxide thickness; unlike in previous papers that used a 20 V gate drive in the on-state for devices with 50 nm gate oxide thickness.

The specific on-resistance was extracted from the measured i-v characteristics at a current of 1 A (current density of 22 A/cm^2). A similar current density was employed when reporting data on 650 V JBSFETs in a recent paper [23]. The average specific on-resistance for the Linear cell case was 6.4 mΩ-cm^2 with a value of 4.7 mΩ-cm^2 measured for the best case. For the Hexagonal cell design, the average specific on-resistance was 5.3 mΩ-cm^2 with a best value of 4.7 mΩ-cm^2. The Octagonal cell design Oct_A had values of 6.9 mΩ-cm^2 and 6.3 mΩ-cm^2 for the average and best values. The average and best values of specific on-resistance for the Octagonal Oct_B cell design were 10.5 mΩ-cm^2 and 9.3 mΩ-cm^2.

The lowest specific on-resistance is observed for the Hexagonal cell design and the largest value for the Octagonal Oct_B cell design. These differences will be discussed in Section V and compared with values reported in previous publications.

C. THRESHOLD VOLTAGE

The transfer characteristics measured for the four cell designs are shown in Fig. 6. All the cell topologies have similar transfer curves due to the same channel length and gate oxide thickness. The measured threshold voltage is about 2 V. Small difference in its value are due to unequal channel density for the four cell designs.

D. DEVICE CAPACITANCES

The magnitudes of the SiC JBSFET capacitances for the different cell designs can be used to assess their relative switching performance. The input, output, and reverse-transfer (gate-drain) capacitances measured for the four cases are shown in Fig. 7 as a function of drain bias up to 400 V.

The largest input capacitances are observed for the Octagonal cell cases due to extra capacitance produced by the polysilicon bars used to interconnect the polysilicon gate regions. The smallest input capacitance is measured for

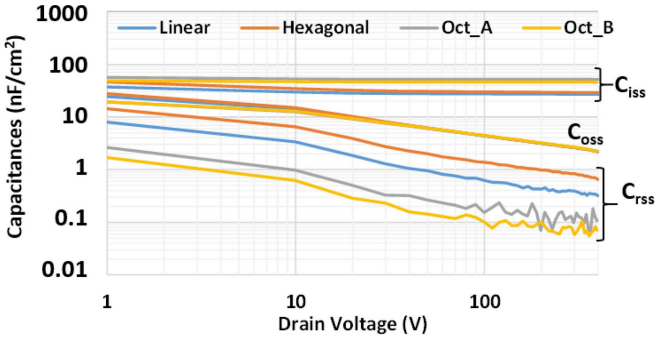

FIGURE 7. SiC JBSFET capacitances (C_{iss}, C_{oss}, and C_{rss}) for the four cell designs measured at 100 kHz.

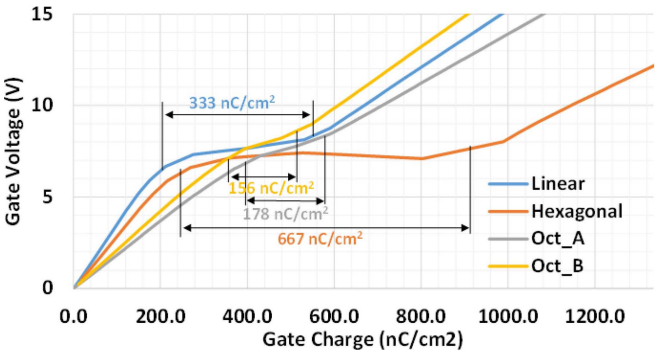

FIGURE 8. SiC JBSFET gate charge waveforms measured @V_{ds} = 400 V, I_d = 10 A for the four cell designs.

the Linear cell design. The input capacitances increase as expected with increasing gate overlap area given in Table 1. The output capacitances for all four cell designs are nearly identical. This is due to a similar junction area across the same active area for all the devices. A significant difference is observed for the reverse-transfer capacitances for the different cell designs. The smallest values are observed for the Octagonal cell topologies and the largest values for the Hexagonal cell topologies. In comparison with the Octagonal Oct_A cell design, the C_{rss} for the Linear cell and Hexagonal cell designs are a factor of 3× and 6× larger. A larger value for C_{rss} extends the drain voltage transient time during turn-on and turn-off switching events producing greater power losses. The low values for C_{rss} achieved for the 650 V JBSFETs with the Octagonal cell topology are beneficial for their use in high frequency applications.

E. GATE CHARGE

The gate voltage exhibits a plateau during turn-on and turn-off transients in typical hard-switching inverter circuits with inductive loads. The drain voltage undergoes a large excursion between the on-state and DC supply values during the gate voltage plateau [26]. The switching energy loss is mainly determined by the power loss during this transient. Power MOSFET datasheets provide the gate charge waveform as a measure of switching performance. The total gate charge (Q_g) required to reach the applied gate drive voltage is used as a measure of gate drive requirements for

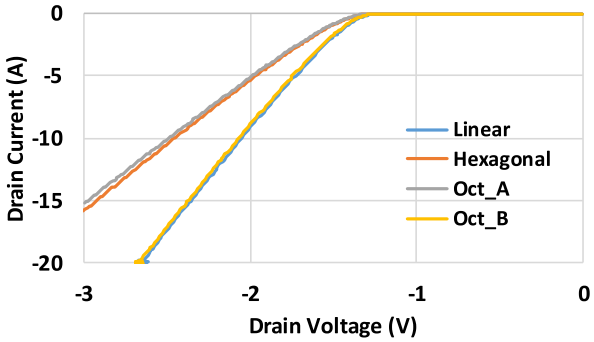

FIGURE 9. SiC JBSFET third quadrant characteristics for the four cell designs.

power MOSFETs. The gate-drain charge (Q_{gd}) defined by the duration of the gate voltage plateau is used as a measure of switching losses.

Gate charge waveforms for the 650 V JBSFETs with four cell designs are shown in Fig. 8. The waveform for the Linear cell case has the typical appearance for power MOSFETs with Q_g = 978 nC/cm^2 and Q_{gd} = 333 nC/cm^2. A much larger plateau period is evident for the Hexagonal cell design in Fig. 8 with Q_g = 1600 nC/cm^2 and Q_{gd} = 667 nC/cm^2. The Octagonal cell designs exhibit very small plateau periods. A Q_g = 1078 nC/cm^2 and Q_{gd} = 178 nC/cm^2 was extracted from the measured waveform for the Oct_A design; and Q_g = 911 nC/cm^2 and Q_{gd} = 156 nC/cm^2 for the Oct_B cell design. The measured values for Q_{gd} for the Octagonal cell designs are about 2× and 4× smaller than for the Linear and Hexagonal cell cases, respectively. The impact of this on overall device performance will be discussed in Section V.

F. THIRD QUADRANT CHARACTERISTICS

The SiC JBSFET was created to allow current flow in the third quadrant via an integrated JBS diode to prevent activation of the P-N body-diode within the power MOSFET structure [18]. In order to achieve this outcome, the area of the Schottky contact within the cells must be sufficiently large so that the voltage drop is less than 3 V in the third quadrant when carrying typical rated current levels.

The third quadrant i-v characteristics for the 650 V JBSFET with the four cell designs are shown in Fig. 9. The on-state voltage drop for the baseline Linear cell design is 2.1 V @ 10 A (222 A/cm^2), which is well below the level required to prevent body-diode activation. The Hexagonal cell design has an on-state voltage drop of 2.5 V @ 10 A, which is larger than for the Linear cell but adequate to suppress the body-diode. The same third quadrant characteristic is observed for the Octagonal Oct_A cell design. The on-state voltage drop in the case of the Oct_B cell design matches that for the Linear cell case. These differences are discussed in Section V.

V. ANALYSIS AND DISCUSSION

Wafer-level measurements of the static and dynamic parameters for the 650 V JBSFETs fabricated using 27 nm

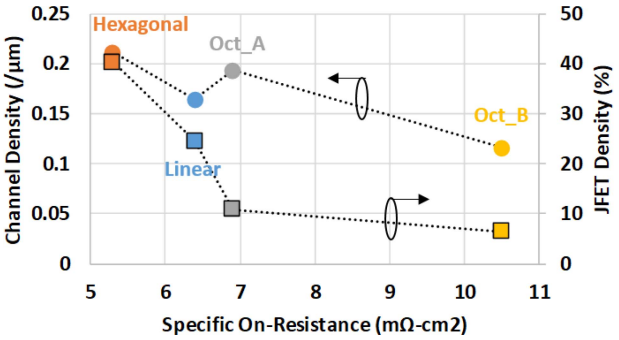

FIGURE 10. **Variation of $R_{ON,SP}$ vs. Channel and JFET Density for four cell types.**

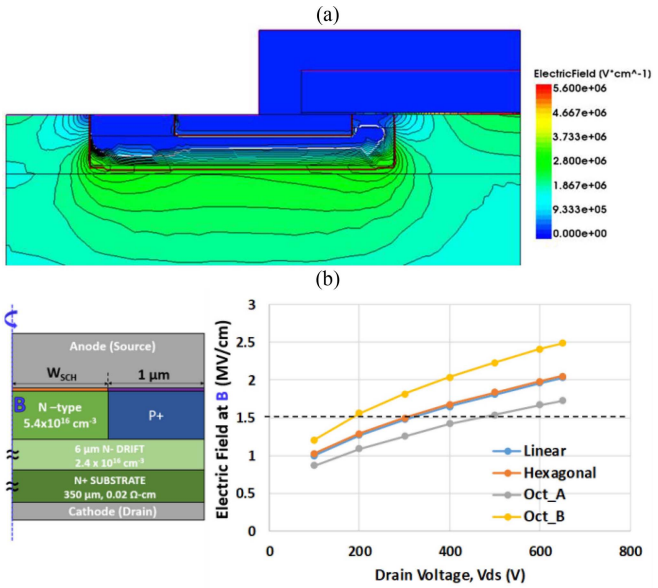

FIGURE 11. **(a) Electric field contours at 650 V for the Linear cell JBSFET; (b) Electric field increase at middle of Schottky contact with increasing drain bias for various cell designs.**

gate oxide thickness were provided in the previous section for four cell designs. The differences between the four cases are analyzed and discussed in this section. The values measured for the devices in this study are also compared with those reported in previous work on 650 V JBSFETs.

A summary of the static parameter data is provided in Table 2 for the 650 V JBSFETs with four cell designs. These values are discussed below.

A. SPECIFIC ON-RESISTANCE

The average values for the specific on-resistance for each cell design are given in Table 2. The specific on-resistance has been analytically modelled for different cell topologies [26]. From the models, the channel and JFET resistances are found to make a significant contribution in the 650 V SiC JBSFETs because the drift region resistance is very low. Fig. 10 shows a plot of average $R_{on,sp}$ against the Channel and JFET density for each cell type. Among the four cell designs fabricated in this study, the lowest specific on-resistance is observed for the Hexagonal cell case because it has large channel and JFET densities (see Table 1) when compared with other cell designs. The specific on-resistance for the Linear cell case is 1.21× larger due a lower channel and JFET density. A comparable specific on-resistance is observed for the Octagonal Oct_A cell design because its channel density is larger but its JFET density is smaller. The largest specific on-resistance is observed for the Octagonal Oct_B cell design because of its low channel and JFET density.

A specific on-resistance of 5.6 mΩ-cm^2 has been recently reported using a gate bias of 20 V for 650 V JBSFETs with the Linear cell topology [23]. These devices were fabricated using a gate oxide thickness of 50 nm. The lowest value of 4.7 mΩ-cm^2 for the Linear cell design in this work at a gate bias of 15 V is superior to the previously achieved result.

B. BLOCKING CHARACTERISTICS

The blocking characteristics of SiC power MOSFETs can be compromised by high electric field in the gate oxide in the JFET region. It has been previously demonstrated that the electric field in the 27 nm thick gate oxide SiC power MOSFETs is close to that for 55 nm thick gate oxide devices if the JFET width is properly designed and meets the reliability criterion of 3 MV/cm [13]. This electric field value is different from the electric field for reliable operation in the on-state because of band bending in the opposite directions in the two operating modes [26]. The analysis in this article is therefore focused on the electric field at the Schottky contact for the JBSFET structures.

The average breakdown voltage for all the JBSFET cell designs in this work exceed 700 V for a 650 V rated device. However, the voltage at which the leakage current begins to increase in Fig. 4 differs significantly between the cell designs. The leakage current in JBSFETs is generated at the Schottky contact and is related the magnitude of the electric field at the contact due to Schottky barrier lowering and tunneling effects [26]. The presence of the P-N junction surrounding the Schottky contact in the JBS diode structure reduces the electric field [27]. A greater degree of reduction occurs for the Hexagonal and Octagonal cell designs because of the cylindrical shape of the JBS diode structure compared with the Linear case.

A contour map of the electric field distribution obtained by 2D numerical simulations in Sentaurus TCAD is shown in Fig. 11(a) for the Linear cell JBSFET design at drain bias of 650 V. A high field concentration is observed at the corners of the P^+ shielding region in the JFET and JBS diode regions with a magnitude of about 2.8 MV/cm. It can be seen that the electric field at the Schottky contact and gate oxide is suppressed by the P^+ shielding region junction creating a potential barrier under these areas.

The increase in the magnitude of the electric field at the middle of the Schottky contact with increasing drain bias was obtained using numerical simulations for the four cell design cases and is plotted in Fig. 11(b). The JBS diode

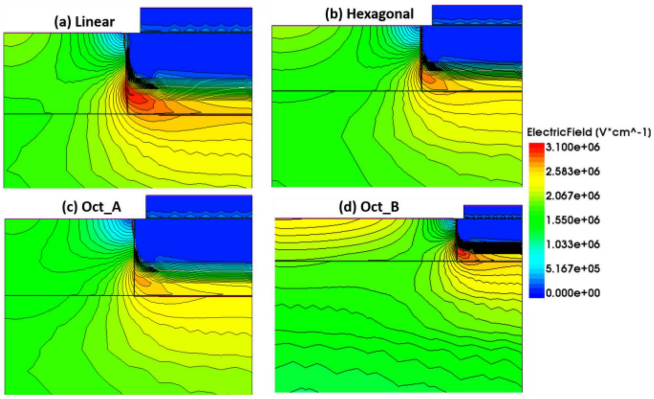

FIGURE 12. Electric field contours at 650 V for (a) the Linear cell JBS Diode, (b) the Hexagonal cell JBS Diode, (c) the Oct_A cell JBS Diode, and (d) the Oct_B cell JBS Diode.

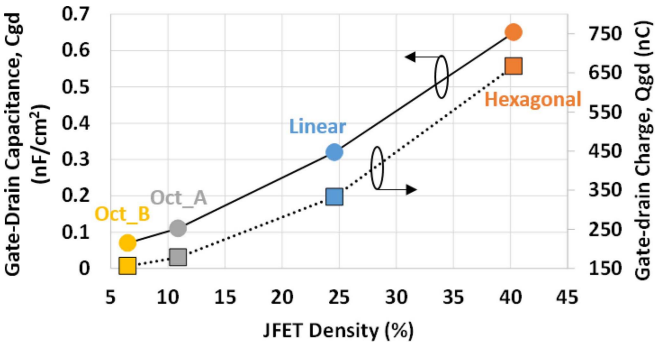

FIGURE 13. Variation of gate-drain capacitance (C_{gd}) and gate-drain charge (Q_{gd}) with JFET Density for the four cell designs.

in the Hexagonal and Octagonal cell designs was modelled using a cylindrical shape as previously described [14] using the 2D cylindrical geometry in Sentaurus TCAD where a 3D device is specified by a 2D mesh and an axis of rotation. From Fig. 11(b), it can be seen that the electric field at the Schottky contact is the largest for the Octagonal Oct_B cell case due to its large Schottky contact width of 2.8 μm despite shielding by a cylindrical junction. The next highest electric field is observed for the Linear case with its narrow Schottky width of 1.0 μm. The electric field for the Hexagonal case is close to the Linear case because of its larger Schottky width of 1.5 μm with shielding by a cylindrical junction. The lowest electric field occurs for the Octagonal Oct_A cell case due to its small Schottky contact width of 1.1 μm and shielding by a cylindrical junction. The smallest electric field occurs with reduced Schottky contact width and the cylindrical structure.

The electric field at the middle of the Schottky contact reaches a magnitude of 1.5 MV/cm (corresponding to the dashed line in Fig. 11(b)) when the drain bias reaches 200 V, 310 V, 310 V, and 500 V for the Oct_B, Linear, Hexagonal, and Oct_A cases, respectively. The leakage current begins to increase at this magnitude for the electric field in all cell design cases but at different drain bias voltages as observed in Fig. 4. The simulation results provide an explanation of the reason for the leakage current increasing rapidly at different values of the drain bias for the various cell designs.

Fig. 12 shows electric field distribution for the integrated JBS diode of each cell design at V_{ds} = 650 V. It can be observed from these plots that Oct_A cell design has the lowest electric field at the P/N junction corner followed by Hexagonal cell. This is because of stronger shielding by the P^+ region due to rotation of the JBS structure as shown in Fig. 11(b) along left axis. Linear and Oct_B structures have larger electric fields at the P/N junction due to lack of rotation and large Schottky contact width, respectively.

C. DYNAMIC PARAMETERS

A summary of the dynamic parameter data is provided in Table 3 for the 650 V JBSFETs with the four cell designs. These values are discussed below.

The measured gate-drain capacitance (@V_{ds} = 400 V) and gate-drain charge (@ V_{ds} = 300 V and I_d = 10 A) for the four cell designs are plotted in Fig. 13 against the JFET density in the cells. An excellent correlation between these dynamic parameters and the JFET density is apparent. A larger JFET density indicates more overlap area between the gate electrode and the drain (drift region) which makes the values for these parameters larger.

The gate-drain charge for the Octagonal cell designs was found to be much smaller than for the Linear case while that for the Hexagonal cell design was much larger than the Linear case. These differences are directly correlated with the JFET density provided in Table 1 as seen in Fig. 13. The JFET density for the Octagonal Oct_A cell is about 2× smaller than for the Linear case consistent with difference in measured gate-drain charge. The JFET density for the Hexagonal cell design is about 2× larger than for the Linear cell consistent with the measured data. No gate-charge data was published in the previous papers on 650 V JBSFETs [20], [23] for comparison with the results from this study.

D. THIRD QUADRANT CHARACTERISTICS

The most distinguishing feature of the SiC JBSFET structure is an integrated JBS diode for by-passing the body-diode within the MOSFET. The on-state voltage drop of the JBS diode is determined by its relative area within the device. The JBS diode density in Table 1 is a good measure of current density in the JBS diode and consequently its on-state voltage drop. A larger JBS diode density will reduce the current density at a fixed value for the current in the third quadrant.

The JBS diode density is large and equal for the Linear and Octagonal Oct_B cases. Consequently, their i-v characteristics coincide in Fig. 9. Similarly, the JBS diode density is smaller and equal for the Hexagonal and Octagonal Oct_A cases resulting in the same third quadrant i-v characteristics.

The on-state voltage drop for the JBS diodes within all the 650 V SiC JBSFET cell designs in this work falls below

TABLE 4. 650 V JBSFET figure-of-merit information.

	Linear	Hexagonal	Oct_A	Oct_B
FOM[R_{on}*C_{gd}][avg] (mΩ*pF)	2048	3445	759	735
FOM[R_{on}*C_{gd}][best] (mΩ*pF)	1504	3055	693	651
FOM[R_{on}*Q_{gd}][avg] (mΩ*nC)	2131	3535	1228	1638
FOM[R_{on}*Q_{gd}][best] (mΩ*nC)	1565	3135	1121	1451
FOM[C_{iss}/C_{rss}]	84	45	471	657

2.5 V at 10 A (222 A/cm^2), which is sufficiently low to prevent conduction via the MOSFET body-diode. In contrast, the on-state voltage drop for the JBS diodes in the JBSFETs reported in 2018 [22] was 3.2 V at 10 A (80 A/cm^2), which is too large to ensure by-passing the body-diode. The on-state voltage drop reported for the JBS diodes within the Linear cell JBSFETs in 2020 [23] was 2.6 V at 10 A (217 A/cm^2), which is slightly larger than for the Octagonal Oct_A design and much larger than for the Octagonal Oct_B design in this work.

E. DEVICE FIGURES-OF-MERIT

The products [R_{on}*C_{gd}] and [R_{on}*Q_{gd}] are commonly used figures-of-merit (FOM) for power MOSFETs because R_{on} is a measure of on-state power loss, while C_{gd} and Q_{gd} are measures of switching energy loss. These FOMs computed for the four cell designs of 650 V SiC JBSFETs with 27 nm gate oxide thickness are provided in Table 4. It can be seen that the smallest (best) FOM is obtained using the Octagonal Oct_A cell design. The average and best values for FOM[R_{on}*C_{gd}] for this case are 759 and 693 mΩ-pF. The average and best values for FOM[R_{on}*Q_{gd}] for the Octagonal Oct_A cell design are 1228 and 1121 mΩ-nC. Using the average values, the FOM[R_{on}*C_{gd}] for the Oct_A cell design is 2.7× superior to the Linear case; and its FOM[R_{on}*Q_{gd}] is 1.7× superior to the Linear case. Previous publications [20], [23] on 650 V SiC JBSFETs did not provide information on gate charge to allow comparison of the FOMs with the results of this work.

Another useful FOM for power MOSFETs is the ratio of C_{iss} to C_{rss}. A larger value for this FOM[C_{iss}/C_{rss}] provides greater immunity against shoot-through currents during operation in circuits at high frequencies with large [dV/dt] transients [26]. This FOM computed for the four cell designs is given in Table 4 for comparison. The Octagonal cell designs have very large values for this FOM, making 650 V SiC JBSFETs with this cell topology well suited for high frequency applications.

The benefits of using a thinner gate oxide for silicon power MOSFETs and IGBTs have been documented over the past 40 years and discussed in textbooks [26]. Thinner gate oxide has been shown to reduce the specific on-resistance of Si power MOSFETs and the latch-up immunity of Si IGBTs while reducing the on-state voltage drop. In this article, it has been demonstrated that a thinner oxide is beneficial to improving the performance of 650 V SiC JBSFETs as well.

VI. CONCLUSION

In this article, the performance of 650 V SiC JBSFETs with three different cell topologies has been described for the case of 27 nm gate oxide thickness for the first time. A unique attribute of these devices is operation at a gate bias of 15 V compatible with widely available Si IGBT gate drivers. The best overall performance was achieved using the Octagonal cell topology. The width of the Schottky contact within the JBSFET cell for all the cell topologies was optimized to obtain an on-state voltage drop of less than 2.6 V in the third quadrant to ensure suppression of the MOSFET body-diode. These devices, fabricated in a 6 inch commercial foundry with good parametric distributions, had excellent figures-of-merit suitable for devices used in high frequency applications.

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