High-Performance GaN Vertical *p-i-n* Diodes via Silicon Nitride Shadowed Selective-Area Growth and Optimized FGR- and JTE-Based Edge Termination

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ABSTRACT In this work, we develop highly efficient ET schemes based on a selective-area processing methodology that can effectively stymie device leakage, resulting in reliable device operation. In particular, we demonstrate plasma-assisted molecular-beam epitaxy (PAMBE) facilitated silicon nitride shadowed selective-area growth (SNS-SAG) technique, capable of producing smooth GaN interfaces and sidewalls as an enabling technology for high-performance vertical GaN power devices. SNS-SAG is shown to reduce leakage current by at least four orders of magnitude compared to a dry etched device. Floating guard ring (FGR) and junction termination extension (JTE) based ET designs for GaN *p-i-n* diodes for punchthrough operation have been simulated and analyzed in order to develop SNS-SAG compatible space-modulated junction termination extension (SM-JTE) schemes capable of achieving maximum reverse blocking efficiency $> 98\%$ while maintaining a wide doping window of up to $\sim 5 \times 10^{17} \text{cm}^{-3}$ at a minimum reverse blocking efficiency of $\sim 90\%$ extending well into high 10^{17}cm^{-3} range ($\sim 8 \times 10^{17} \text{cm}^{-3}$). In conjunction with the proposed SNS-SAG technique, SM-JTE schemes have the prospects to offer reliable GaN vertical power device operation.

INDEX TERMS Punchthrough (PT), reverse blocking efficiency, silicon nitride shadowed selective-area growth (SNS-SAG), space-modulated junction termination extension (SM-JTE).

I. INTRODUCTION

GALLIUM nitride (GaN) is a promising material in the power electronics field due to its superior properties like wider bandgap energy, E_g, higher electron mobility, μ_n, and larger critical electric field, E_c compared to already established power electronic material platforms such as silicon (Si) and silicon carbide (SiC) [1]. Availability of high-quality bulk GaN substrates has recently sparked development of fully-vertical GaN devices with high-current and large reverse blocking capabilities [2]–[7]. However, all of these devices have resulted in far lower breakdown voltage, V_{br}, than predicted by the ideal parallel-plane calculation, $V_{br,id}$. In punchthrough (PT) operation with different drift region thicknesses (t_{dr}) and drift doping concentrations (N_{dr}),

$V_{br,id}$ is given as [8]

$$V_{br,id} = E_c t_{dr} - \frac{q N_{dr} t_{dr}^2}{2 \epsilon_0 \epsilon_{GaN}}, \quad (1)$$

which is ensured if [9]

$$t_{dr} < \frac{\epsilon_0 \epsilon_{GaN} E_c}{q N_{dr}}. \quad (2)$$

Here ϵ_0 and ϵ_{GaN} refer to free-space and GaN relative permittivities, respectively. In PT operation, a thinner drift layer is used with a reduced N_{dr} value to support a large V_{br} in a fully depleted drift region in reverse blocking mode [8]. Typically, reducing N_{dr} is not easy and, instead, a thinner drift layer is used for PT operation, reducing specific
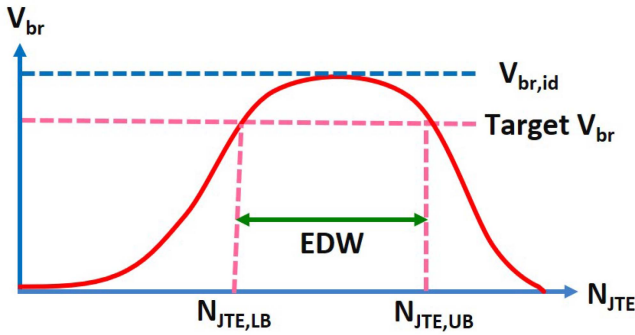
FIGURE 1. The effective doping window (EDW) for a junction termination extension (JTE) is defined here as the difference between the upper bound of the JTE doping, $N_{JTE,UB}$, and the lower bound of the JTE doping, $N_{JTE,LB}$, between which bounds the device breakdown voltage, V_{br} is greater than the target value of $\eta_{br} \times V_{br,id}$, where η_{br} and $V_{br,id}$ refer to the target reverse blocking efficiency and ideal parallel-plane breakdown voltage, respectively.

on-resistance ($R_{on,sp}$) and further increasing performance ($V_{br}^2/R_{on,sp}$). In this work, we will limit our designs to PT operation.

As an example of reverse blocking underperformance, a $30\mu m$-base PT *p-i-n* diode ($N_{dr} \sim 3\times10^{15}\text{cm}^{-3}$) reportedly demonstrated $V_{br} \approx 3.9\text{kV}$ [10]. The diode employed a bilayer single-zone junction termination extension (SZ-JTE) as the edge termination (ET) scheme [11]. Considering $E_c \sim 3.9\text{MV/cm}$ [10], from (1), we have $V_{br,id} \approx 9\text{kV}$. The resulting reverse blocking efficiency is $\eta_{br} = V_{br}/V_{br,id} \approx 43\%$. The effective critical electric field is calculated to be $E_{c,eff} \approx 2.2\text{MV/cm}$ and PT operation is maintained. While this diode demonstrates less than 50% blocking efficiency, it still demonstrates one of the highest reported values of V_{br}. This reinforces that the primary hurdle for the GaN platform is reverse blocking efficiency.

The struggle of GaN devices to achieve the material limits of efficiency is primarily explained by the lack of suitable processing methods and ET schemes. Conventional selective-area processing techniques typically consist of dry etching [i.e., inductively-coupled plasma reactive-ion etching (ICP-RIE)] and ion implantation, both of which are known to introduce lattice damage and defects generating significant device leakage. This device leakage contributes to decreasing breakdown voltage and device lifetime. Additionally, many of the conventional edge termination schemes are designed for very specific ET doping levels. In these cases, even small deviations in doping level can significantly decrease the blocking ability of the device. This makes it imperative to have a range, or effective doping window (EDW), where the dependence of blocking voltage on doping level is not significant, as is detailed in Fig. 1.

In this work, we address these issues. First, we develop and experimentally demonstrate a selective-area processing technique capable of producing high-quality, smooth, and low-leakage interfaces and sidewalls. Second, we design and analyze floating guard ring (FGR) and JTE-based

ET schemes compliant with our selective-area processing technique for fully-vertical GaN *p-i-n* diodes on bulk GaN substrates. Together, these techniques and designs can unlock the full potential of GaN power devices.

II. SELECTIVE-AREA GROWTH
A. MOTIVATION AND BACKGROUND

A power device, such as, a *p-i-n* diode with or without ET, can be conventionally fabricated via epitaxial growth followed by either ion implantation or dry etching. In general, various power devices with ET structures can be processed by using ion implantation in combination with ICP-RIE. Mg-implantation (Mg being the main *p*-type dopant in GaN) causes various defects including dopant clustering, vacancies, dislocation, and Mg diffusion along threading dislocations [12], [13]. Recently, symmetric multi-cycle rapid thermal annealing has been proposed to activate $\sim 8\%$ of the implanted Mg (up from $\sim 1\%$ typical of ion implantation) by restoring some degree of crystallinity [14]–[16]. However, not all defects can be expected to be removed by any rapid annealing process. In addition to the effects on blocking capability, ion implantation was shown to impair the forward current density seriously in SiC merged *p-i-n* Schottky barrier (MPS) diodes [17]. GaN, being hyper-prone to various native defects, is only expected to have more aggravated issues.

Dry etching (ICP-RIE) introduces similar point and line defects (e.g., vacancies) [18] contributing to sidewall leakage component [19] and higher overall leakage current contribution [5]. Therefore, both conventional processing routes result in the loss of crystallinity forming leakage pathways. Because of the crystal damage, it is inferred that the dopant activation in the damaged areas is reduced. This has been experimentally demonstrated with depletion or even inversion occurring in etch-damaged *p*-regions [20]. To appreciate the effects from this, we consider the electric field profile of a SZ-JTE structure in Fig. 2(a). In a functional SZ-JTE ET scheme, the JTE region is expected to be fully depleted so that it acts as a high-resistivity region. Consequently, the whole drift region underneath the *p*-base and the JTE is depleted to sustain a large V_{br} value in PT operation [32]. However, in a damaged *p*-base/JTE interface, a lower effective doping (N_{Dam}) causes the JTE to be loosely connected to *p*-base. In the worst case, this damaged region might even turn into an n^--region [20]. As a result of this, the long JTE region [which is $50\mu m$ long in Fig. 2(a)] fails to fully deplete, a fact also confirmed from simulations. Consequently, premature breakdown initiates in the damaged region at the lower end of *p*-base/JTE interface [Fig. 2(a)] due to the electric field crowding. To appreciate the effect of damage spot size, L_{Dam} (extent of damage on each side) and N_{Dam}, we plot η_{br} as a function of N_{Dam} for different L_{Dam} values in Fig. 2(b). Clearly, the lattice damage reduced V_{br} is quite insensitive to the exact value of N_{Dam}. For the damaged diode depicted in Fig. 2(a), $V_{br} \sim 2.4\text{kV}$, in contrast to an expected $V_{br} \sim 4.4\text{kV}$ for the undamaged diode. In addition to these effects,
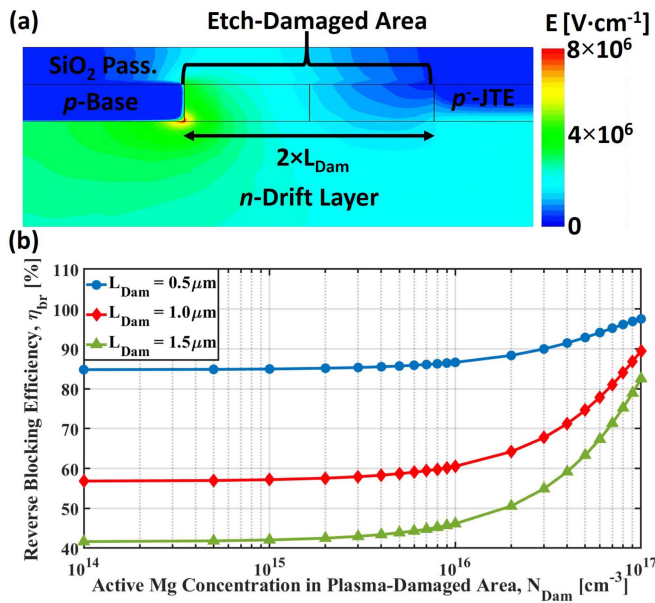
FIGURE 2. Effect of lattice damage: (a) two dimensional (2-D) simulated post-breakdown electric field profile at a reverse bias of $\sim$ 3kV and (b) plots of reverse blocking efficiency, η_{br} versus active Mg concentration in plasma-damaged *p*-regions, N_{Dam} in a single-zone junction termination extension (SZ-JTE) edge termination (ET) scheme. Premature breakdown due to the electric field crowding at the lower end of *p*-base/JTE interface is clearly visible in (a). The damage spot size, L_{Dam} is also indicated in (a). In accordance with the experimental observation [20], a lower effective dopant concentration in ICP-RIE etch-damaged *p*-regions is assumed in the simulations. The schematic diagram of SZ-JTE ET is illustrated in Fig. 14(a). We assume $N_{Dam} = 1 \times 10^{15} \mathrm{cm}^{-3}$ and $L_{Dam} = 1\mu$m for this case.

FIGURE 3. The PAMBE-SAG process from a cross-sectional schematic view [top row] and a top-down scanning electron microscope (SEM) view [bottom row] as read from the left to the right. Step # 1 is the deposition and patterning of the silicon dioxide (SiO$_2$) mask. Step # 2 is the regrowth of the GaN layers, with polycrystalline GaN (poly-GaN) forming on the mask region. Step # 3 is the mask stripping, which leaves a clean surface for further processing. Poly-GaN growth on masked region is believed to be both a result of the lower growth temperatures and the high reactivity of atomic nitrogen in the PAMBE system. The SAG layers here are $\sim$ 200nm thick with a root-mean-squared (RMS) roughness of $\sim$ 0.7nm.

concomitant defects and lattice damage in GaN [not reliably modeled in technology computer-aided design (TCAD) simulations] are expected to cause large leakage contribution, compromising the long-term device reliability. Therefore, the simulations in Figs. 2(a) and 2(b) represent a more ideal version of the true impact that conventional processing methodologies can have.

Supporting this, a bilayer SZ-JTE ET was reported to have an experimental $V_{br} \sim$ 2.6kV in contrast to a target $V_{br} \sim$ 4.7kV [11]. Hayashida *et al.* demonstrated that a larger ICP-RIE damage area ushers in a huge leakage current, lowering the effective V_{br} [5]. In experimentally demonstrated 1μm and 2μm *p*-striped merged *p-i-n* Schottky (MPS) diodes by Li *et al.* [21], the leakage current density was almost the same as that of a fabricated *p-i-n* diode, even though the TCAD simulation suggested leakage current density many orders smaller (close to the computational precision limit of the TCAD software) in the *p-i-n* diode. This suggests serious *p*-sidewall leakage, a fact also suggested and experimentally corroborated elsewhere [19].

B. METHODS

We require a selective-area processing (SAP) technique that avoids dry etching or ion implantation induced damages and defects. Our group previously reported a plasma-assisted molecular-beam epitaxy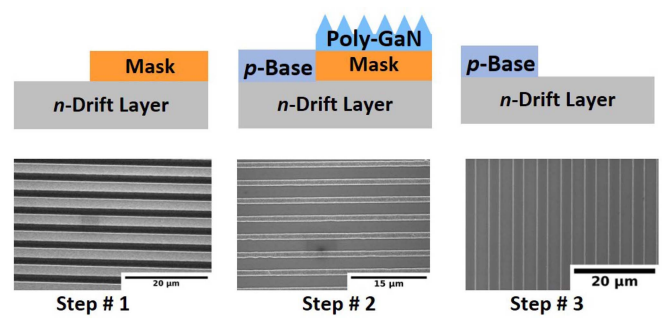 (PAMBE) enabled selective-area growth (SAG) process, or PAMBE-SAG, which bypasses both etching and implantation damages, and achieved record low *n*-type ohmic contact resistance [22]–[27]. Very recently, we demonstrated smooth *p-n* grid structures using this methodology [28], [29]. Fig. 3 shows this SAG process as a cross-sectional diagram as well as a top-down view via scanning electron microscope (SEM) imagery. The regrown areas are well defined with a thickness of $\sim$ 200nm, above which noticeable sidewall roughness begins to occur. However, many structures, including edge termination, require thicker layers.

This version of the SAG process could not be directly extended to thicker layers due to the poly-GaN that grows on the mask sidewalls. The poly-GaN will inevitably intersect with the epitaxial regions unless somehow prevented. PAMBE, being a line-of-sight restricted technique (due to the low surface diffusivity of atomic nitrogen), provides a solution. By making the sidewalls out of line-of-sight of the nitrogen plasma source, the sidewalls are "shadowed" or starved of flux, and there is no growth of poly-GaN as well as limited growth of epitaxial GaN in the intersecting region as illustrated schematically in Fig. 4(a). Clearly, the maximum amount of shadowing that could be achieved by most methods is that from a perfectly vertical mask sidewall.

However, in a real growth scenario, the substrate is rotated for the sake of uniformity and, as such, even a nearly 90° sidewall will result in a small amount of roughness as seen in Fig. 4(b). This means that to achieve total shadowing, the base of the sidewall must be removed. To achieve this, we integrated a secondary base layer of silicon nitride (SiN$_x$) beneath the original SiO$_2$ that can be selectively wet etched out via hot phosphoric acid (H$_3$PO$_4$). This allows us to produce a controllable amount of undercut in the SAG growth mask. In addition to providing this shadowing, the SiO$_2$ acts as the structural layer with its superior strength and the SiN$_x$ acts as a stress relief interlayer with a coefficient of
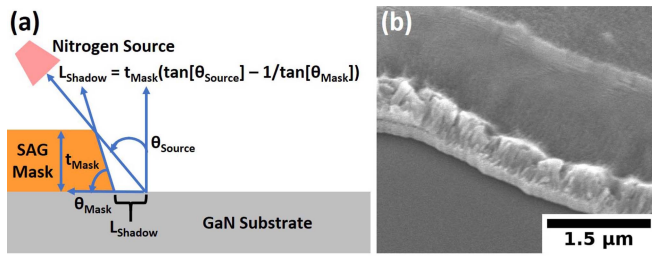
FIGURE 4. The shadowing effect in PAMBE-SAG: (a) a schematic diagram showing the geometry that creates shadowing and (b) SEM (tilted 30°) image of SAG sidewall from a fully vertical silicon dioxide mask sidewall. The roughness at the base is indicative of the intersection of the mask and epitaxial layer that is addressed by the bilayer mask.
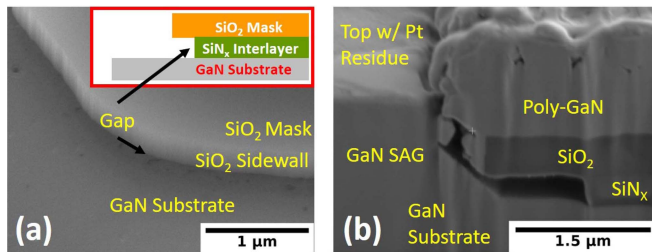

FIGURE 5. SEM images of: (a) silicon nitride shadowed SAG (SNS-SAG) mask (tilted 45°) with inset showing mask schematic and (b) cross-section of an undercut mask (the gap in the SiN$_x$ interlayer between the SiO$_2$ mask and the GaN substrate) post-growth. The cross-section in (b) is produced by focused ion-beam milling and is tilted 52° from the top surface. The mask is 1 μm in this case but can easily be made thicker. The grown layer is approximately 1.5 μm thick. The undercut mask in (b) corresponds to the gap shown in (a) and the inset therein.

thermal expansion (CTE) between that of SiO$_2$ and GaN. This method for producing selective epitaxial growth of thick ($> 1\mu$m) layers is here referred to as silicon nitride shadowed SAG (SNS-SAG).

C. RESULTS AND DISCUSSION

Both the smooth SiO$_2$ sidewall as well as the gap from the recessed SiN$_x$ interlayer post-H$_3$PO$_4$ etch can be seen in Fig. 5(a) for SNS-SAG processing. The inset shows the schematic diagram of the stack. Fig. 5(b) shows a cross section of an undercut mask post-growth. The mask on the right side of the image shows the bilayer structure with part of the SiN$_x$ interlayer (the void between the SiO$_2$ mask and the GaN substrate) etched out. Note that in this case the height of the grown mesa was larger than the mask resulting in some roughness at the top. SEM images of typical SNS-SAG grown mesas after mask stripping appears in Fig. 6(a). The root-mean-squared (RMS) roughness of the mesas is the same as the planar grown regions, being ~ 0.7nm.

To assess the efficacy of PAMBE-SAG, we fabricated two Schottky barrier diode (SBD) structures identical to the one pictured in Fig. 7(a), each using only one of the two processing techniques: ICP-RIE or SNS-SAG. To do this, a GaN ICP-RIE technique using a Ni hard mask was developed based on Zhang *et al.* [19] and Shul *et al.* [30]. The SEM image of side-by-side SNS-SAG and ICP-RIE mesas appear
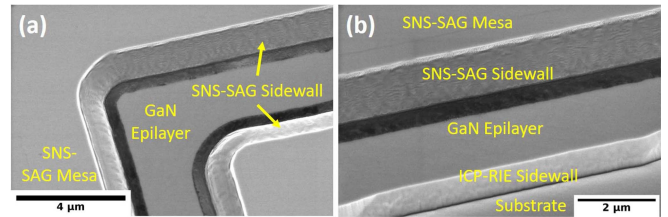

FIGURE 6. SEM (tilted 45°) images of: (a) SNS-SAG grown GaN mesa after mask stripping and (b) SNS-SAG GaN mesa with an ICE-RIE etched mesa in a tiered fashion.

in Fig. 6(b). For this demonstration, a 1.5μm-thick UID drift layer was initially grown atop a 330μm-thick bulk GaN substrate ($n > 1\times10^{18}$cm^{-3}) purchased from the SixPoint Materials. Then, half of the sample was patterned with an SNS-SAG mask while the other half was left bare. An additional 1μm was then grown on the sample. In the patterned region, this resulted in SNS-SAG mesas where growth in the bare region was planar. The planar region was then etched 1μm using the ICP-RIE technique to produce mesas parallel to the SNS-SAG mesas.

The I-V characteristics of both cases are shown in Fig. 7(b). The SNS-SAG grown SBD shows an improvement by more than four orders of magnitude in leakage current compared to its ICP-RIE counterpart, validating the fact that SNS-SAG is a promising technique leading to high-efficiency GaN power device structures. By nature, the sidewalls should have defect densities comparable to planar epitaxy. As such, the grown mesas will have minimal defects and leakage, and is, thus, suitable for the JTE- and FGR-based ET schemes discussed in the following sections. The only difference in processing the SBD structures for ICP-RIE and SNS-SAG cases is the sidewall. Therefore, the large leakage component associated with ICP-RIE processed SBDs must be attributed to the sidewall leakage component. Sugimoto *et al.* confirmed and experimentally measured this sidewall leakage current component, which Zhang *et al.* went to great lengths to target and reduce, albeit with limited success [19], [20]. This well documented sidewall leakage component arising from ICP-RIE has clearly been significantly reduced by simply using SNS-SAG instead. This leakage component is indicated in Fig. 7(a) in blue dotted arrow.

Notably, the current of the ICP-RIE processed SBD in forward direction is larger compared to that of the SNS-SAG processed SBD. The ICP-RIE and SNS-SAG diodes turn on at ~ 0.55V and ~ 0.75V, respectively. Suda *et al.* experimentally demonstrated thermionic field emission (TFE) rather than thermionic emission (TE) as the tunneling mechanism in GaN SBDs [31]. The reduction in diode turn-on voltage for the ICP-RIE case is, thus, speculated to be due to TFE and the overlap of the Schottky anode electrode with etch-damaged area. The larger current before turn-on reinforces this as higher leakage through the Schottky contact signifies a reduced Schottky barrier. This continues through the
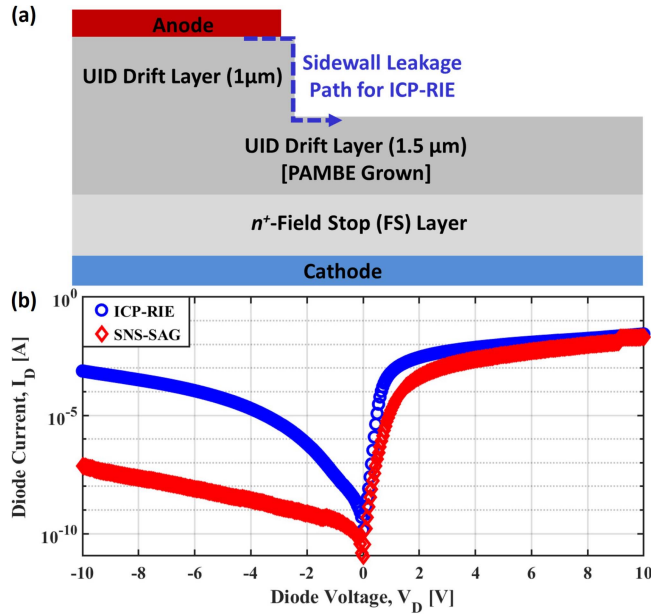
(a)

(b)

FIGURE 7. Schottky barrier diode (SBD): (a) schematic diagram of the device half-structure and (b) comparison of experimental I-V characteristics for devices processed using ICP-RIE or SNS-SAG. In (b), the device structure [shown in (a)] is identical for both ICP-RIE and SNS-SAG. The top 1 μm-thick UID drift layer in (a) is processed using either ICP-RIE or SNS-SAG. The ICP-RIE sidewall leakage path is also shown in (a).

FIGURE 8. Schematic diagram of the core *p-i-n* diode half-structure, serving as base for ET schemes in this work.

forward-bias and contributes to larger forward current initially. However, clearly the SNS-SAG processed SBD catches up with ICP-RIE processed SBD and implies a lower $R_{on,sp}$. This larger leakage through Schottky contacts can be a factor in dampening bipolar surge current strength in a GaN MPS diode, for example. This preliminary demonstration, while meant to be predominantly comparative, clearly showcases the benefits of using SNS-SAG to minimize defect density.

III. SPACE-MODULATED JTES
A. MOTIVATION AND BACKGROUND

Edge termination greatly impacts device performance in the reverse blocking mode. Without it, V_{br} will always be significantly below $V_{br,id}$. However, with optimized ET, V_{br} can come within a few percent of $V_{br,id}$. In a JTE for example, this optimization process typically involves choosing a very specific ET doping concentration, N_{JTE}. In practice, it can be very difficult to reliably obtain the optimum value of N_{JTE} and therefore V_{br}. First, the degree of precision achievable in epitaxial growth or implantation for the ET may be limited. For example, SZ-JTE ET scheme proposed by Wierer *et al.* [32] resulted in a very narrow centroid-shaped V_{br} characteristic as a function of net SZ-JTE doping, N_{JTE}. Second, due to the presence of surface charges [33], this characteristic is modified sometimes unpredictably along with the optimum value of V_{br}. By choosing a minimum desired η_{br}, we can consider an effective doping window (EDW) where deviations from the optimum N_{JTE} do not significantly reduce V_{br} [*vide* Fig. 1].
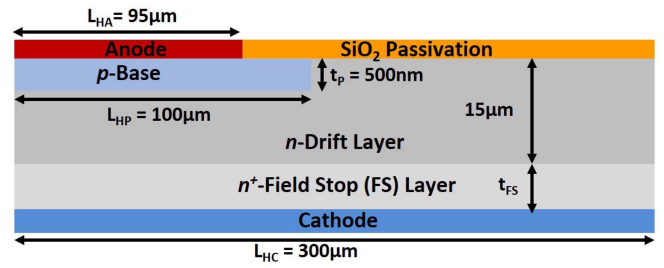
Increasing the JTE thickness can widen the EDW [32]. However, this is a small improvement and can be problematic in terms of processing. The multi-zone (MZ-JTE) ET scheme offers a solution to this problem by helping widen the EDW to some extent, but it comes at the expense of increased processing steps and, more significantly, with the requirement of very precise control in the ratio of the net doping concentrations in various JTE regions for optimum operation [33]. Another important issue is the value of the lower bound of the EDW, $N_{JTE,LB}$ [defined in Fig. 1]. In metal-organic chemical-vapor deposition (MOCVD) grown UID GaN layers, $N_{dr,UID} \sim 1$–2×10^{16}cm^{-3} [4], [34], [35]. This was also found to be true even for PAMBE samples [28], [29], though lower values can be achieved via compensation doping [36], [37]. Therefore, it is desirable that $N_{JTE,LB}$ be as far away from $N_{dr,UID}$ as possible, i.e., $N_{JTE,LB} \geq 1.5 \times 10^{17}$cm^{-3} while maintaining a large EDW for practicality to ensure the JTE is of *p*-type.

In the following sections, we gradually develop ET schemes that address the following design targets: (1) compatibility with SNS-SAG processing to ensure low-leakage and reliable operation, (2) simplicity in SNS-SAG processing (fewer SAG mask steps), (3) $N_{JTE,LB} \geq 1.5 \times 10^{17}$cm^{-3} to avoid JTE layer accidentally being *n*-doped, (4) EDW $\geq 4 \times 10^{17}$cm^{-3} for $\eta_{br} \sim 80\%$ to ensure a reasonable reverse blocking efficiency in the worst-case processing deviation, (5) EDW $\geq 1.5 \times 10^{17}$cm^{-3} for $\eta_{br} \sim 90\%$ (i.e., $V_{br} \sim 4$kV for a thin drift layer for PT operation), and (6) reduction in electric field crowding at critical points to avoid premature breakdown and other associated nonidealities.

B. METHODS

The design proceeds with the two dimensional (2-D) simulation performed by TCAD tool [38]. The core *p-i-n* diode half-structure for simulation is shown in Fig. 8 with various dimensions mentioned therein. The *p*-base net doping concentration (N_{p-Base}), N_{dr}, and the field stop (FS) doping concentration (N_{FS}) are 1×10^{19}cm^{-3}, 5×10^{15}cm^{-3}, and 1×10^{19}cm^{-3}, respectively. The impact ionization rates at an electric field, E can be calculated using the Chynoweth equation as [39]

$$\alpha_{n,p} = A_{n,p} \exp\left(-\frac{B_{n,p}}{E}\right), \qquad (3)$$

TABLE 1. Various parameters used in TCAD simulations.

Symbol	Value	Reference(s)
E_g	3.437eV	[32]
$m_{n,p}$	0.2, 1.25	[40]
ϵ_{GaN}	9.0	[32]
$A_{n,p}$	$3.1 \times 10^7 \text{cm}^{-1}$, $3.1 \times 10^7 \text{cm}^{-1}$	[11]
$B_{n,p}$	$3.5 \times 10^7 \text{V/cm}$, $3.5 \times 10^7 \text{V/cm}$	[11]
$E_{D,A}$	17meV, 180meV	[40], [32]
$g_{c,v}$	2, 4	[32], [40]
J_{br}	$1 \mu\text{A/cm}^2$	— —
T_{Amb}	27°C	— —

Here $m_{n,p}$ are the electron and hole effective masses, $E_{D,A}$ are the donor (Si) and acceptor (Mg) impurity levels, $g_{c,v}$ are the donor and acceptor degeneracies, J_{br} is the threshold cathode current density for breakdown, and T_{Amb} is the ambient temperature.

FIGURE 9. Schematic diagram of a SZ-JTE scheme aided by SM-FGRs [top] and spatial modulation of average Mg concentration (after [42]) [bottom]. In the device structure, *p*-type SM-FGRs are embedded in the JTE and have the same doping concentration as the *p*-base. The p^--JTE doping concentration is lower than that of SM-FGRs.

where $A_{n,p}$ and $B_{n,p}$ are the impact ionization parameters for electrons and holes, respectively. The simulation parameters are listed in Table 1. From simulations, the unterminated device in Fig. 8 results in V_{br} values of $\sim$ 972V and $\sim$ 978V for t_{FS} values of $0.5\mu\text{m}$ and $375\mu\text{m}$ (thicker FS layer – a more realistic situation), respectively. Therefore, t_{FS} does not have much impact on the simulation. To reduce the computational time, we will, hereafter, adhere to $t_{FS} = 0.5\mu\text{m}$. To find $V_{br,id}$, we simulate a structure where the *p*-base is infinitely long, giving $V_{br,id} \sim 4.43\text{kV}$. Using (2), this structure in ideal case should operate in PT mode. However, we have to be cautious in applying (1) for the core diode. Eq. (1) was derived assuming a planar *p-n* junction where the *p*-base is infinitely long, unlike the structure in Fig. 8. At the onset of breakdown, both the horizontal and vertical *p-n* junctions in the core diode contribute to avalanche runaway. Therefore, we find V_{br} for t_{dr} values of both $14.5\mu\text{m}$ and $15\mu\text{m}$ and average it out to obtain $V_{br,id} \sim 4.44\text{kV}$. This indicates the accuracy of our simulation setup.

C. RESULTS AND DISCUSSION

The SZ-JTE overall fails to achieve a reasonably wide EDW, and FGRs suffer from instabilities caused by high surface electric field and surface charges that may change the surface potential and create conductive paths on the drift layer between rings [41]. However, their combinations [SZ-JTE structures aided by equidistant FGRs] have been successfully used in SiC *p-i-n* diodes [41]. We have explored both SZ-JTE and double-zone JTE (DZ-JTE) schemes aided by equidistant FGRs and space-modulated FGRs (SM-FGRs). The schematic of a SZ-JTE structure aided by SM-FGRs is illustrated in Fig. 9. The concept of spatial modulation of average Mg concentration, $N_{Mg,Avg}$, is illustrated to create an equivalence of MZ-JTE with a much simpler process. The simplicity is attributable to the fact that it is much more reliable to modulate physical spacing than doping concentrations. The quantity $N_{Mg,Avg}$ can then be changed by varying the space modulation factor for the *i*-th FGR, defined as [42]

$$a_{FGR,i} = \frac{L_{FGR,i}}{L_{FGR,i} + L_{Gap,i}} = \frac{L_{FGR,i}}{L_{Period}}, \quad (4)$$
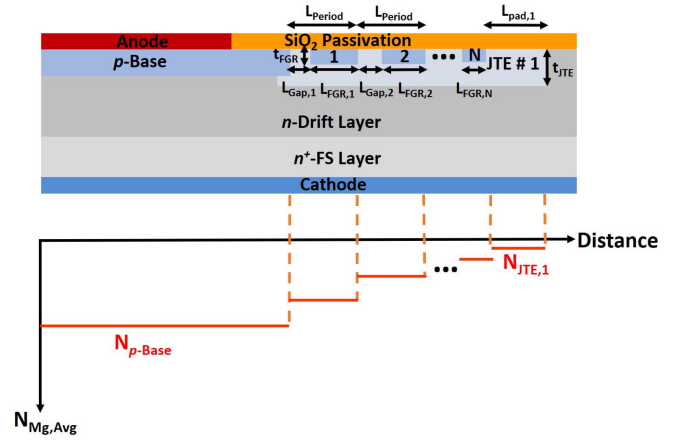
where $L_{FGR,i}$ and $L_{Gap,i}$ are the width of the *i*-th FGR and the gap to the left of it, respectively. The length, L_{Period} is kept constant for all the FGRs.

For the sake of brevity, the details (i.e., ET geometry and numerical results) of this exploration are omitted but rather the important conclusions motivating this section are included. SZ-JTEs with space-modulated FGRs are superior to those with equidistant FGRs with the spatial modulation widening the EDW curve. However, another important feature of SZ-JTE schemes aided by FGRs is that the extension of the doping window is to the left which is contrary to the requirement [higher $N_{JTE,LB}$, target (3) in Section III-A] stipulated earlier. In fact, $N_{JTE,UB}$ decreases with the addition of the FGRs. Switching to DZ-JTE designs, the additional JTE zone will, of course, widen the EDW, which is desired. However, once again most of the benefit of the FGRs is lost due to the EDW widening being in the direction of lower doping concentrations.

To explain the working principle of JTE scheme aided by FGRs, we consider the electric field profiles for SZ-JTE scheme and the SZ-JTE scheme aided by SM-FGRs in Fig. 10. The SZ-JTE scheme aided by SM-FGRs reduces the electric field by $\sim$ 40% at the *p*-base/JTE interface by distributing the electric field crowding over a larger space by virtue of the FGRs. However, the electric field crowding at the JTE end remains largely unchanged. This demonstrates why the FGRs help boost V_{br} at lower values of Mg concentration in JTE and can decrease it at higher values of Mg concentration in JTE. For lower Mg-concentrations, the bulk of the electric field is crowded near the *p*-base/JTE interface, increasing the effectiveness of the FGR field dispersion. For higher values of Mg-concentrations, the highest electric field spike shifts to the JTE end. This makes the FGRs ineffective with their presence actually raising the average Mg-concentration making the junction effectively more abrupt than in the ideal case.
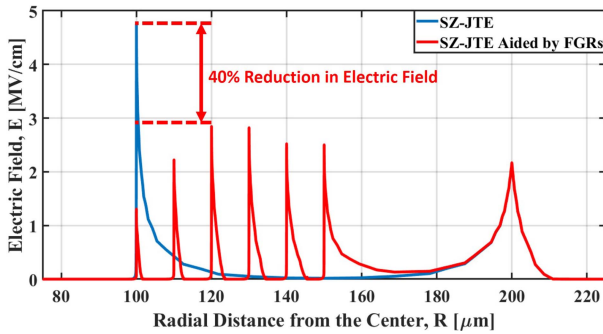
FIGURE 10. Simulated 2-D electric field profiles for SZ-JTE scheme and a variant of SZ-JTE scheme aided by SM-FGRs ($N_{JTE,1} = 1 \times 10^{17} cm^{-3}$) at the SiO$_2$/JTE interface at a reverse bias of $\sim$ 4kV. For fair comparison, $L_{JTE,1} = 100\mu m$ and $t_{JTE} = 1\mu m$ have been used for the SZ-JTE scheme. This SZ-JTE scheme aided by SM-FGRs variant involves five rings with $a_{FGR,i}$ decreasing from 0.85 to 0.45 and $L_{Period} = 10\mu m$.

From this behavior in Fig. 10, we, therefore, consider FGRs terminating the JTE region [embedded in the drift region], rather than FGRs embedded in the JTE as shown in Fig. 9, in order to relieve the field crowding at the JTE end and increase upper EDW bound, $N_{JTE,UB}$. The JTE structures, when used with the SM-FGRs as the extension, are called space-modulated JTEs (SM-JTEs). This ET scheme spatially modulates the average Mg-concentration by varying the widths of FGRs in a manner very similar to the one illustrated earlier in Fig. 9. The schematic diagram of the SM-JTE ET scheme and various relevant dimensions are shown in Fig. 11(a). The advantages of SM-JTE schemes compared to other schemes include widening the EDW, increasing $N_{JTE,LB}$, and simplifying processing via SNS-SAG technique quite significantly compared to that for JTE schemes aided by FGRs.

A larger EDW is directly related to a more gradual change in spatial modulation, which in turn is dependent on values of L_{Period} and $L_{Gap,1}$ (the innermost and smallest $L_{Gap,i}$). However, from a device processing standpoint, $L_{Gap,1}$ cannot be made unrealistically small. To ensure both that the values of $L_{Gap,1}$ are practical and that the modulation in $N_{Mg,Avg}$ is gradual, we want L_{Period} to be as large as possible [please refer to Figs. 11(a) and (4)]. However, the size of L_{Period} is, in turn, limited by N_{dr} to a large extent as follows.

Because of the high UID-concentration in GaN, the lowest reported value of N_{dr} has been $\sim 2 \times 10^{15} cm^{-3}$ [43], about an order larger than those reported for SiC diodes [42], [44]–[48]. This means that to maintain PT operation, we are forced to use a thin drift layer [from (2)]. Additionally, the length of the ET, L_{Term} that contributes to maximum blocking efficiency is equal to a certain multiple of t_{dr} (around $5 \sim 6$ for SM-JTEs). Therefore, we are constrained to use smaller L_{Period} values. We chose a range of $L_{JTE,1}$ values, from small to large: $10\mu m$, $17.5\mu m$, $25\mu m$, and $45\mu m$ in a stark contrast to SiC SM-JTE designs [42], [44]–[48] in an effort to achieve a reasonable $L_{Gap,1}$ value.

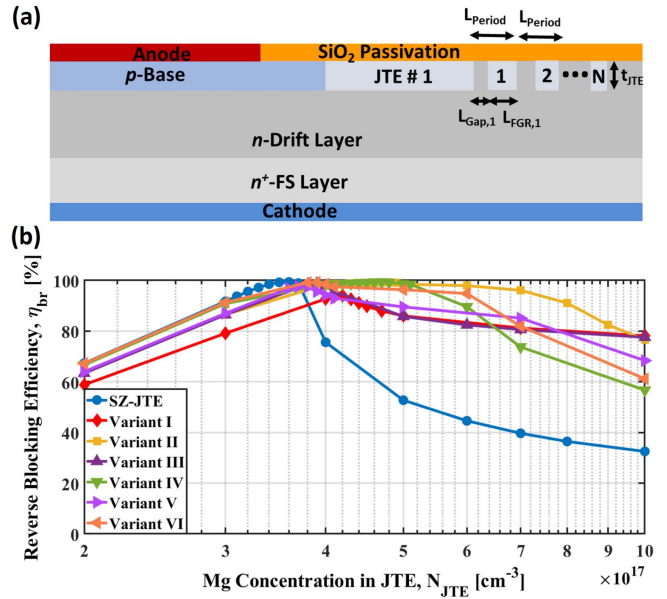Plots of simulated reverse blocking efficiency, η_{br} versus JTE Mg-concentration, N_{JTE} for six variants are illustrated

FIGURE 11. SM-JTE scheme: (a) schematic diagram and (b) plots of simulated η_{br} versus Mg concentration in the JTE and the FGRs, N_{JTE} for the six variants. For comparison, SZ-JTE plot is also included. For the details of the variants, please refer to Table 2. In (a), *p*-type SM-FGRs have the same doping concentration as the p^--JTE and they are appended to the JTE, in contrast to SZ-JTE scheme aided by SM-FGRs pictured in Fig. 9.

TABLE 2. Details of various SM-JTE variants.

Variant	$L_{JTE,1}$	N_{FGR}	L_{Period}	Range of $a_{FGR,i}$
I	$10\mu m$	6	$10\mu m$	$0.8 \sim 0.55$
II	$10\mu m$	6	$10\mu m$	$0.95 \sim 0.7$
III	$25\mu m$	5	$10\mu m$	$0.8 \sim 0.6$
IV	$25\mu m$	5	$10\mu m$	$0.95 \sim 0.75$
V	$17.5\mu m$	3	$17.5\mu m$	$0.9 \sim 0.8$
VI	$45\mu m$	5	$6\mu m$	$0.917 \sim 0.583$

The number of FGRs is indicated as N_{FGR}. For each variant, $L_{FGR,i}$ is decreased in equal steps. The total length of the ET scheme is given by $L_{Term} = L_{JTE,1} + N_{FGR} \times L_{Period}$. The various dimensions are defined in Fig. 11(a) and (4).

in Fig. 11(b). The details of the SM-JTE variants appear in Table 2 while the performance metrics of the SM-JTE schemes are listed in Table 3. Concerning the initial design targets, $N_{JTE,LB}$ is greater than $2 \times 10^{17} cm^{-3}$ in all cases. Referring to Fig. 11(b), $N_{JTE,UB}$ approaches high $10^{17} cm^{-3}$ mark for all the variants. In short, except for variants I and III falling slightly short of the EDW target for $\eta_{br} \sim 90\%$, all of the SM-JTE schemes fulfill the previously outlined design targets in Section III-A. The SM-JTE is the only ET design to have achieved this landmark.

Variants II, IV, and VI demonstrate the EDW widening effect with increasingly gradual modulation. For each curve, the starting point of the plateau on the left corresponds to the maximum blocking efficiency of the SZ-JTE, similar to the SiC case [44]. For variant VI, at lower values of N_{JTE}, the electric field lines crowd around the *p*-base/JTE interface since the field is not effectively transmitted along the JTE. Therefore, these structures act very similarly, and

TABLE 3. Performance of SM-JTE variants.

Var.	EDW$_1$ ($\eta_{br} \sim 80\%$) [$\times 10^{17}$cm^{-3}]	EDW$_2$ ($\eta_{br} \sim 90\%$) [$\times 10^{17}$cm^{-3}]	ΔEDW (EDW$_1$−EDW$_2$) [$\times 10^{17}$cm^{-3}]	$N_{JTE,LB}$ ($\eta_{br} \sim 90\%$) [$\times 10^{17}$cm^{-3}]
I	5	0.7	4.3	3.78
II	6.73	4.82	1.91	3.28
III	4.92	1.38	3.54	3.22
IV	4.1	3	1.1	2.96
V	5.16	1.66	3.5	3.17
VI	4.77	3.42	1.35	2.95

Effective doping windows [*vide* Fig. 1] for six variants, the details of which can be found in Table II. The windows for both 80% and 90% η_{br} are shown. For the demonstration of extension of the EDW when the target η_{br} is lowered, the difference between 80% and 90% η_{br} is shown as ΔEDW in the fourth column. The rightmost column displays the minimum doping in the JTE and the FGRs, $N_{JTE,LB}$ to achieve $\eta_{br} \sim 90\%$.

variant VI is not much different from the SZ-JTE. Variant IV is also seen to behave very similarly to these ET schemes at low doping levels, however, because of the more slowly modulated $N_{Mg,Avg}$, even with a moderate JTE length ($L_{JTE,1} = 25\mu$m) there is a significant expansion of the EDW. It follows that variant II, with the most gradual space modulation, has the widest EDW of all. However, this comes at the expense of a small $L_{Gap,1}$ value. From practical processing considerations, a larger $L_{Gap,1}$ value can be chosen with a slightly reduced EDW value. There is, however, another option to maintain high EDW values. For the N_{dr} value considered in this work (Section III-B), the diode is in PT mode up to a maximum t_{dr} value of 30μm (corresponds to $V_{br,id} = 6.78$kV). As long as PT operation is maintained, we can increase t_{dr} value to obtain a larger $L_{Gap,1}$ value suitable for practical photolithographic resolution without compromising EDW values.

Variants I and III reinforce the need for gradualness with $L_{Gap,1}$ being too large to effectively transfer the field to the rest of the rings even with otherwise comparable structures to II and IV. Variant V enables a tradeoff between large EDW and large values of L_{Period} and $L_{Gap,1}$. Therefore, the precision with which $L_{Gap,1}$ can be defined ultimately dictates the choice of SM-JTE variants, unlike SiC *p-i-n* diodes.

Simulated electric field profiles of SZ-JTE, and SM-JTE variants II and V are shown in Fig. 12(a). In the SZ-JTE case, field crowding occurs at the JTE corner, as shown by the hotspot. The JTE Mg-concentration is past the optimum value ($N_{JTE,opt} = 3.8 \times 10^{17}$cm^{-3}) and, therefore, the JTE is not fully depleted. This incomplete depletion of the JTE results in the JTE corner bearing the brunt of electric field crowding. In contrast, the SM-JTE variants spread the electric field over a large distance causing the electric field crowding to be shared by both the JTE and the SM-FGRs and thereby blunting the impact of field crowding.

It is important to notice that electric field crowding gives rise to large leakage leading to premature breakdown (usually not predicted by TCAD simulations in the absence of precise modeling in GaN) and breakdown voltage
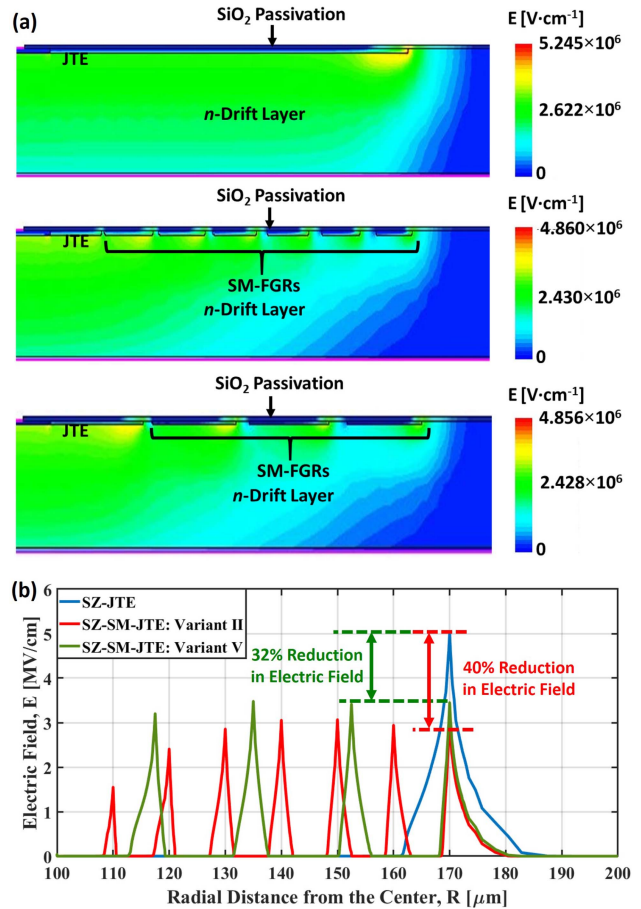

FIGURE 12. (a) Simulated 2-D electric field profiles of SZ-JTE [top profile], SM-JTE variant II [middle profile], and SM-JTE variant V [bottom profile] with a Mg-concentration in the JTE of 4×10^{17}cm^{-3} and at a reverse bias of ~ 3.5kV and **(b)** electric field at the SiO$_2$/JTE interface. In all three cases, the total length of the termination, $L_{Term} = 70\mu$m has been used for fair comparison.

walkout [44]. During avalanche runaway, some of the electrons have enough energy to cross the passivation dielectric/semiconductor barrier and slip into the conduction band of the dielectric. These electrons get trapped and charge the dielectric negatively, causing the reduction of electric field in the surface depletion region of the *p-n* junction [49]. Thus, V_{br} is temporally dependent on reverse stress, giving rise to instability. This phenomenon is referred to as breakdown voltage walkout. Therefore, reducing the electric field at the SiO$_2$/JTE interface is crucial. The electric field profiles for SZ-JTE and SM-JTE variants II and V at the SiO$_2$/JTE interface are shown in Fig. 12(b). Variants II and V succeed in reducing the interfacial electric field by $\sim 40\%$ and $\sim 32\%$, respectively. Therefore, SM-JTE schemes can efficiently mitigate field crowding and associated problems in the JTE end of SZ-JTE schemes.

The device fabrication flow for *p-i-n* diodes with SM-JTE ET schemes using SNS-SAG is shown in Fig. 13. The regular device structure for SM-JTE schemes shown in Fig. 11(a) needs to be specially adapted to conform to SNS-SAG processing, while retaining all the key features and achievements
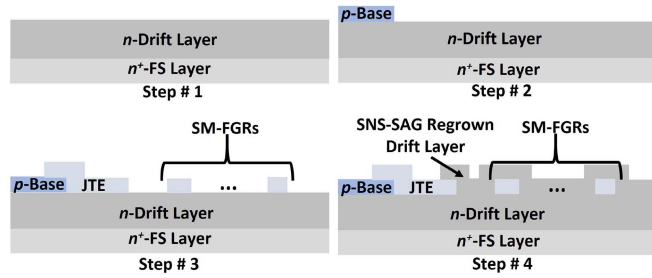
FIGURE 13. SNS-SAG fabrication flow for *p-i-n* diodes with SM-JTE ET schemes sans passivation layer and electrodes. Step # 1 is the starting GaN substrate with initial drift layer, followed by SNS-SAG growth of *p*-base (Step # 2, first SAG layer). These steps are followed by SNS-SAG growth of JTE and SM-FGRs using single SAG mask (Step # 3, second SAG layer). The process is wrapped up by selective regrowth of drift layer (Step # 4, third SAG layer).
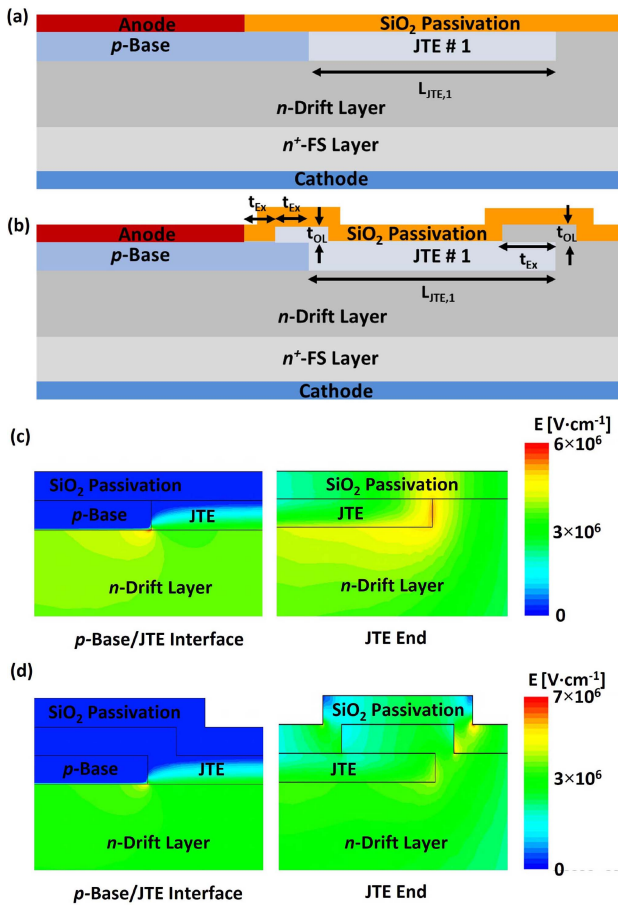

FIGURE 14. Modifications to standard *p-i-n* diode structure for SNS-SAG processing: (a) schematic diagram of regular half-structure with SZ-JTE ET, (b) schematic diagram of practical half-structure with SZ-JTE ET for SNS-SAG processing, (c) simulated post-breakdown 2-D electric field profile of the structure in (a), and (d) simulated post-breakdown 2-D electric field profile of the structure in (b). In (a) and (b), $L_{JTE,1} = 50\mu$m, $t_{OL} = 500$nm, and $t_{Ex} = 2.5\mu$m. For both (c) and (d), a reverse bias of $\sim$ 5kV and an optimum Mg-concentration in the JTE, $N_{JTE,opt}$ of 3.8×10^{17}cm^{-3} have been considered.

of SM-JTE schemes designed so far. The justification for this modified device structure is provided in the Appendix. As shown in Fig. 13, we need three SNS-SAG mask steps

for SM-JTE schemes. Finally, the low-leakage feature with smooth vertical sidewall enabled by SNS-SAG can serve as a key to successful integration of the SM-JTE schemes designed above to GaN power devices.

IV. CONCLUSION

Reverse blocking efficiency and excessive leakage are two major issues in modern GaN power devices. To combat this, we have developed solutions in the form of a damage-free selective-area processing technique and high-efficiency edge termination schemes. SNS-SAG was demonstrated as an effective way of making smooth, thick sidewalls and was shown to have more than four orders of magnitude lower leakage current than an optimized ICP-RIE method. Through detailed analysis and optimization of various edge termination techniques, SM-JTE schemes enabled by SNS-SAG technique were demonstrated as a practical means that creates a wide effective doping window and avoids issues with other methods. Together, SNS-SAG and SM-JTE schemes have great promise for producing highly efficient GaN power devices.

APPENDIX

For practical SNS-SAG processing, we need to consider the resolution of photolithography techniques. As a general example, we will consider a simple SZ-JTE structure. Schematic diagrams of regular and practical *p-i-n* diode half-structures with SZ-JTE ET scheme are illustrated in Figs. 14(a) and 14(b), respectively. The regular structure in Fig. 14(a) is more suitable for implant-based processing. In contrast, controlling range and dosage in ion implantation is difficult for GaN power devices [50], due to various defects and lattice damages. The major problem in the regular structure, is the difficulty in achieving precise mask alignment at various interfaces. By using the structure in Fig. 14(b), the mask alignment requirement is bypassed. The 2-D post-breakdown electric field profiles at *p*-base/JTE interface and JTE end of the structures depicted in Figs. 14(a) and 14(b) are shown in Figs. 14(c) and 14(d), respectively. The electric field crowding at the *p*-base/JTE interface is similar. The V_{br} value for the practical structure is 4.38kV compared to a value of 4.39kV for the regular structure. Thus, the structures in Figs. 14(a) and 14(b) are equivalent. For the sake of simplicity, the analysis has been performed for SZ-JTE structure.

ACKNOWLEDGMENT

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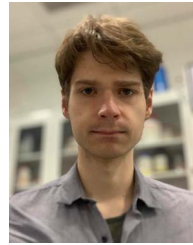
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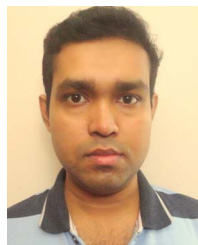
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