Received 17 September 2020; revised 30 October 2020; accepted 8 November 2020. Date of publication 17 November 2020; date of current version 28 January 2021. The review of this article was arranged by Editor S. Ikeda.

Digital Object Identifier 10.1109/JEDS.2020.3038391

Improvement in Self-Heating Characteristic by Incorporating Hetero-Gate-Dielectric in Gate-All-Around MOSFETs

YOUNG SUH SONG [1,2] (Graduate Student Member, IEEE), JANG HYUN KIM [3] (Member, IEEE), GARAM KIM [4], HYUN-MIN KIM [1] (Graduate Student Member, IEEE), SANGWAN KIM [5] (Member, IEEE), AND BYUNG-GOOK PARK [1] (Fellow, IEEE)

1 Department of Electrical and Computer Engineering, Inter-University Semiconductor Research Center, Seoul National University, Seoul 08826, South Korea
2 Department of Computer Science, Korea Military Academy, Seoul 01805, Republic of Korea
3 School of Electrical Engineering, Pukyong National University, Busan 48513, Republic of Korea
4 Department of Electronic Engineering, Myongji University, Yongin 17058, Republic of Korea
5 Department of Electrical and Computer Engineering, Ajou University, Suwon 16499, Republic of Korea

CORRESPONDING AUTHORS: S. KIM AND B.-G. PARK (e-mail: sangwan@ajou.ac.kr; bgpark@snu.ac.kr)

This work was supported in part by the MOTIE/KSRC (Future Semiconductor Device Technology Development Program) under Grant 10080575; in part by the National Research Foundation (NRF) of Korea funded by MSIT under Grant NRF-2020R1F1A1072340 and Grant NRF-2020M3F3A2A01081672; in part by the National Research Foundation of Korea grant funded by the Korea Government (MSIT) under Grant 2020R1G1A1101263; in part by the 2021 Research Fund of Korea Military Academy (Hwarangdae Research Institute); in part by the Brain Korea 21 Plus Project in 2021; and in part by the Pukyong National University Research Fund in 2020 under Grant CD20200849.

(Young Suh Song and Jang Hyun Kim contributed equally to this work.)

ABSTRACT For improving self-heating effects (SHEs) in gate-all-around metal-oxide-semiconductor field-effect transistors (GAA MOSFETs), hetero-gate-dielectric (HGD) is utilized. The HGD consists of hafnium dioxide (HfO_2) and silicon dioxide (SiO_2), which has high thermal conductivity, hence SHEs are improved. In order to validate the HGD, technology computer-aided design (TCAD) simulation is performed through Synopsys Sentaurus three-dimensional (3D) tool. As a result, when the HGD is adopted in GAA MOSFETs, SHEs can be significantly improved from 498 K to 415 K. In addition, suppression of gate current, more than 2 orders, is also achieved because of bigger bandgap of SiO_2 in HGD. Consequently, this structure takes advantage of higher thermal conductivity and bigger bandgap of SiO_2, and higher permittivity of HfO_2 for improving SHEs and gate leakage current.

INDEX TERMS Self-heating effects (SHEs), hetero-gate-dielectric (HGD), GAA MOSFETs, nanowire, high-k, gate current.

I. INTRODUCTION

Recently, gate-all-around metal-oxide-semiconductor field-effect transistors (GAA MOSFETs) have been broadly researched as the substitutable devices for FinFETs due to their higher gate controllability [1]–[3]. In addition, the GAA MOSFETs adopting high-κ/metal gate (HKMG) technology have been widely investigated for the superior electrical performance [4]–[7]. Therefore, the GAA MOSFETs with HKMG have emerged as promising candidates to the real industries [8]–[11]. However, they have disadvantage in terms of heat dissipation due to high-κ dielectric, which is lower thermal conductivity material and fully covers channel area in contrast to FinFETs [12]–[14]. For this reason, it has been widely accepted that the GAA MOSFETs are inferior to FinFETs in terms of self-heating effects (SHEs) [15]–[21]. These SHEs cause lots of reliability issues such as metallization lifetimes of circuit [22], negative-bias temperature instability [23], hot-carrier induced degradation [24], [25], and decrease of threshold voltage as well [26]–[27]. Importantly, this SHE becomes remarkable as the device is scaled down [28]. As more and more integration has achieved, increased number of transistors are integrated in unit area of semiconductor chip and more heat per unit area is generated [28]. Therefore, the importance of SHE becomes

critical as device is scaled down. Namely, for the successful integration with safety device operation, it is essential to improve SHEs for accomplishing high integration with better device reliability.

In order to address these issues, the omega-shaped-gate nanowire MOSFETs (ONWFETs) have been presented in [29]. However, changing the gate shape concomitantly degrades gate controllability. Furthermore, the structure of ONWFETs are not suitable for vertically stacked GAA MOSFETs. Therefore, it requires another strategy to address the above-mentioned issues.

In addition, gate current has also arisen as one of the important reliability issues as well [30]. Specifically, as the modern HKMG technology incorporates HfO_2 for gate dielectric material, lots of gate current flows through gate dielectric due to the low bandgap of HfO_2 and oxide reliability issues become a critical problem in modern HKMG GAA MOSFET [31]. Therefore, it is really important to improve gate current in designing GAA MOSFET.

In this framework, the aim of this article is to improve SHEs and gate current in GAA MOSFETs using the structure with hetero-gate-dielectric (HGD) [32]. Conventionally, the HGD structure has been adopted for lowering gate-to-drain coupling and consequently reducing undesirable ambipolar current in Tunnel FET (TFET) by utilizing dual permittivity (dual-?) of two dielectric materials [33]. Specifically, by partially using low permittivity material (SiO_2) in drain side of HGD of TFET, it was possible to reduce undesirable ambipolar current in TFET caused by gate-to-drain coupling and maintain significant on-current characteristic due to high permittivity material (HfO_2) in source side of HGD of TFET [34].

By incorporating this HGD structure into GAA MOSFET, the proposed structure intelligently takes the advantages of HfO_2 (high permittivity) and SiO_2 (high thermal conductivity and bandgap) simultaneously for improving SHEs and gate current.

This article is organized as follows. First, the electrical characteristics such as on-current (I_{ON}) and off-current (I_{OFF}) are analyzed after calibration. Second, the improvement of SHEs and gate current from the proposed structure have been discussed by investigating the location of heat dissipation path. Finally, the gate leakage current, which is the main source of degradation in oxide reliability, is analyzed [30].

II. DEVICE STRUCTURE AND MODEL PHYSICS

The proposed HGD-GAA MOSFET structures used in this article are simulated using Synopsys Sentaurus three-dimensional (3D) TCAD simulation [36]. For detailed specification of structures, the value of the 5-nm node presented in the International Technology Road Map for Semiconductors (ITRS) is utilized [37].

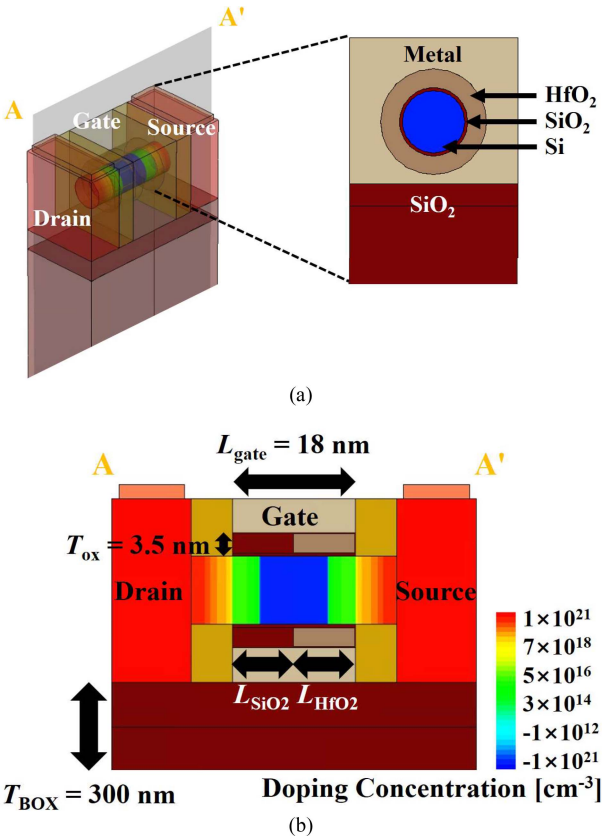

FIGURE 1. (a) Overall structure of the proposed HGD-GAA MOSFET with cross sectional view illustrating gate, gate dielectric, and channel. (b) Another cross-sectional view of the proposed HGD-GAA MOSFET describing position of HGD. The proposed HGD-GAA MOSFET features different gate insulators at the source side (high-κ material, HfO_2) and drain side (high thermal conductivity material, SiO_2). The SiO_2 in HGD-GAA MOSFET effectively acts as heat sink, which improves SHEs.

A. STRUCTURE OF THE PROPOSED HGD-GAA MOSFET

Fig. 1 shows the schematic structure of the proposed HGD-GAA MOSFET. The gate stack is composed of 3 nm-thick HGD and 0.5 nm-thick interfacial SiO_2 layers [Fig. 1(a)]. Since most heat generation in GAA MOSFETs occurs at drain side of channel [15]–[21], SiO_2 is added at the drain side of gate stack due to high thermal conductivity [Fig. 1(b)]. The HGD layer is varied with SiO_2 length (L_{SiO_2}) of 4.5, 9, 13.5 nm. Moreover, the proposed HGD-GAA MOSFETs have gate length (L_{gate}) of 18 nm, and channel diameter of 10 nm. The doping concentration for source/channel/drain regions are set as $1\times10^{21}/1\times10^{15}/1\times10^{21}$ cm^{-3}, respectively. The thermal conductivities of 0.49, 1.4, 7.5, 15 W/(K·m) are applied for HfO_2, SiO_2, Si, Si_3N_4, respectively [38]. Then, all of parameters are summarized in Table 1.

For the purpose of investigating the electrical and thermal characteristics, thermodynamic, Shockley-Read-Hall (SRH) recombination, high field saturation, and Fermi models are used by Synopsys Sentaurus 3D TCAD simulation. In addition, trap-assisted-tunneling (TAT), Fowler Nordheim (FN)

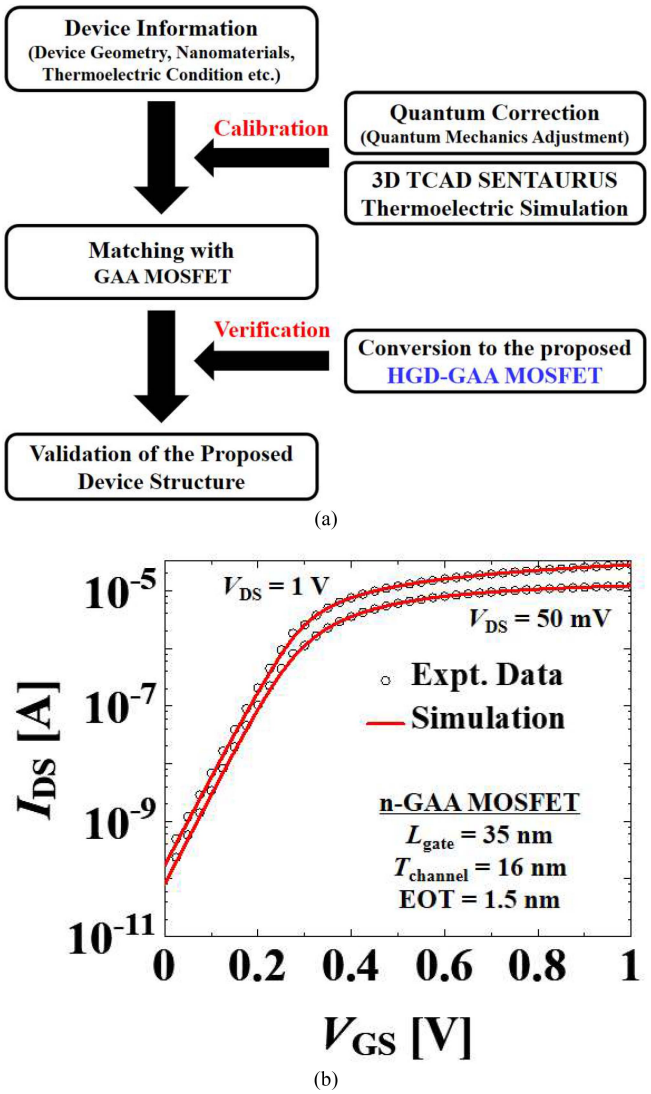

FIGURE 2. **(a) Overall workflow for validation of the proposed device structure. (b) $I_{DS} - V_{GS}$ calibration results based on the GAA MOSFET structure [10].**

tunneling, and direct tunneling are considered to precisely analyze gate current.

B. WORKFLOW OF STUDY AND CALIBRATION PROCESS

Fig. 2(a) explains the overall workflow in this study. The calibration of GAA MOSFET is performed and then the HGD layer is incorporated. Finally, validation of the proposed HGD-GAA MOSFET is conducted in terms of SHEs and gate current.

During calibration, quantum correlations are conducted for I_{DS}-V_{GS} calibration under Synopsys Sentaurus 3D TCAD simulation [36]. For more accurate simulation, we use the mobility model (phumob/Enormal(Lombardi)/thin layer) to consider Coulomb scattering and interfacial surface calibration roughness scattering. First, I_{DS}-V_{GS} calibration is performed by carefully applying the quantum model and velocity saturation model and gate work function (WF).

TABLE 1. **Used model parameters and corresponding values.**

Symbol	Model Parameter	Value	Unit[a]
L_{gate}	Gate length	18	nm
L_{HfO2}	Hafnium oxide length	13.5, 9, 4.5	nm
L_{SiO2}	Silicon dioxide length	4.5, 9, 13.5	nm
T_{ox}	Gate stack thickness	3.5	nm
T_{HfO2}	Hafnium oxide thickness	3	nm
T_{SiO2}	Silicon dioxide thickness	0.5	nm
T_{BOX}	Buried oxide thickness	300	nm
κ_{HfO2}	Hafnium oxide thermal conductivity	0.49	W/(K*m)
κ_{SiO2}	Silicon dioxide thermal conductivity	1.4	W/(K*m)
κ_{Si}	Silicon thermal conductivity	7.5	W/(K*m)
κ_{Si3N4}	Silicon nitride thermal conductivity	15	W/(K*m)

[a]The stated units are the same as international system of units (SI) for Thermoelectrics [37]; nm = nanometer, W = Watt, K = Kelvin, m = meter.

Second, the thermal conductivity, heat conduction paths, and thermal boundary condition (300 K) to each heat path are adjusted in order to reflect the thermal characteristics of the GAA MOSFET. Fig. 2(b) demonstrates our simulation results are well fit with the measured data of the GAA MOSFET [10].

III. RESULTS AND DISCUSSION

A. COMPARATIVE ANALYSIS BY ELECTRICAL CHARACTERISTICS

Fig. 3(a) illustrates transfer characteristics of conventional GAA MOSFET (L_{SiO_2} = 0 nm), the proposed HGD-GAA MOSFETs (L_{SiO_2} = 4.5, 9, 13.5 nm), and SiO_2-based GAA MOSFET (L_{SiO_2} = 18 nm). For comparing I_{ON} and I_{OFF} in these structures, drain voltage (V_{DS}) is fixed at 0.6 V, and both I_{ON} and I_{OFF} are calculated on the basis of drain current under same gate voltage (V_{GS} = 0.6 V). As demonstrated in Fig. 3(b), the increase of L_{SiO2} gradually increases I_{OFF} and gradually decreases I_{ON} due to lower gate controllability from shorter L_{HfO_2} in HGD. Remarkably, the difference of I_{ON} between conventional GAA MOSFET and the proposed HGD-GAA MOSFETs is mitigated as SHEs are considered [Fig. 4] because conventional GAA MOSFET suffers more SHEs compared to the proposed HGD-GAA MOSFETs (This will be explained at the following paragraph).

B. IMPROVEMENT OF SHES BY THE PROPOSED HGD-GAA MOSFET

For investigating the improvement of SHEs, the maximum temperature of the devices is investigated with conventional GAA MOSFET (L_{SiO_2} = 0 nm), the proposed HGD-GAA MOSFETs (L_{SiO_2} = 4.5, 9, 13.5 nm), and SiO_2-based GAA MOSFET (L_{SiO_2} = 18 nm) as demonstrated in Fig. 5. The maximum temperature is calculated when $V_{DS} = V_{GS}$ = 0.6 V and it has been demonstrated that maximum temperature is significantly improved from 498 K to 415 K by using the structure of the proposed HGD-GAA MOSFET. Specifically, the maximum temperature is

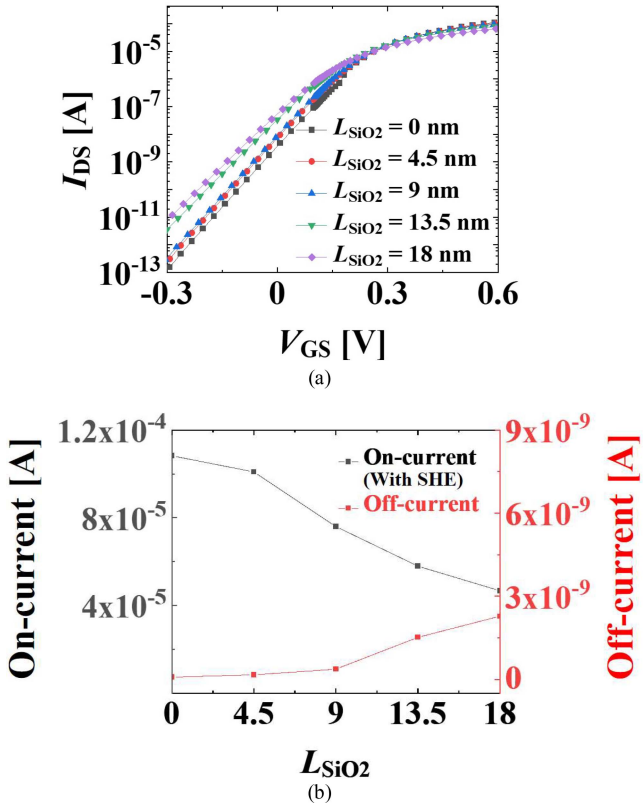

FIGURE 3. (a) Transfer curves of the conventional GAA MOSFET (L_{SiO_2} = 0 nm), the proposed HGD-GAA MOSFETs (L_{SiO_2} = 4.5, 9, 13.5 nm), and SiO_2-based GAA MOSFET (L_{SiO_2} = 18 nm). Conventional GAA MOSFET shows better transfer characteristics due to higher gate control ability with longer HfO_2. (b) I_{ON} and I_{OFF} of the conventional GAA MOSFET (L_{SiO_2} = 0 nm), the proposed HGD-GAA MOSFETs (L_{SiO_2} = 4.5, 9, 13.5 nm), and SiO_2-based GAA MOSFET (L_{SiO_2} = 18 nm). I_{ON} and I_{OFF} are calculated when V_{GS} = 0.6 V and 0 V respectively.

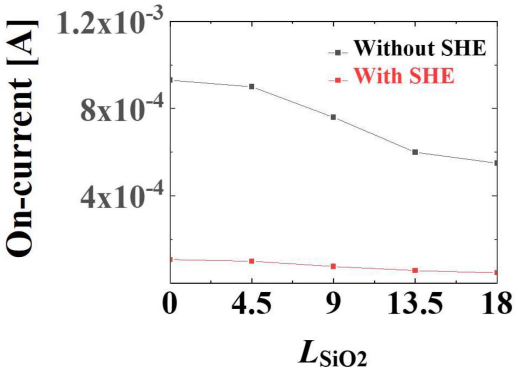

FIGURE 4. I_{ON} calculated with SHEs and without SHEs. It is remarkable that the difference in I_{ON} is mitigated when SHEs are considered. Since conventional GAA MOSFET suffers from more SHEs compared to the proposed HGD-GAA MOSFETs, the actual difference in I_{ON} decrease as SHEs are considered.

dramatically improved when SiO_2 in HGD layer is initially introduced at drain side (when L_{SiO_2} varies from 0 nm to 4.5 nm) because the maximum temperature of the devices is determined by the drain side of channel [Fig. 6].

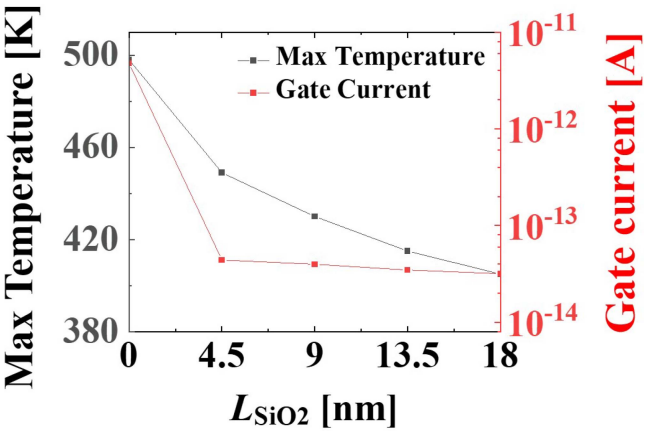

FIGURE 5. Maximum temperature and gate current are simulated with the conventional GAA MOSFET (L_{SiO_2} = 0 nm), the proposed HGD-GAA MOSFETs (L_{SiO_2} = 4.5, 9, 13.5 nm), and SiO_2-based GAA MOSFET (L_{SiO_2} = 18 nm). The newly added material SiO_2 in the proposed HGD-GAA MOSFETs significantly decrease maximum temperature from its higher thermal conductivity and improves gate current from its higher bandgap.

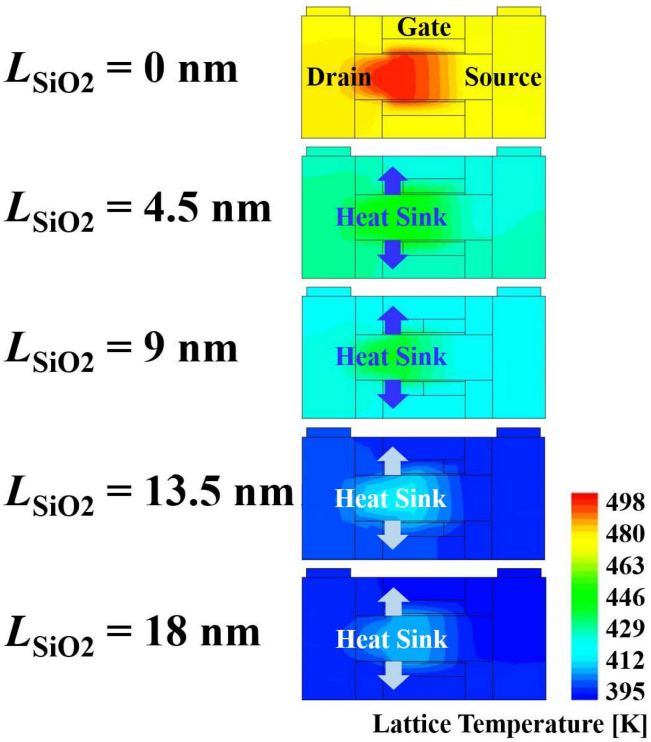

FIGURE 6. The cross-sectional view describing distribution of lattice temperature and location of heat sink. The lattice temperature is calculated when V_{GS} = 0.6 V and V_{DS} = 0.6 V.

C. IMPROVEMENT OF GATE CURRENT BY THE PROPOSED HGD-GAA MOSFET

Interestingly, our proposed structure can also improve gate current as well. The gate current is successfully suppressed by introducing HGD layer [Fig. 5] and this result can be explained by energy band diagram. As illustrated in Fig. 7(a), the HfO_2 has lower bandgap and conventional

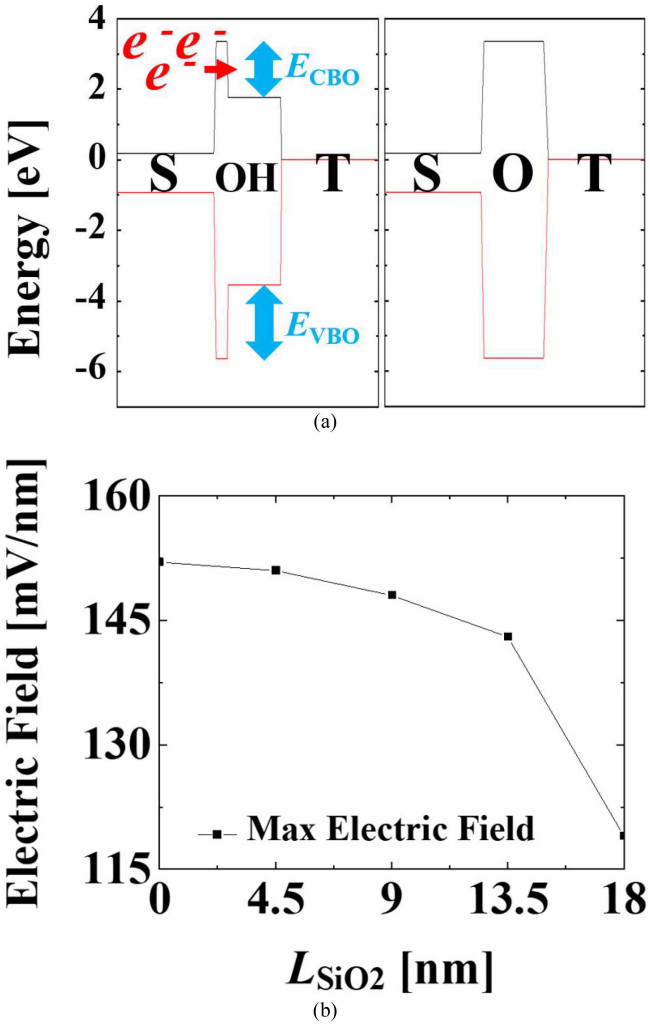

FIGURE 7. (a) Comparison of energy band diagram of conventional GAA MOSFET (left side) and that of the proposed HGD-GAA MOSFET (right side). The abbreviated letters S, H, O, T stand for Si, HfO_2, SiO_2 (interfacial layer), titanium nitride (TiN, gate metal) respectively. Energy band diagram of conventional GAA MOSFET includes description of conduction band offset (CBO) and valance band offset (VBO). (b) Comparison of the maximum electric field at gate dielectric of the conventional GAA MOSFET (L_{SiO_2} = 0 nm), the proposed HGD-GAA MOSFETs (L_{SiO_2} = 4.5, 9, 13.5 nm), and SiO_2-based GAA MOSFET (L_{SiO_2} = 18 nm).

GAA MOSFET consequently has higher conduction band offset (CBO) and valence band offset (VBO) at the same time. On the other hand, SiO_2 in HGD layer has higher bandgap and is possible to act as suppressor against direct tunneling.

In addition, maximum electric field at gate dielectric also decreases as L_{SiO_2} increases due to decrease of effective equivalent oxide thickness (EOT) [Fig. 7(b)]. Therefore, the decrease of electric field also contributes to the decrease of gate current [Fig. 5].

Specifically, gate current is significantly suppressed when SiO_2 in HGD is initially introduced at drain side (when L_{SiO_2} varies from 0 nm to 4.5 nm) as shown in Fig. 5. This is because electron at drain side has highest energy from increased temperature [Fig. 6] whereas SiO_2 in the drain side of HGD layer can efficiently suppress the direct tunneling of this high energy electron. Therefore, our proposed technique is strategic for preventing SHEs and oxide degradation at the same time [39].

IV. CONCLUSION

We have demonstrated the improvement of self-heating characteristic by our proposed structure with HGD layer in GAA MOSFETs. Our proposed structure utilizes the advantage of higher thermal conductivity of SiO_2 for improving SHEs. Furthermore, incorporating HGD layer in GAA MOSFETs can significantly improve gate leakage current as well because the bigger bandgap of SiO_2 in HGD layer results in suppression of direct tunneling. Our proposed structure is strategic for future scaling technology with improved SHEs and also opens up potential possibility of SHEs improvement in vertically stacked GAA MOSFETs.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

REFERENCES

[1] C.-C. Chung, H.-Y. Ye, H. H. Lin, W. K. Wan, M.-T. Yang, and C. W. Liu, "Self-heating induced interchannel Vt difference of vertically stacked Si nanosheet gate-all-around MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 12, pp. 1913–1916, Dec. 2019.

[2] Y. Choi *et al.*, "Simulation of the effect of pSimulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FETarasitic channel height on characteristics of stacked gate-all-around nanosheet FET," *Solid-State Electron.*, vol. 164, pp. 1–7, Feb. 2020.

[3] Y. Huang, M. Chiang, and S. Wang, "Speed optimization of vertically stacked gate-all-around MOSFETs with inner spacers for low power and ultra-low power applications," in *Proc. 20th Int. Symp. Qual. Electron. Design (ISQED)*, Santa Clara, CA, USA, 2019, pp. 231–234.

[4] J.-W. Han, D.-I. Moon, J. S. Oh, Y.-K. Choi, and M. Meyyappan, "Vacuum gate dielectric gate-all-around nanowire for hot carrier injection and bias temperature instability free transistor," *Appl. Phys. Lett.*, vol. 104, no. 25, pp. 1–3, Jun. 2014.

[5] J. Madan and R. Chaujar, "Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 2, pp. 227–234, Jun. 2016.

[6] D.-I. Moon *et al.*, "Silicon nanowire all-around gate MOSFETs built on a bulk substrate by all plasma-etching routes," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 452–454, Apr. 2011.

[7] Y. S. Song *et al.*, "Tunneling oxide engineering for improving retention in nonvolatile charge-trapping memory with TaN/Al_2O_3/HfO_2/SiO_2/Al_2O_3/SiO_2/Si structure," *Jpn. J. Appl. Phys.*, vol. 59, no. 6, pp. 1–7, Jun. 2020.

[8] Y. Y. Yeoh *et al.*, "Investigation on hot carrier reliability of gate-all-around twin Si nanowire field effect transistor," in *Proc. IEEE Int. Rel. Phys. Symp.*, Montreal, QC, Canada, Apr. 2009, pp. 400–404.

[9] J. Zhang *et al.*, "High-*k* metal gate fundamental learning and multi-Vt options for stacked nanosheet gate-all-around transistor," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 22.1.1–22.1.4.

[10] S. Bangsaruntip *et al.*, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *IEEE IEDM Tech. Dig.*, Dec. 2009, pp. 297–300.

[11] J. Park *et al.*, "Investigation of self-heating effects in gate-all-around MOSFETs with vertically stacked multiple silicon nanowire channels," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4393–4399, Nov. 2017.

[12] E. Bury *et al.*, "Self-heating in FinFET and GAA-NW using Si, Ge and III/V channels," in *IEDM Tech. Dig.*, Dec. 2016, pp. 15.6.1–15.6.4.
[13] S. Shin *et al.*, "Direct observation of self-heating in III–V gate-all-around nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3516–3523, Nov. 2015.
[14] M. A. Wahab, S. Shin, and M. A. Alam, "3D modeling of spatiotemporal heat-transport in III-V gate-all-around transistors allows accurate estimation and optimization of nanowire temperature," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3595–3604, Nov. 2015.
[15] H. Kim. Y. Seo, I. H. Myong, M. Kang, and H. Shin, "Analysis on DC and AC characteristics of self heating effect in nanowire," *J. Nanosci. Nanotechnol.*, vol. 17, no. 5, pp. 3056–3059, May 2017.
[16] S. H. Shin *et al.*, "Impact of nanowire variability on performance and reliability of gate-all-around III-V MOSFETs," in *IEDM Tech. Dig.*, Dec. 2013, pp. 7.5.1–7.5.4.
[17] O. Badami, F. Driussi, P. Palestri, L. Selmi, and D. Esseni, "Performance comparison for FinFETs, nanowire and stacked nanowires FETs: Focus on the influence of surface roughness and thermal effects," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 13.2.1–13.2.4.
[18] M. A. Wahab, S. Shin, and M. A. Alam, "Spatio-temporal mapping of device temperature due to self-heating in Sub-22 nm transistors," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Pasadena, CA, USA, 2016, pp. 1–6.
[19] G. Chalia and R. S. Hegde, "Study of self-heating effects in silicon nano-sheet transistors," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Shenzhen, China, 2018, pp. 1–2.
[20] C. Prasad, S. Ramey, and L. Jiang, "Self-heating in advanced CMOS technologies," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. 6A-4.1–6A-4.7.
[21] W. Ahn *et al.*, "Integrated modeling of Self-heating of confined geometry (FinFET, NWFET, and NSHFET) transistors and its implications for the reliability of sub-20 nm modern integrated circuits," *Microelectron. Rel.*, vol. 81, pp. 262–273, Feb. 2018.
[22] B. K. Liew, N. W. Cheung, and C. Hu, "Effects of self-heating on integrated circuit metallization lifetimes," in *IEDM Tech. Dig.*, Dec. 1989, pp. 323–326.
[23] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, no. 1, pp. 1–18, Jun. 2003.
[24] P. Aminzadeh, M. Alavi, and D. Scharfetter, "Temperature dependence of substrate current and hot carrier-induced degradation at low drain bias," in *Symp. VLSI Technol. Dig.*, Jun. 1998, pp. 178–179.
[25] N. Sano, M. Tomizawa, and A. Yoshii, "Temperature dependence of hot carrier effects in short-channel Si-MOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 12, pp. 2211–2216, Dec. 1995.
[26] J. Roig, D. Flores, S. Hidalgo, M. Vellvehi, J. Rebollo, and J. Millán, "Study of novel techniques for reducing self-heating effects in SOI power LDMOS," *Solid-State Electron.*, vol. 46, no. 12, pp. 2123–2133, Dec. 2002.
[27] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, J. T. Bunyan and M. J. Uren, "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2240–2248, Dec. 1996.
[28] E. Burt *et al.*, "Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes," in *Proc. IEEE Int. Rel. Phys. Symp.*, Waikoloa, HI, USA, Jun. 2014, pp. XT.8.1–XT.8.6.
[29] Y. S. Song *et al.*, "Electrical and thermal performances of omega-shaped-gate nanowire field effect transistors for low power operation," *J. Nanosci. Nanotechnol.*, vol. 20, no. 7, pp. 4092–4096, Jul. 2020.
[30] E. Cartier *et al.*, "Fundamental aspects of HfO_2-based high-k metal gate stack reliability and implications on tinv-scaling," in *Proc. Int. Electron Device Meeting (IEDM)*, Washington, DC, USA, Dec. 2011, pp. 18.4.1–18.4.4.
[31] B. Kaczer *et al.*, "Electrical and reliability characterization of metal-gate/HfO_2/Ge FET's with Si passivation," *Microelectron. Eng.*, vol. 84, nos. 9–10, pp. 2067–2070, Sep./Oct. 2007.
[32] W. Y. Choi and W. Lee, "Hetero-gate-dielectric tunneling field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317–2319, Sep. 2010.
[33] M. J. Lee and W. Y. Choi, "Effects of device geometry on hetero-gate-dielectric tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1459–1461, Oct. 2012.
[34] N. Cui, R. Liang, and J. Xu, "Heteromaterial gate tunnel field effect transistor with lateral energy band profile modulation," *Appl. Phys. Lett.*, vol. 98, no. 14, pp. 1–3, Apr. 2011.
[35] G. Li, S. I. Morozov, Q. Zhang, Q. An, P. Zhai, and G. J. Snyder, "Enhanced strength through nanotwinning in the thermoelectric semiconductor InSb," *Phys. Rev. Lett.*, vol. 119, Nov. 2017, Art. no. 215503.
[36] *Version K-2015.06-SP1*, Synopsys Inc., Mountain View, CA, USA, 2017.
[37] *The International Technology Roadmap for Semiconductors (ITRS)*, 2017.
[38] M. A. Panzer *et al.*, "Thermal properties of ultrathin hafnium oxide gate dielectric films," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1269–1271, Dec. 2009.
[39] A. Yassine and R. Hijab, "Temperature dependence of gate current in ultra thin SiO_2 in direct-tunneling regime," in *Proc. IEEE Int. Integr. Rel. Workshop Final Report*, Lake Tahoe, CA, USA, 1997, pp. 56–61.