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# High-Performance ZnO Thin-Film Transistors on Flexible PET Substrates With a Maximum Process Temperature of 100 °C

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**ABSTRACT** In the present work, we testify a strategy to achieve high-performance ZnO thin film transistors (TFTs) on a flexible PET substrate at a maximum process temperature no more than 100 °C. Interestingly, the ZnO TFTs exhibit superior electrical properties, including a field-effect mobility of 14.32 $cm^2V^{-1}s^{-1}$, a sub-threshold swing of 0.21 V/decade, and an on-to-off current ratio of $3.03 \times 10^7$. Also, ideal uniformity, hysteresis property, contact resistance, and stability are achieved. Threshold voltage shift ($\Delta V_{TH}$) under positive and negative bias stress are 0.17 and −0.18 V, respectively. Moreover, the ZnO TFTs manifest good mechanical performance at a bending radius of 10 mm. We expect that our findings propel practical application of the oxide TFTs in flexible electronics.

**INDEX TERMS** Flexible electronics, low-temperature process, thin film transistors, ZnO.

## I. INTRODUCTION

During the past decade, rapid progress has been made in the field of flexible electronics, which drives development of novel applications such as electronic skin, wearable sensors, imperceptible implants, and flexible display [1]–[5]. These innovative applications have the potential to enhance our living quality, however, more stringent requirements are proposed to the electronic devices that they utilize. The electronic devices should not only have good electrical and mechanical performance, but also be portable, stretchable, and transparent [6]. Flexible oxide thin film transistors (TFTs) well meet all the above requirements [7]. Using low-temperature processes, the state-of-the-art oxide TFTs achieve a mobility higher than 10 $cm^2V^{-1}s^{-1}$ at a bending radius of 10 mm [8]. However, the oxide TFTs need to be subject to a post-annealing treatment at a temperature equal to or higher than 300 °C to optimize electrical properties and stability [9], [10], which limits the fabrication of them on cost-effective flexible substrates like PET, PEN, and PC [11], [12]. Thereby, it is urgently in need to develop process methods for fabricating the high-performance oxide TFTs at a low temperature.

Atomic layer deposition (ALD) process has been developed into a mature film-deposition method so far, since it combines the advantages of excellent large-area uniformity, atomic-level thickness controllability, and wonderful conformality [13]. In addition, ALD is applicable to deposit high-quality oxide semiconductor and insulation films at a low temperature (≤200 °C) [14], [15]. Therefore, variety of oxide TFTs based on the ALD process have been demonstrated such as ZnO TFTs, AlZnO (AZO) TFTs, GaZnO (GZO) TFTs, and InGaZnO (IGZO) TFTs, and performance of them is comparable or even surpasses to that of the oxide TFTs based on sputtering process [16]–[19].

In the present work, bottom gate ZnO TFTs are fabricated on a flexible PET substrate, where the ZnO active layer and $Al_2O_3$ dielectric are successively deposited by ALD. The maximum process temperature is set at 100 °C during the experiments. The ZnO TFTs exhibit ideal electrical performance, uniformity, hysteresis

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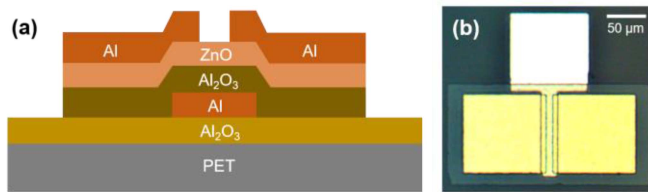


**FIGURE 1. (a) Schematic device structure of ZnO TFTs. (b) Top-view micrograph of ZnO TFTs. Feature size is W/L = 100 $\mu$m/10 $\mu$m.**

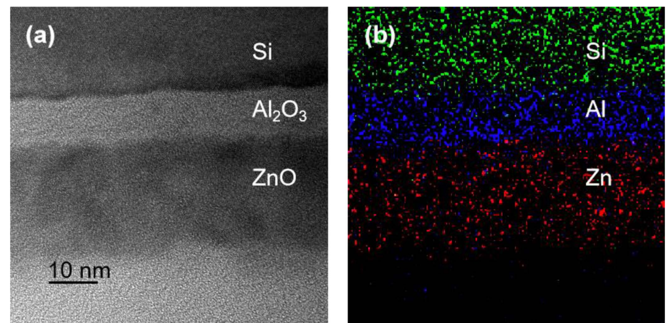


**FIGURE 2. (a) TEM image of ZnO/$Al_2O_3$ bilayer. Image resolution is 10 nm. There is no transition layer near interface. (b) EDX mapping of ZnO/$Al_2O_3$ bilayer. Green, blue, and red region represent for Si, Al, and Zn element, respectively. A sharp transition between Zn and Al element can be observed.**

property, bias stress stability as well as mechanical performance.

## II. EXPERIMENTAL SECTION

Schematic device structure of the ZnO TFTs is shown in Fig. 1(a), and detailed fabrication procedure is as follows. Firstly, a 10-nm $Al_2O_3$ buffer layer was deposited on a PET substrate by ALD at 100 °C. Then, a160-nm Al gate electrode was deposited by sputtering at room temperature. After this, a 30-nm $Al_2O_3$ dielectric and a 25-nm ZnO active layer were deposited by ALD at 100 °C in turn. Finally, a 120-nm Al source/drain electrode was deposited by sputtering at room temperature. Lithography and lift-off process were carried out to pattern the ZnO TFTs. Top-view micrograph of the ZnO TFTs is shown in Fig. 1(b).

During the ALD processes, trimethylaluminum, diethylzinc, and deionized water were utilized as precursors for Al, Zn, and O element, respectively. $N_2$ served as carrier and purge gases. Purge time was set as 25 s. During the sputtering processes, Al electrodes were deposited in Ar atmosphere with a pressure of 1 Pa and a power of 100 W.

Before we measured current-voltage (I-V) curves, the ZnO TFTs were subject to annealing treatment in vacuum at 100 °C for 1 h. I-V curves were measured in dark at room temperature using a semiconductor parameter analyzer (Agilent B1500A). The applied electric fields are fixed at 1 and -1 MV/cm, respectively, when we measured positive bias stress (PBS) and negative bias stress (NBS) stability. The stress time is 1000 s.

A ZnO/$Al_2O_3$ bilayer were deposited on a Si substrate using the same condition as the ZnO active layer and $Al_2O_3$ dielectric. Interface topography and film components of the ZnO/$Al_2O_3$ bilayer were explored by high-resolution transmission electron microscopy (TEM) and energy dispersive X-ray detector (EDX) measurement, respectively.

## III. RESULTS AND DISCUSSION

In order to gain an insight into interface topography of the ZnO/$Al_2O_3$ bilayer, high-resolution TEM measurement was performed, as shown in Fig. 2(a). Of note, there is no transition layer near the interface between the ZnO layer and $Al_2O_3$ layer. Besides, the ZnO layer exhibits polycrystalline lattice structure, while the $Al_2O_3$ layer exhibits amorphous microstructure.

To examine film component of the ZnO/$Al_2O_3$ bilayer, EDX measurement was performed, as shown in Fig. 2(b). It should be stressed that distribution region of Si, Al, and Zn element is quite clear, and a significantly sharp transition between Zn and Al element can be observed. The above TEM and EDX results demonstrate that high-quality interface between the ZnO active layer and $Al_2O_3$ dielectric can be formed by ALD process at a temperature of 100 °C.

Next, we focused on electrical performance of the ZnO TFTs. As shown in Fig. 3(a), the output curve exhibits distinct linear and saturation region. No current crowding effect occurs in the linear region. Saturation drain current ($I_D$) at drain voltage ($V_D$) = 5 V increases with gate voltage ($V_G$), thus the ZnO TFTs are enhancement mode devices. As shown in Fig. 3(b), transfer curves exhibit typical switch characteristic. According to the transfer curve with a $V_D$ of 0.1 V, we extracted electrical properties of the ZnO TFTs, including a field-effect mobility of 14.32 $cm^2V^{-1}s^{-1}$, a sub-threshold swing of 0.21 V/decade, and an on-to-off current ratio ($I_{ON}/I_{OFF}$) of $3.03 \times 10^7$.

To explore uniformity of the ZnO TFTs, we measured transfer curve of 15 individual devices. As shown in Fig. 3(c), all of the ZnO TFTs exhibit an off-state current ($I_{OFF}$) lower than 10 pA and an $I_{ON}/I_{OFF}$ larger than $10^7$. Sub-threshold region of the transfer curves highly overlaps with each other, implying high uniformity of the ZnO TFTs. Hysteresis curve of the ZnO TFTs is shown in Fig. 3(d). Threshold voltage ($V_{TH}$) variation between reverse and forward line is an extremely small value of 0.07 V, which reinforces the evidence of high-quality interface between the ZnO active layer and $Al_2O_3$ dielectric.

To study source/drain contact of the ZnO TFTs, transfer curves of the devices with different width/length ratio was measured, as shown in Fig. 4(a). The on-state current ($I_{ON}$) negatively correlates with channel length. Contact resistance ($R_{S/D}$) at the source/drain region was extracted using transfer line method (TLM). Total resistance ($R_T$) of the TFTs at on-state can be described as: $R_T = r_{ch}L + 2R_{S/D}$, where $r_{ch}$ is channel resistance per unit length, and L is channel length [20], [21]. Fig. 4(b) presents $R_T$ versus L at different $V_G$. By applying linear fitting, we calculated

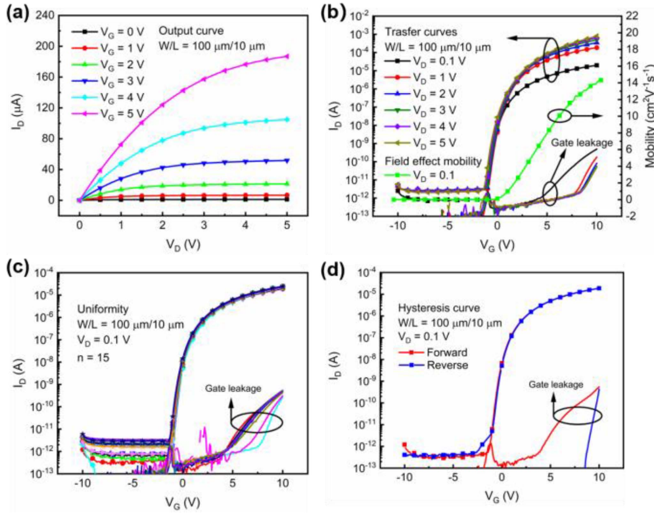


**FIGURE 3. (a) Output curve of ZnO TFTs. (b) Transfer curves and field-effect mobility of ZnO TFTs. (c) Uniformity of ZnO TFTs. n = 15. (d) Hysteresis curve of ZnO TFTs. W/L = 100 $\mu$m/10 $\mu$m. ZnO TFTs show preferable electrical performance.**

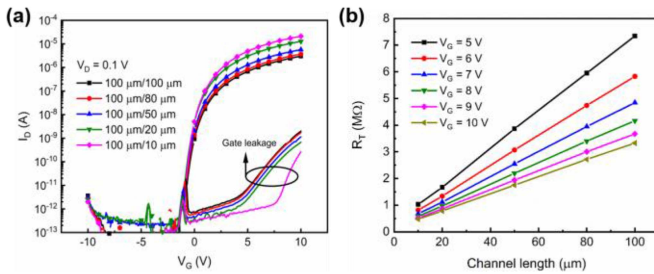


**FIGURE 4. (a) Transfer curves of ZnO TFTs with different width/length ratio. (b) $R_T$ versus L at different $V_G$. $R_{S/D} \times$ W is 0.75 k$\Omega \cdot$ cm, which indicates ideal ohmic contact between ZnO active layer and Al source/drain electrode.**

that the width-normalized contact resistance ($R_{S/D}$ × W) is 0.75 k$\Omega \cdot$ cm. The relatively small $R_{S/D}$ is attributed to the ideal ohmic contact between ZnO active layer and Al source/drain electrode.

To investigate stability of the ZnO TFTs, 1000 s PBS and NBS were applied to gate electrode, and the devices were measured every 200 s. As shown in Fig. 5(a) and 5(b), the transfer curves exhibit positive and negative parallel shift under PBS and NBS, respectively. Moreover, electrical properties of mobility, sub-threshold swing, and $I_{ON}/I_{OFF}$ show no degradation. Remarkably, threshold voltage shift ($\Delta V_{TH}$) is 0.17 under PBS, and is −0.18 V under NBS. Previous studies testified that $\Delta V_{TH}$ is caused by electron/hole trapping into the dielectric or at the interface between active layer and dielectric [22]. The ZnO TFTs keep stable in the measuring process, which indirectly verifies preferable insulation characteristics of $Al_2O_3$ dielectric and high-quality interface between ZnO active layer and $Al_2O_3$. To sum up, the electrical performance results manifest that low-temperature strategy which we proposed is effective for realizing ZnO TFTs with high performance and stability on flexible PET substrates.

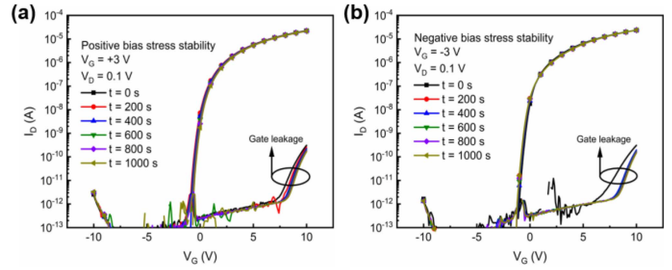


**FIGURE 5. (a) PBS stability of ZnO TFTs. (b) NBS stability of ZnO TFTs. Applied electric field are 1 and −1 MV/cm, respectively. Stress time is 1000 s. $\Delta V_{TH}$ is 0.17 and −0.18 V under PBS and NBS, respectively.**

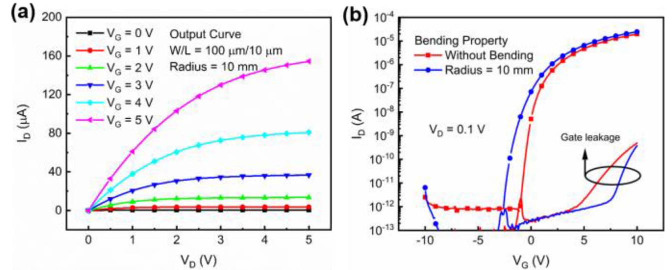


**FIGURE 6. (a) Output curve of ZnO TFTs at a bending radius of 10 mm. (b) Transfer curves of ZnO TFTs without and with bending. No serious degeneration occurs after the ZnO TFTs being bended.**

In the following section, tensile strain was applied on the ZnO TFTs, and the bending radius was set as 10 mm. Output curve of the ZnO TFTs with bending is shown in Fig. 6(a), the ZnO TFTs exhibit a lower saturation current than the ZnO TFTs without bending. Transfer curve of the ZnO TFTs with and without bending are shown in Fig. 6(b). We found that the transfer curve negatively shifts, and electrical properties are as follows: a field-effect mobility of 16.37 $cm^2V^{-1}s^{-1}$, a sub-threshold swing of 0.22 V/decade, and an $I_{ON}/I_{OFF}$ of $2.59 \times 10^7$. The reason for parameter variations is that atom distance of the ZnO active layer increases during bending [23], [24]. More electrons move to the anti-bonding state, therefore the channel conductivity increases. It is shown that no serious degeneration occurs. Consequently, the ZnO TFTs exhibit desirable bending property.

To comprehensively evaluate the ZnO TFTs, a comparison with previously reported flexible ZnO TFTs that based on ALD process is made. Parameters in terms of process temperature, bending radius, mobility, and sub-threshold swing are shown in Table 1. Compared with the previous works, our ZnO TFTs better combined electrical and mechanical performance.

## IV. CONCLUSION

A low-temperature strategy to fabricate high-performance ZnO TFTs on PET substrates is proposed in this work, and the maximum process temperature is set at 100 °C. We found that high-quality interface between the ZnO

**TABLE 1. Comparison of flexible ZnO TFTs based on ALD process.**

| Ref. | Process Temp. (℃) | Bending Radius (mm) | Mobility ($cm^2V^{-1}s^{-1}$) | Sub-threshold Swing (V/decade) |
|---|---|---|---|---|
| This Work | 100 | 10 | 14.32 | 0.21 |
| [25] | 150 | 12 | 20.9 | 0.91 |
| [26] | 140 | 3 | 13 | no data |
| [27] | 110 | 13 | 20.2 | 0.38 |
| [28] | 80 | no data | 8.40 | 0.142 |

active layer and $Al_2O_3$ dielectric was formed due to the successive deposition based on ALD process, which results in preferable uniformity, hysteresis property, stability, and mechanical performance of the ZnO TFTs. Notably, the ZnO TFTs exhibit superior electrical properties, including a field-effect mobility of 14.32 $cm^2V^{-1}s^{-1}$, a sub-threshold swing of 0.21 V/decade, an $I_{ON}/I_{OFF}$ of $3.03 \times 10^7$, and a $R_{S/D}$ of 0.75 kΩ · cm. Thereby, our work provides an effective method for the fabrication of high-performance oxide TFTs on cost-effective flexible substrates.

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