Foreword
Special Issue on Compact Modeling of Semiconductor Devices

THIS Special Issue is dedicated to recent research in the field of compact modeling of semiconductor devices. This is the first J-EDS Special Issue on compact modeling. In the last years, a number of new semiconductor device structures, for electronic and photonic applications, have been developed. Compact models are needed for the incorporation of these new devices in integrated circuits. Therefore, a Special Issue was needed to present recent compact modeling solutions for semiconductor devices

A total of 8 regular papers and 2 invited papers have been accepted in this Special Issue. All papers, including the invited ones, were subjected to a thorough peer reviewing. A high number of reviewers participated in this process. This has resulted in a Special Issue containing very high-quality papers.

The published papers target compact modeling aspects for a wide number of devices, such as SiGe HBTs, IGBTs, SiC SB diodes, LDMOSFETs, Multi-Gate MOSFETs, RRAMs, TFET SRAMs, and organic TFTs. Open source Verilog-A compiling is also targeted by one paper. Different operation regimes and conditions are addressed: charging/discharging, THz, high power, tunneling radiation environments, . . .

One invited paper, by U. Sharma and S. Mahapatra, addresses the modeling of HCD Kinetics for full VG/VD span under different experimental conditions across architectures and its SPICE implementation The other invited paper, by Fregonese *et al.*, presents a review of THz characterization and modeling of SiGE HBTs.

I would like to thank the work done by the rest of the Editors of this Special Issue and also by all the reviewers who participated in this process. And of course, I want to thank all the authors for their interest in submitting papers to this Special Issue. Thanks to authors, reviewers, and editors, this high-quality Special Issue has been possible.

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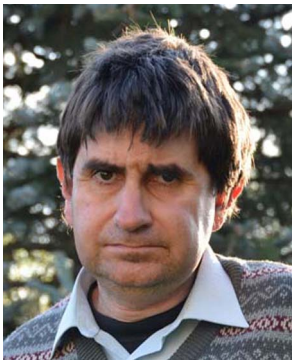


Benjamin Iñiguez (Fellow, IEEE) received the Ph.D. degree in physics from the Universitat de les Illes Balears in 1996. In February 2001, he joined the Department of Electronic, Electrical and Automatic Control Engineering, Universitat Rovira i Virgili, Tarragona, Spain, as a Titular Professor, where he became a Full Professor in February 2010. He led or is leading two research projects funded by the European Union. He has supervised 14 Ph.D. students, and co-supervised one more. He has published more than 170 research papers in international journals and more than 160 abstracts in proceedings of conferences. His main research interest is the compact modeling of emerging semiconductor devices, in particular nanoscale multigate MOSFETs GaN HEMTs, and organic and oxide TFTs. He obtained the Distinction from the Catalan Government for the Promotion of University Research in 2004 and the ICREA Academia Award (ICREA Institute) in 2009 and 2014.

Yogesh Singh Chauhan is a Professor with the Indian Institute of Technology Kanpur, India. He was with the Semiconductor Research and Development Center, IBM Bangalore from 2007 to 2010; the Tokyo Institute of Technology in 2010; the University of California at Berkeley from 2010 to 2012; and ST Microelectronics from 2003 to 2004. He is the Developer of several industry standard models: ASM-GaN-HEMT model, BSIM-BULK (formerly BSIM6), BSIM-CMG, BSIM-IMG, BSIM4, and BSIM-SOI models. His research group is involved in developing compact models for GaN transistors, FinFET, nanosheet/gate-all-around FETs, FDSOI transistors, negative capacitance FETs, and 2-D FETs. He has published more than 200 papers in international journals and conferences. His research interests are characterization, modeling, and simulation of semiconductor devices.

Prof. Chauhan received the Ramanujan Fellowship in 2012, the IBM Faculty Award in 2013, the P. K. Kelkar Fellowship in 2015, the CNR Rao Faculty Award, the Humboldt Fellowship, and the Swarnajayanti Fellowship in 2018. He has served on the technical program committees of IEEE International Electron Devices Meeting, IEEE International Conference on Simulation of Semiconductor Processes and Devices, IEEE European Solid-State Device Research Conference, IEEE Electron Devices Technology and Manufacturing, IEEE International Conference on VLSI Design, and IEEE International Conference on Embedded Systems. He is the Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES and a Distinguished Lecturer of the IEEE ELECTRON DEVICES SOCIETY. He is the member of the IEEE-EDS Compact Modeling Committee and a Fellow of the Indian National Young Academy of Science. He is the Founding Chairperson of the IEEE ELECTRON DEVICES SOCIETY U.P. Chapter and the Vice-Chairperson of IEEE U.P. Section.

Slobodan Mijalkovic (Senior Member, IEEE) received the graduate engineering, Magister, and Doctoral degrees from the Faculty of Electronics Engineering, University of Nis, Yugoslavia, in 1982, 1989, and 1991, respectively. From 1991 to 1998, he was with the Department of Microelectronics, Faculty of Electronics Engineering, University of Nis as an Assistant/Associate Professor of Physical Electronics. He also served as a Guest Researcher with the German National Center for Information Technology (GMD) in 1995 and 1996. From 1998 to 2007, he was a Principal Researcher with the Delft University of Technology, The Netherlands, where he has led a team for standardization of the Mextram bipolar transistor model with compact model coalition. Since 2007, he has been a Senior Research and Development Engineer with Silvaco Inc., responsible for all aspects of compact model development and implementation in Silvaco EDA tools. He is a member of the EDS Compact Modeling Technical Committee.

Kejun Xia (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Auburn University, Auburn, AL, USA, in 2006. After graduation, he joined Maxim Integrated, Beaverton, OR, USA, where he served as a Senior Principal Member of Technical Staff leading the modeling activities for the advanced BCD and SiGe BiCMOS technologies. From 2014 to 2015, he was with the Analog and Sensor BU, Freescale Semiconductor, Chandler, AZ, USA, as a Modeling Manager, where he expanded his experience to modeling ESD, reliability, MEMS, and product behavior model. From 2016 to 2019, he managed a device and product modeling team for NXP Semiconductors, Chandler, where he currently manages a High Voltage and Analog Technology Development Team. He has published many technical papers in renowned journals and conferences. His research interests include device physics, process, compact modeling, and model and its interaction with analog circuits. He has been a frequent reviewer for IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE ELECTRON DEVICE LETTERS, and *Solid-State Electronics*. He has served as a Guest Editor for IEEE TED and JEDS special issues. He has been on the technical program committees for the IEEE EDTM conference. He is a member of the IEEE Compact Modeling Committee.

Jung-Suk Goo was born in Seoul, South Korea, in 1966. He received the B.S. degree in electrical engineering from Yonsei University, Seoul, in 1988, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1997 and 2001, respectively.

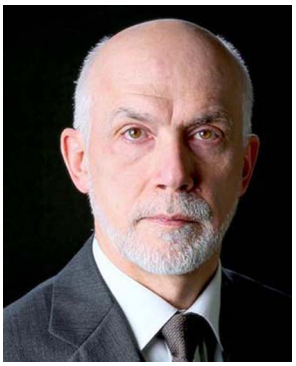
He is currently the Senior Manager with the Passive and Advanced Modeling Group, GLOBALFOUNDRIES. While he has spent his entire career in the industry, he has been deeply involved in research societies all the time. He has authored and coauthored 55 technical papers in international journals and conferences, including four invited papers, across a wide variety of technical topics, such as radio-frequency circuit design, semiconductor devices, reliability, characterization, simulation, and modeling. He also holds 38 U.S. patents. In recognition of his work in achieving the world-record lowest noise CMOS low-noise amplifier design, he was listed in Maquis "Who's Who in Science and Engineering" and "Who's Who in America" as a renowned engineer. Additionally, he was the Chair of the SRC Technical Advisory Board for Compact Modeling Research for three years and a member of the SRC Technical Advisory Board for Analog/Mixed-Signal Devices Research for ten years. Since 1997, he has been a journal reviewer for IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON NANOTECHNOLOGY, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, *Solid-State Electronics*, and *IEE Proceedings Circuits, Devices and Systems*. He was also on "The Golden Reviewers List" of the IEEE Electron Device Society for five years in a row. He is currently a member of the IEEE EDS Compact Modeling Committee and Berkeley Device Modeling Center Advisory Board.

Marcelo Antonio Pavanello (Senior Member, IEEE) received the electrical engineering degree from FEI University in 1993, and the M.Sc. and Ph.D. degrees in electrical engineering (microelectronics) from the University of São Paulo, Brazil, in 1996 and 2000, respectively.

From August to December 1998, he was with the Laboratoire de Microélectronique, Université Catholique de Louvain (UCL), Belgium, working in the fabrication and electrical characterization of novel channel-engineered silicon-on-insulator (SOI) transistors. From 2000 to 2002, he was with the Center of Semiconductor Components and Nanotechnologies, State University of Campinas, Brazil, where he worked as a Postdoctoral Researcher with the development of a CMOS n-well process. In 2003, he joined FEI University, where he is currently a Full Professor with the Electrical Engineering Department. Since 2008, he has been with UCL as a Visiting Professor. From 2010 to 2020, he also served as the Vice-Rector for Teaching and Research with FEI. He has authored or coauthored more than 400 technical papers in peer-reviewed journals and conferences, and is an author/editor of six books. He coordinates several research projects fomented by Brazilian agencies like FAPESP, CNPq, and Capes. He also supervised several Ph.D. dissertations, M.Sc. thesis, and undergraduate projects in electrical engineering. His current interests are the compact modeling, fabrication, electrical characterization, and simulation of SOI CMOS transistors with multiple gate configurations and silicon nanowires; the wide temperature range of operation of semiconductor devices; and the digital and analog operation of novel channel-engineered SOI devices and circuits.

Prof. Pavanello received the Award "Instituto de Engenharia" given for the best student among all the modalities of engineering programs offered at FEI. He is also a Researcher associated to the National Council for Scientific Development (CNPq), Brazil. Since 2007, he has been serving as an IEEE Electron Devices Society (EDS) Distinguished Lecturer and has been nominated to the Compact Modeling Technical Committee of EDS in 2018. Since 2019, he has been assigned as an Editor for Process and Device Modeling of IEEE TRANSACTIONS ON ELECTRON DEVICES. He is a Senior Member of the Brazilian Microelectronics Society.

Marek Mierzwinski received the B.S. degree in engineering physics from Cornell University and the master's and Ph.D. degrees in electrical engineering from Stanford University. He is a Research and Development Engineer with Keysight Technologies, responsible for compact device models for their commercial circuit simulators. He started at Hewlett Packard as a Product Engineer in the fab, then a Research and Development Project Manager responsible for their first modulation doped FET IC. He later moved to the EEsof Division and was a Research and Development Project Manager for the analog circuit simulator. In 2002, he co-founded Tiburon Design Automation, which developed the industry's first Verilog-A compiler that could be used by different commercial simulators.



Wladek Grabinski received the Ph.D. degree from the Institute of Electron Technology, Warsaw, in 1991. From 1991 to 1998, he was with IIS, ETHZ, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPFL, and was engaged in the compact model developments. Later, he was a Technical Staff Engineer with Motorola/Freescale Geneva Modeling Center. He is currently consulting for modeling, characterization, Verilog-A standardization, and parameter extraction of nanoscaled MOST for the design of RF CMOS ICs. He is an Editor of the reference modeling book *Transistor Level Modeling for Analog/RF IC Design* and also coauthored more than 70 papers. He is a member of ESSDERC TPC Track4: "Device and Circuit Compact Modeling" and the IEEE EDS Compact Modeling Technical Committee. He is involved in activities of the MOS-AK Association and has been serving as a Coordinating Manager since 1999.