Foreword
Special Issue From the Selected Extended Papers Presented at EDTM 2020

THIS Special Issue is assembled from a selection of highly-rated technical papers presented at the 4th *IEEE Electron Devices Technology and Manufacturing Conference* 2020, EDTM 2020. It took place during April 6-21, 2020 and signified the 1st of its kind as a virtual conference financially-sponsored by the *Electron Devices Society* (EDS). The original EDTM 2020 was planned as a full three-day event at the *Hotel Equatorial*, Penang, Malaysia from March 16 to 18, 2020. However, due to the COVID-19 pandemic, EDTM 2020 was held as a *virtual event*.

The EDTM 2020 virtual event featured a technical program of 182 papers in all areas of electron devices technology and manufacturing including materials, processes and tools, devices, modeling and simulation, reliability, manufacturing and yield, and packaging and heterogeneous integration. They were given by the very best experts, along with young scientists and engineers in the field of electron devices technology and manufacturing from 27 different countries worldwide. There were *six* Plenary talks offered by internationally recognized technical leaders from industry and academia. In addition there were presentations from 13 sponsors and *one* exhibitor as well as *four* local (Penang) high school student Posters.

In this special issue, the extended versions of the 25 top-rated papers presented at the EDTM 2020 are published following a process of rigorous review by the *Journal of Electron Devices Society* (J-EDS) reviewers as per IEEE publication policy.

The first *three* papers describe different aspects of silicon carbide (SiC) based device technology and modeling. The *first* paper, "Third Generation PRESiCE Technology for Manufacturing SiC Power Devices in a 6-inch Commercial Foundry," by Baliga from North Carolina State University, USA, reports the process qualification of third-generation PRESiCE™ technology for manufacturing 1.2 kV SiC power devices, such as junction-barrier controlled Schottky (JBS) diodes, metal-oxide-semiconductor field-effect transistor (MOSFET) power devices, and junction-barrier Schottky field-effect transistor (JBSFET) in a commercial foundry using *six*-inch wafers. The author demonstrated good yield and excellent parametric distributions in inter- and intra-wafer lots using test structures fabricated in commercially available products. The *second* paper "Performance Modeling of Silicon Carbide Photoconductive Switches for High-Power and High-Frequency Applications," by Rakheja, Huang, and Riege *et al*. from the University of Illinois, New York University, and Lawrence Livermore National Laboratories, USA, respectively, presents a theoretical study on the performance of SiC-based photoconductive semiconductor switches (PCSS) using coupled electrical and optical simulation along with a physics-based analytical model for accurate modeling of PCSS. It is shown that with proper optimization of the operating and design conditions, the output power density of 4H-SiC-based PCSS can be significantly improved by increasing the optical generation rate and using a thicker SiC layer to improve the absorption characteristics of SiC. The *third* paper, "Charge Sheet Super Junction in 4H-Silicon Carbide: Practicability, Modeling and Design," by Akshay *et al.*, Indian Institute of Technology Madras, India, reports the theory, modeling, and design of a charge sheet super-junction (CSSJ) transistor and shows the advantages of CSSJ over the conventional super-junction (SJ) in 4H-SiC material. It is shown that in 4H-SiC, CSSJ offers a simpler fabrication process, lower charge imbalance, and lower specific ON resistance for a given breakdown voltage compared to SJ. Furthermore, the paper presents that CSSJ in SiC is over 10 times less sensitive to charge imbalance than in Si, thus providing a great future device option.

The next *two* papers report high electron mobility transistor (HEMT) power devices. The *first,* "Quasi-Normally-Off AlGaN/GaN HEMTs with SiN_x Stress Liner and Comb Gate for Power Electronics Applications," by Cheng *et al.*, Southern University of Science and Technology, China in collaboration with Chan, Hong Kong University of Science and Technology, presents recess-free quasi-normally-off AlGaN/GaN HEMTs with threshold voltage of 0.24 V using local control of two-dimensional electron gas (2DEG) density using a SiN_x stress liner in the gate region of the channel. It is shown that the comb structure they used suppresses the short channel effects. The authors presented superior electrostatic performance of the quasi-normally-off GaN HEMT devices compared to the normally-off commercial p-GaN HEMTs as well as published data, thus demonstrating the potential for strain engineering to achieve normally-off GaN HEMTs. The *second* paper, "Efficient Modeling of Barrier Resistance for an Improved Lumped Element Model of GaN-based MIS-HEMT Gate Stack," by Rai, Saha, and Ganguly, Indian Institute of Technology, Bombay and Mahajan, Vellore Institute of Technology, India, presents accurate modeling of the gate stack of GaN based metal-insulator-semiconductor HEMTs (MIS-HEMTs). Here, the authors accounted for the border

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trap admittance and the energy distribution of the interface trap capture cross section to achieve close agreement between simulation and measurements. They concluded that the conventional small-signal admittance method cannot be used to extract the interface trap density, and that it is critical that non-ideal effects be incorporated in the equivalent circuit models of GaN-based MIS-HEMTs.

The next *two* papers describe the design and performance of semiconductor devices built with emerging materials systems. The *first* paper, "Effect of Nanostructure on Carrier Transport Mechanism of III-Nitride and Kesterite Solar Cells: A Computational Analysis," by Routray, Pradhan, and Mishra, from the SRM Institute of Science and Technology, Kattankulathur, Indian Institute of Information Technology Design and Manufacturing, Kancheepuram, and the National Institute of Technology, Raipur, India, respectively, presents a comparative study of III-Nitride (GaN/InGaN) and Kesterite material-based nanostructure solar cells. The authors analyze the influence of stress-induced polarization charges in III-nitride and the effect of inherent defects in Kesterite materials on carrier transport mechanisms in nanostructure solar cells. Using computational analysis, it is shown that the performance of solar cells depends on carrier recovery and transport from the nanostructures as well as device engineering. The *second* paper, "Indium Silicon Oxide TFT Fully Photolithographically Processed for Circuit Integration," by Yao, *et al.*, from the University of Cambridge, U.K., Ma from the Suzhou Institute of Biomedical Engineering and Technology, Chinese Academy of Sciences, China, and Nathan from Darwin College, University of Cambridge, U.K., presents silicon-oxide-doped indium oxide (In_2O_3:SiO_2) amorphous semiconductor thin-film transistors (TFTs) fabricated using a fully photolithographic process at sub-200°C achieving full compatibility for integration on plastic substrates to realize flexible TFT integrated circuits (ICs). The report shows excellent electrostatic characteristics of the TFTs and reliable stability behavior under electrical bias stress as well as negative bias illumination stress, along with a pulse-based compensation solution for persistent photoconductivity arising from the latter. In addition, the authors present design considerations of a fully integrated TFT voltage amplifier circuit using extracted values of device parameters of fabricated transistors.

The next *four* papers present different aspects of modeling and characterization of emerging field-effect transistors (FETs). The *first* paper, "Compact Modeling of Surface Potential, Drain Current and Terminal Charges in Negative Capacitance Nanosheet FET including Quasi-Ballistic Transport," by Gaidhane *et al.*, Indian Institute of Technology, Kanpur, India and Pahwa *et al.*, University of California, Berkeley, USA reports a compact model for negative capacitance (NC) nanosheet (NS) FETs (NC-NSFETs) using drift-diffusion and quasi-ballistic transport formulation that is applicable to sub-7 nm technology node. The drain current model offers thickness dependence of ferroelectric material and channel length dependence of NC-NSFET devices. Using the core model, the authors, also, developed models for terminal and inner fringing charges, and validated the model with numerical device simulation, subsequently implementing it in Verilog-A code for circuit analysis. Also, the application of the model is demonstrated on NC-NSFET based CMOS inverter and SRAM circuits. The *second paper*, "Compact Modeling of Multi-layered MoS_2 FETs including Negative Capacitance Effect," by Nandan *et al*. and Yadav, from the Indian Institute of Technology, Kanpur and National Institute of Technology, Calicut, India, respectively, and Toral-Lopez *et al*. from the University of Granada, Spain, reports a surface potential based compact drain current model with NC effect for multilayer molybdenum disulfide (MoS_2) channel in symmetric double gate (DG) FET devices. The authors validated their channel thickness-dependent baseline current and negative capacitance models with the numerical simulation data for mono- to penta-layer MoS_2 channel DG-FETs. The *third* paper, "Comparison of LER Induced Mismatch in NWFET and NSFET for 5-nm CMOS," by Jha *et al.* and Vega from the Indian Institute of Technology, New Delhi, India and IBM Research, New York, USA, respectively, analyses the impact of three-dimensional (3D) line-edge roughness (LER) on the electrical characteristics of NSFETs and nanowire FETs (NWFETs) for sub-7 nm technology nodes. A two-dimensional (2D) auto covariance function (ACVF) with two degrees of freedom is used to generate a 3D-LER profile along the sidewalls and top and bottom surfaces of the FETs. It is shown that the NSFETs appear to be immune to on-current mismatch compared to NWFETs, although the latter show lower mismatch in drain-induced barrier lowering (DIBL) and subthreshold swing (SS). The *fourth* paper "Impact of Interface Traps on Negative Capacitance Transistor: Device and Circuit Reliability," by Prakash *et al*. and Amrouch from the Karlsruhe Institute of Technology and the University of Stuttgart, Germany, respectively, and Gupta *et al.* from the Indian Institute of Technology, Kanpur, India reports the impact of Si-SiO_2 interface traps on the reliability of NC transistors and circuits using a physics-based NC model. The model is implemented in the industry standard BSIM-CMG compact FinFET model. It is shown that the amplified electric field across the SiO_2 layer within p-channel FinFET (pFinFET) increases the interface trap concentration due to NC effect causing higher degradation in the NC-pFinFET reliability compared to that of a conventional pFinFET operated at the same nominal supply voltage. However, at the same interface trap concentration, the NC-pFinFET exhibits lower degradation than the baseline pFinFET due to the superior electrostatic integrity of NC-pFinFET.

The next *two* papers are in the domain of high frequency and related device modeling and simulation. The *first* is the paper, "Heterostructure Ge-Body pTFETs for Analog/RF Applications," with contributions from Ghosh, Sarkar, and Koley, Jadavpur University, India, and Saha from Prospicient Devices, USA. The paper examines the analog/RF performance of staggered heterostructure Ge-pTFET devices compared with the all Ge pTFET counterparts with Ge source and body. Through simulation they assessed the static and dynamic characteristics of different device structures with Ge body and $GeSi_{1-x}Ge_x$, $In_{1-x}Al_xAs$, and $GaAs_xP_{1-x}$ sources, and extracted their relevant small

signal parameters for performance comparison. The *second* paper, "A CMOS Low Power Current Source Tunable Inductor with 80% Tuning Range for RFIC," by Mariappan and Rajendran *et al.*, University Science Malaysia and Rustagi *et al.*, SilTerra Malaysia signifies a collaborative effort between academia and industry on development of a novel low power architectural solution for tuning the inductor impedance for CMOS radio frequency ICs. The tunable inductor comprising a common source transistor, stabilizer resistor and coupling capacitor is capable of increasing the physical inductance value up to 80%, contributing to an area reduction by as much as 52% at 2.5 GHz, and is resilient to process variations, hence boosting the manufacturing yield.

Next *four* papers represent the *sensing device technology* for Internet of Things (IoT) to enabling smart environments and integrated ecosystems. The *first* paper, "Printable Low Power Organic Transistor Technology for Customizable Hybrid Integration Towards Internet of Everything," by Huang and Guo *et al.*, based on a collaborative effort between academia and industry in China namely Shanghai Jiao Tong University, LinkZill Technology Co. Ltd. and the Shanghai Aerospace Electronic Technology Institute, reports on heterogeneous integration of organic field effect transistor electronics with silicon IC for applications encompassing the broader Internet of everything (IoE) space. The transducer as well as sensor interface is a field effect transistor based on organic materials to enable flexible, conformable, and large area coverage; and the silicon IC chip to perform the obvious needs of signal acquisition, processing, and transmission. The work highlights an economic solution for diverse customized sensor applications. Continuing along the same theme of sensors, the *next* paper, "Multilayer CVD-Graphene and MoS_2 Ethanol Sensing and Characterization using Kretschmann-based SPR," signifies the result of an international collaborative effort between Menon and Burhanuddin *et al.*, Institute of Microengineering and Nanoelectronics (IMEN), National University of Malaysia, Hewak and Huang, Optoelectronics Research Centre, University of Southampton, U.K., and Mishra, Srinivasan, and Bhat, Centre for Nanoscience and Engineering (CeNSE), Indian Institute of Science, India. Using a combination of numerical and experimental routes, the paper examines ethanol detection using a Kretschmann-based surface plasmon resonance (K-SPR) sensor using multilayer graphene and MoS_2 structures on a plasmonic gold layer. The *third* paper, "Subthreshold Operation of Photodiode-Gated Transistors Enabling High-Gain Optical Sensing and Imaging Applications," by Wang *et al.* from the Sun Yat-Sen University, Guangzhou, China and Hu from the University of Electronic Science and Technology of China, Zhongshan Institute, Zhongshan, China, presents the device architecture and performance of high gain and high sensitivity optical sensors achieved through subthreshold operation of photodiode-gated TFTs. The *fourth* paper, "Under-FET Thermal Sensor Enabling Smart Full-Chip Run-Time Thermal Management," by Li *et al.* from the University of California Riverside, USA, reports the design, fabrication, and analysis of a novel under-FET in-hole thermal sensor diode structure fabricated in a CMOS process. This under-FET temperature sensor enables smart full-chip runtime thermal management with spatial resolution down to single transistor level. The authors demonstrate the new chip-level thermal management technique using a prototype power amplifier IC fabricated using 40 nm CMOS.

The next *two* papers describe the performance of emerging random access memory (RAM) devices. The *first* paper, "Analysis of Switching under Fixed Voltage and Fixed current in Perpendicular STT-MRAM," by Fiorentini *et al.*, Institute for Microelectronics, TU Vienna, Austria and Goes *et al.*, Silvaco Europe Ltd, Cambridge, U.K., presents a comparative analysis of the switching time of spin-transfer torque (STT) magnetoresistive RAM (STT-MRAM) computed by a fixed voltage across the magnetic tunnel junction (MTJ) and fixed current and fixed current density applied to MTJ. It is shown that a correction to the fixed current is required to accurately reproduce the switching time distribution in STT-MRAMs for a broad range of tunneling magnetoresistance ratio depending on the ambient temperature, size of the MTJ structure as well as its resistance. The *next* paper of the group, "A Unified Memory and Hardware Security Module based on the Adjustable Switching Window of Resistive Memory," by Lin *et al.*, Tsinghua University, Beijing, China, reports a tri-functional module using resistive RAM (RRAM) for lightweight hardware protection by a two-phase forming process to generate and store physically unclonable function (PUF) ID on the switching window. It is demonstrated that since the PUF ID is stored by the switching window, and PUF cells can be written to low resistance state and high resistance state, hence can be used as a true random number generator (TRNG) and memory.

Next *two* papers describe the design, fabrication, and application of neural networks (NNs). The *first* paper, "Generation of STDP with Non-Volatile Tunnel-FET Memory for Large-Scale and Low-Power Spiking Neural Networks," by Kino *et al.*, Tohoku University, Japan, reports on design, fabrication, and characterization of low power spiking NNs using non-volatile tunnel-field-effect-transistor memory and demonstrates the spike-timing-dependent plasticity (STDP) of a biological synapse. The *second* paper, "Neural Network Based Design Optimization of 14-nm Node Fully-Depleted SOI FET for SoC and 3DIC Applications," by Baek *et al.*, Pohang University of Science and Technology, Korea, describes the machine learning method of NNs to optimize fully-depleted (FD) silicon-on-insulator (SOI) FET structures. The aim is to achieve high on/off current ratio for high performance, low operating power, and low stand-by power System-on-Chip (SoC), and sequential 3D-IC realization at the 14 nm node conventional FDSOI FETs technology.

The final *four* papers of this *Special Issue* present the reliability physics, built-in reliability design, and on-chip protection of very large scale integrated (VLSI) circuits and systems. The *first* paper, "Modeling of DC - AC NBTI Stress - Recovery Time Kinetics in P-Channel Planar Bulk and FDSOI MOSFETs and FinFETs," by Choudhury *et al.*, Indian Institute of Technology, Bombay, India, reviews the physics-based bias temperature instability (BTI) analysis tool (BAT) used to model the time kinetics of threshold voltage shift

(ΔVT) during and after negative BTI (NBTI) in p-channel planar bulk and FDSOI MOSFETs and SOI FinFETs. The paper describes the physical mechanisms and modeling techniques of BAT frame work including the uncorrelated contributions from the trap generation at the channel/gate-insulator interface and in gate insulator and hole trapping in pre-existing gate insulator traps. The *next* paper, "3D TCAD Analysis Enabling ESD Layout Design Optimization," by Pan *et al.*, University of California, Riverside, USA, presents a comparative analysis of the optimization of electrostatic discharge (ESD) layout design using 2D and 3D technology computer aided design (TCAD) tools for simulation of ESD protection diodes of a 55 nm CMOS technology. It is shown that 3D-TCAD offers accurate simulation of geometrical effects and thus, provides useful ESD layout design guidelines for the optimization and prediction of ESD protection in IC devices and chips. The *third* paper "Pad-Based CDM ESD Protection Methods Are Faulty," by Di *et al.*, University of California Riverside, USA, discusses the challenges of charged device model (CDM) ESD protection scheme for the reliability of a packaged IC-chip where the central ESD block is achieved by a pad-based protection network connected to all pads on the chip. The paper highlights the potential root cause of the randomness and uncertainty of pad-based CDM ESD protection designs and emphasizes the critical need for new CDM ESD protection solution. The *final* paper of this Special Issue, "Understanding and Improving Reliability for Wafer Level Chip Scale Package: A Study Based on 45nm RFSOI Technology for 5G Applications," by Zhuo-Jie *et al.*, Globalfoundries, USA, reports a comprehensive reliability study of wafer level chip scale package (WLSCP) using 45 nm RFSOI technology for 5G RF applications. It is shown that the WLSCP reliability can be significantly improved by comprehensive testing, deep understanding of the failure mechanisms, and co-optimization of design and process in implementing board and interconnects for 5G applications.

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SAMAR K. SAHA, *Guest Editor*
Department of Exploratory Device Research
Prospicient Devices
Milpitas, CA 95035 USA
(e-mail: samar@ieee.org)

AROKIA NATHAN, *Guest Editor*
Darwin College
University of Cambridge
Cambridge CB3 9EU, U.K.
(e-mail: an299@cam.ac.uk)

P. SUSTHITHA MENON, *Guest Editor*
Institute of Microengineering and Nanoelectronics
Universiti Kebangsaan Malaysia
Bangi 43600, Malaysia
(e-mail: susi@ukm.edu.my)

JAGADHESWARAN RAJENDRAN, *Guest Editor*
Collaborative Microelectronic Design Excellence Centre
Universiti Sains Malaysia (Sains@USM)
Pulau Pinang 11900, Malaysia
(e-mail: jaga.rajendran@usm.my)

ASRULNIZAM BIN ABD MANAF, *Guest Editor*
Collaborative Microelectronic Design Excellence Centre
Universiti Sains Malaysia (Sains@USM)
Pulau Pinang 11900, Malaysia
(e-mail: eeasrulnizam@usm.my)

LEONG WAI YIE, *Guest Editor*
Faculty of Engineering and Information Technology
MAHSA University
Jenjarom 42610, Malaysia
(e-mail: waiyie@gmail.com)

Samar K. Saha (Fellow, IEEE) has authored over 100 research papers; two books, titled, *FinFET Devices for VLSI Circuits and Systems* (Boca Raton, FL, USA: CRC Press, 2020) and *Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond* (Boca Raton, FL, USA: CRC Press, 2015); one book chapter on Technology Computer-Aided Design; and holds 12 U.S. patents. He served as the 2016–2017 President of the IEEE Electron Devices Society (EDS), and is currently serving as the Senior Past President of EDS. He is the Chief Scientist with Prospicient Devices, USA, and an Adjunct Faculty with the Electrical Engineering Department, Santa Clara University, USA.

Arokia Nathan (Fellow, IEEE) received the Ph.D. degree in electrical engineering from the University of Alberta, Canada, in 1988. He is a leading pioneer in the development and application of thin-film transistor technologies to flexible electronics, display, and sensor systems. He joined LSI Logic USA and subsequently the Institute of Quantum Electronics, ETH Zürich, Switzerland, before joining the Electrical and Computer Engineering Department, University of Waterloo, Canada. In 2006, he joined the London Centre for Nanotechnology, University College London as the Sumitomo Chair of Nanotechnology. He moved to Cambridge University in 2011 as the Chair of Photonic Systems and Displays, and he is currently a Bye-Fellow and a Tutor with Darwin College. He has over 600 publications, including four books, and more than 110 patents and four spin-off companies. He is a recipient of the 2020 IEEE EDS J. J. Ebers Award. He is an IEEE/EDS Distinguished Lecturer, a Chartered Engineer in U.K., and a Fellow of the Institution of Engineering and Technology, U.K.

P. Susthitha Menon (Senior Member, IEEE) received the B.Eng. degree (Hons.) and the Ph.D. degree (with Distinction) in optoelectronics specializing in Si/InGaAs/InP photodiodes from the National University of Malaysia (UKM) in 1998 and 2008, respectively. She has been an Associate Professor with the Institute of Microengineering and Nanoelectronics, UKM, since 2009. She worked with Intel Malaysia from 1999 to 2002 as a Product Engineer for mobile modules and motherboard systems. She has authored more than 100 peer-reviewed journals in plasmonics/nanophotonics, optoelectronic devices/biosensors/imaging, and engineering optimization. She is currently the 2019–2021 Vice Chair of the Region 10 IEEE EDS Subcommittee for Regions/Chapters and the 2017–2018 Chair of the IEEE EDS Malaysia Chapter.

Jagadheswaran Rajendran (Senior Member, IEEE) is currently a Senior Lecturer with the Collaborative Microelectronic Design Excellence Centre, Universiti Sains Malaysia. He has coauthored more than 40 articles and holds one U.S. patent. His research interests include CMOS analog IC design, CMOS radio-frequency IC design, and monolithic microwave integrated circuit design. He was the recipient of the IEEE Circuit and Systems Outstanding Doctoral Dissertation Award in 2015. He served as the Chairman of the IEEE EDS/MTT/SSC Penang Chapter in 2011 and 2018.

Asrulnizam Bin Abd Manaf (Senior Member, IEEE) received the Ph.D. degree in engineering from the School of Fundamental Science and Technology, Keio University, Japan, in 2009. He is an Associate Professor and the Deputy Director with the Collaborative Microelectronic Design Excellence Center (CEDEC), Universiti Sains Malaysia. He is a Leader of the CMOS-based sensing interface integrated circuitry, microfluidic based-MEMS/NEMS and printable-based devices technology group with CEDEC. He has authored and coauthored 60 international technical journals or conference papers. His research interest has been in the areas of microfluidic-based devices, CMOS sensing interface integrated circuitry, heterogeneous integration, micro 3-D grayscale technology, MEMS/NEMS fabrication technology, printable electronics, and wearable electronics. He received the IETE J. C. Bose Memorial Award for the best engineering-oriented paper in 2017.

Leong Wai Yie is currently the Chairperson of the Institution of Engineering and Technology (Malaysia Local Network), the Vice President of the Institution of Engineers Malaysia (IEM), and the Committee Member of World Federation of Engineering Organization (Women in Engineering Committee). She is the Chief Editor of IEM and an Editor of IET. She is specialized in medical signal processing and telecommunications research and has been successfully attracting research and development investment from businesses. She has received the Ten Outstanding Young Malaysian 2017 Award, the Top Research Scientists Malaysia in 2017, the ASEAN Meritorious Service Award in 2017, the IEM Best Paper Award in 2015, the Richard Jago Research Prize in 2004, and the Trailblazer Innovation Award in Australia in 2005.