Received 3 August 2020; revised 22 September 2020; accepted 11 October 2020. Date of publication 26 October 2020;
date of current version 10 November 2020. The review of this article was arranged by Editor S. Reggiani.

*Digital Object Identifier 10.1109/JEDS.2020.3032649*

# Simulative Researching of a 1200V SiC Trench MOSFET With an Enhanced Vertical RESURF Effect

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This work was supported in part by the Natural Science Foundation Project of CQ CSTC under Grant cstc2020jcyj-msxmX0243; in part by the Science and Technology on Analogue Integrated Circuit Laboratory under Grant 6142802180508; and in part by the Fundamental Research Funds for the Central Universities under Grant 2020CDJ-LHZZ-024.

**ABSTRACT** A SiC trench MOSFET with an enhanced vertical RESURF effect is proposed and analyzed in this article. The device features a deep oxide trench surrounded by a P-type doping layer at the source-side. With the assistant depletion effect of the P-type layer, the concentration of the N-drift region is increased and the specific on-resistance ($R_{on,sp}$) is thus reduced. The P-type doping can significantly reduce the intensity of the electric field at the gate oxide corner, and modulate the bulk electric field for the device. The breakdown voltage ($BV$) is therefore improved. As a result, the proposed SiC MOSFET has a better trade-off of BV and $R_{on,sp}$. The $R_{on,sp}$ decreases by 59% and the $BV$ increases by 16% for the proposed device without a CSL layer compared with the conventional trench MOSFET with a CSL layer. Meanwhile, the device exhibits a lower gate-to-drain charge ($Q_{gd}$) which is reduced by 52% and the switching loss is also reduced by 19%.

**INDEX TERMS** Silicon carbide, bulk electric field, breakdown voltage, specific on-resistance, gate-to-drain charge, switching loss.

## I. INTRODUCTION

In recent years, the wide-bandgap material silicon carbide (SiC) has been widely used in semiconductor power devices because of its basic characteristics, and SiC MOSFET is one of the major devices in power systems [1]–[3]. In order to optimize the trade-off relationship between the breakdown voltage ($BV$) and specific on-resistance ($R_{on,sp}$), some technologies have been successfully developed in SiC MOSFET products. The trench structure is employed to reduce $R_{on,sp}$ by eliminating JFET resistance [4]–[6]. It is well know that the high electric field at the corner of trench influences the BV of the SiC trench MOSFETs [7], [8]. Once the maximum electric field peak in SiC at the position reaches to the critical electric field, breakdown occurs. In addition, the high electric field in semiconductor will affect the endurance of the gate oxide material and lead to hot carrier effects at the bottom corner of the gate oxide, and P+ shielding layer structure under the oxide trench has been proposed [9]–[13]. Reduced surface field (RESURF) technology which has been widely used in silicon transverse power devices, makes the epitaxial layer depleted before the electric field in the lateral junction reaches the critical breakdown electric field, thus increases the BV [14], [15]. RESURF effect is drawing more and more attention in the usage of SiC power devices, and needs more development for the SiC MOSFET.

A novel SiC trench MOSFET with a vertical RESURF structure (V-RESURF TMOS) has been researched. The vertical RESURF is caused by a oxide trench on the source side and the surrounding P-type layer, which can further reduce the electric field at the corners of gate oxide trench as to improve $BV$ and reduce $R_{on,sp}$. In addition, resulting from the lower gate-to-drain charge ($Q_{gd}$), the switching loss is also decreased. The static and dynamic characteristics of the proposed device are investigated by numerical simulation.

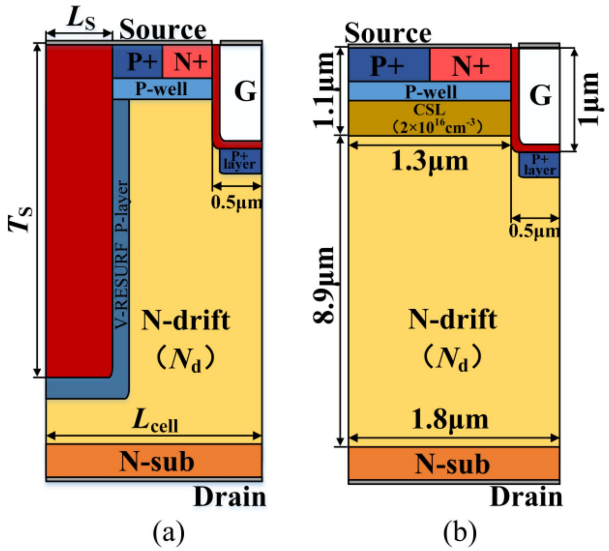


**FIGURE 1.** Cross-sectional structures of (a) the proposed vertical RESURF trench MOSFET (V-RESURF TMOS), (b) the conventional trench MOSFET (C-TMOS).

## II. DEVICE STRUCTURE AND MECHANISM

Fig. 1 shows the view cross-section of the proposed V-RESURF TMOS and the conventional trench MOSFET (C-TMOS). The P+ shielding layer under the oxide trench of both devices is used to relieve the electric field of the bottom corner of the trench. The V-RESURF TMOS features a P-type layer surrounding a deep trench filled with $SiO_2$ at the source-side compared to the C-TMOS. With the assistant depletion effect of the P-type layer, the depletion of the epitaxial layer is caused not only by the vertical reverse biased P-well/N-drift junction, but also by the lateral reverse biased P-layer/N-drift junction. Thus, before the electric field near the P-well/N-drift junction reaches the critical breakdown electrical field, the epitaxial layer is depleted completely, and the distribution of the electric field in the N-drift becomes more uniform, and an enhanced vertical-RESURF is formed. The BV of the proposed device is increased. In addition, the doping concentration of the N-drift can be higher than that of the C-TMOS, and therefore, the $R_{on,sp}$ is reduced. Because of the higher doping concentration of the N-drift, the CSL (carrier spreading layer) is not used in the V-RESURF TMOS.

The key parameters of the devices are defined and given in Table 1. While making the simulations, SRH, AUGER, OkutoCrowell are used as recombination models, and DopingDependence, HighFieldSaturation and Enormal are used as mobility models.

## III. RESULTS AND DISCUSSIONS

Fig. 2 shows the trade-off between *BV* and *FoM* with different $L_S$ and $T_S$ for the V-RESURF TMOS. The *BV* increases by 3% as $L_S$ goes from 0.5 μm to 1.25 μm, the changes are not obvious. At the same time, the *FoM* ($FoM = BV^2/R_{on,sp}$) decreased obviously as the increasing of $L_S$. The *BV* and

**TABLE 1.** Key parameters of the proposed and C-TMOS devices.

| | V-RESURF | C-TMOS | UNIT |
|---|---|---|---|
| N-drift doping, $N_d$ | optimized | $7\times10^{15}$ | $cm^{-3}$ |
| N-drift thickness, $T_d$ | 9.3 | 8.9 | μm |
| P+-layer doping, $N_{P+}$ | $1\times10^{19}$ | $1\times10^{19}$ | $cm^{-3}$ |
| P+-layer thickness, $T_{P+}$ | 0.3 | 0.3 | μm |
| P-well doping, $N_{Pwell}$ | $2\times10^{17}$ | $2\times10^{17}$ | $cm^{-3}$ |
| P-well thickness, $T_{Pwell}$ | 0.3 | 0.3 | μm |
| CSL-layer doping, $N_{CSL}$ | / | $2\times10^{16}$ | $cm^{-3}$ |
| CSL-layer thickness, $T_{CSL}$ | / | 0.4 | μm |
| Gate oxide thickness, $T_{ox}$ | 50 | 50 | nm |
| Source side oxide length, $L_S$ | optimized | / | μm |
| Source side oxide thickness, $T_S$ | optimized | / | μm |
| V-RESURF P-layer doping, $N_p$ | optimized | / | $cm^{-3}$ |

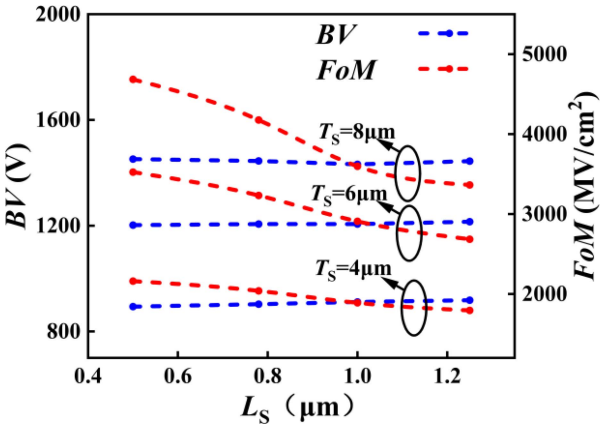


**FIGURE 2.** The *BV* at $V_{gs} = 0$ V and the *FoM* at $V_{gs} = 15$ V for the V-RESURF TMOS with different $L_S$ and $T_S$.

*FoM* at $T_S = 4$ μm, $T_S = 6$ μm, $T_S = 8$ μm increased gradually, which is due to the wider V-RESURF region. The optimized values of $L_S$ and $T_S$ for the V-RESURF structure are 0.75 μm and 8 μm, respectively.

Fig. 3 (a) shows the blocking $I - V$ curves, and the *BV*s of proposed V-RESURF TMOS and C-TMOS are 1552 V and 1368 V, respectively. The breakdown criterion is that $I_{ds}$ reaches 0.001 μA/cm$^2$. The vertical electric field distributions of the two devices at breakdown voltages are shown in Fig. 3 (b). Because of the assistant depletion effect of the vertical RESURF structure, the electric field distribution of the V-RESURF TMOS are more uniform so that the *BV* is higher than that of C-TMOS.

Fig. 4 shows the electric field contours of the two devices at the drain voltages $V_{ds}$ of 1200 V and *BV,* respectively. For the V-RESURF TMOS, even at the breakdown voltage which is higher than that of the C-TMOS, the maximal electric field in gate oxide ($E_{ox}$) of 1.34 MV/cm is much lower than that of 2.55 MV/cm for the C-TMOS. In addition, both of the $E_{ox}$ and the $E_{SiC}$ (the maximal electric field in SiC) are lower for the V-RESURF TMOS.

Fig. 5 (a) shows the influences of $N_p$ and $N_d$ on *BV* for the V-RESURF TMOS. As the increase of $N_d$, to keep the balance of charge, $N_p$ has to increase. Once the $N_p$ is over the optimum value, the *BV* will decline because of the higher lateral electric field. The trade-off between

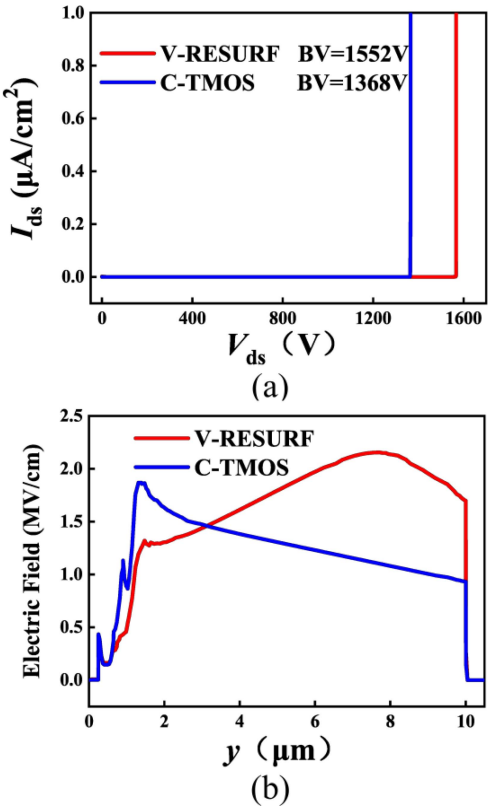


**FIGURE 3.** (a) The breakdown voltages are 1552 V and 1368 V, respectively. (b) The vertical electric field distributions at the *BV*s.

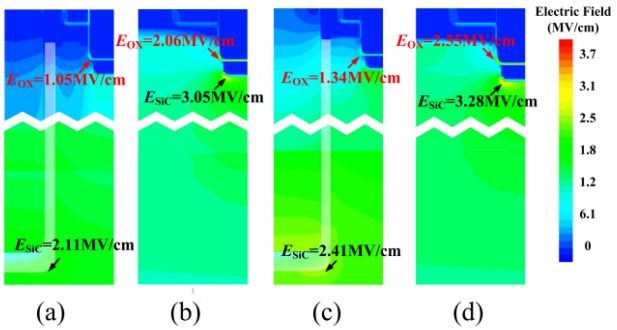


**FIGURE 4.** Electric field at breakdown voltage for (a) V-RESURF TMOS at $V_{ds}$ = 1200 V, (b) C-TMOS at $V_{ds}$ = 1200 V, (c) V-RESURF TMOS at $V_{ds}$ = 1552 V, (d) C-TMOS at $V_{ds}$ = 1368 V.

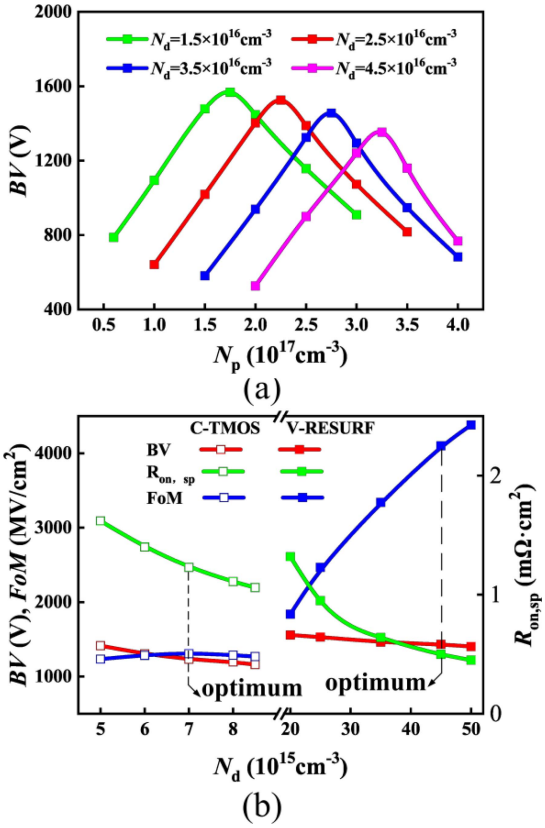


**FIGURE 5.** (a) The influence on breakdown voltage of $N_p$ and $N_d$. (b) The trade-off between breakdown voltage and $R_{on,sp}$ for the proposed V-RESURF TMOS and the C-TMOS.

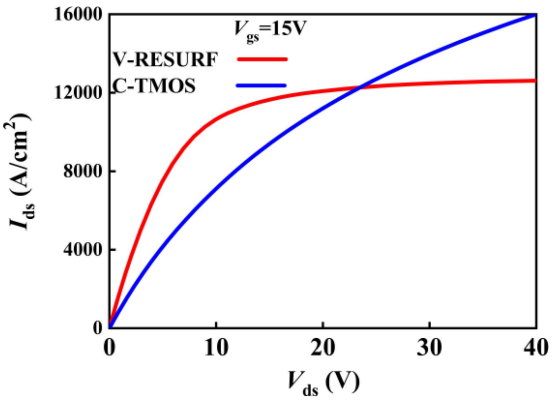


**FIGURE 6.** The $I_{ds} - V_{ds}$ curves at $V_{gs}$ = 15 V.

breakdown voltage and $R_{on,sp}$ for the two devices are shown in Fig. 5(b). The relationship is represented by the figure of merit ($FoM = BV^2/R_{on,sp}$). The optimum value of $N_d$ for the proposed device is $4.5 \times 10^{16}$ cm$^{-3}$ which is much higher than $7 \times 10^{15}$ cm$^{-3}$ for the C-TMOS. The *FoM* of the former is far higher than that of the latter.

Fig. 6 shows the output characteristic curves of the two devices at $V_{gs} = 15$ V. It is obvious that the on-resistance of the proposed device is lower than that of the C-TMOS. The former works into saturation region at the $V_{ds}$ of about 15 V, but according to the output curve, the C-TMOS still works in linear region at $V_{ds} = 40$V.

Fig. 7 shows the gate charge ($Q_g$) of the two devices evaluated by the testing circuit in the inset. The devices' areas are both set as 1 cm$^2$. The $Q_g$ and the gate-to-drain charge ($Q_{gd}$) of the proposed device are 677 nC/cm$^2$ and 144 nC/cm$^2$, respectively, which are far smaller than those of C-TMOS (906 nC/cm$^2$ and 302 nC/cm$^2$). At the gate plateau voltage ($V_{GP}$), the gate-to-drain capacitance ($C_{gd}$) discharges through the gate current to decrease the $V_{ds}$. Once the $V_{ds}$ reaches to on-state voltage ($V_{on}$), the $V_g$ will keep rising to the $V_{gs}$. Due to the smaller $Q_{gd}$, the proposed device has narrower miller plateau.

The basic switching characteristics of the two devices are shown in Fig. 8 (a). The proposed device allows lower

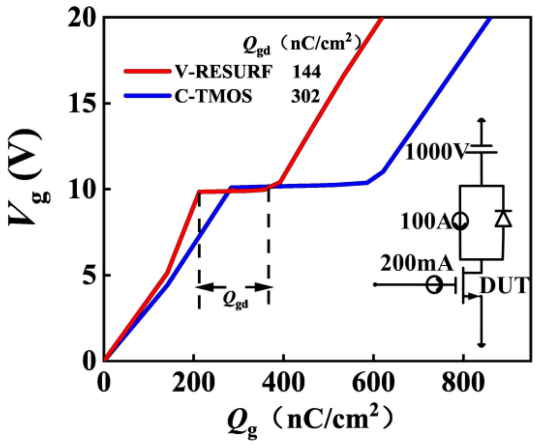


**FIGURE 7.** Gate charge characteristic curves. The $Q_{gd}$ of V-RESURF TMOS and C-TMOS is 144 nC/cm² and 302 nC/cm², respectively. The insert picture is the testing circuit.

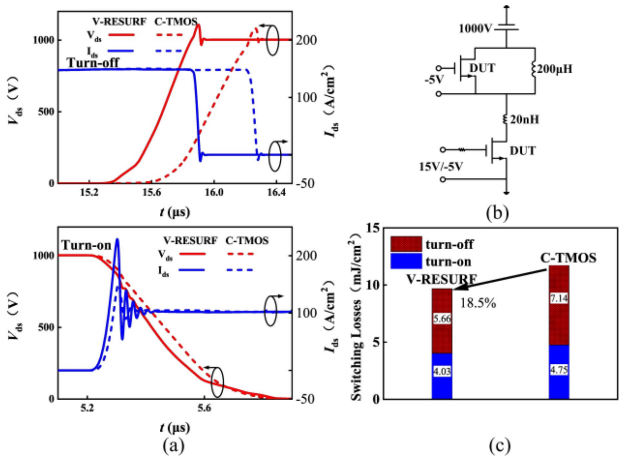


**FIGURE 8.** (a) switching waveforms, (b) testing circuit of switching characteristics, (c) switching losses.

**TABLE 2.** Characteristics of the proposed and C-TMOS.

| | V-RESURF TMOS | C-TMOS | UNIT |
|---|---|---|---|
| $BV$ | 1432 | 1232 | V |
| $R_{on,sp}$ | 0.50 | 1.23 | mΩ·cm² |
| $BV^2/R_{on,sp}$ | 4101 | 1307 | MV/cm² |
| $E_{ox-m}$ | 1.05 | 2.06 | MV/cm |
| $Q_g$ | 677 | 906 | nC/cm² |
| $Q_{gd}$ | 144 | 302 | nC/cm² |
| $Q_{gd}/Q_g$ | 0.21 | 0.33 | / |
| Switching Loss | 9.69 | 11.89 | mJ/cm² |

Optimized parameters of the proposed V-RESURF TMOS, $N_d = 4.5\times10^{16}$ cm$^{-3}$, $N_p = 3.15\times10^{17}$ cm$^{-3}$, half cell pitch is 2 μm, $L_S = 0.75$ μm, $T_S = 8$ μm. Testing $R_{on,sp}$ at $V_{gs} = 15$ V, testing $E_{ox-m}$ at $V_{ds} = 1200$ V, testing $Q_{gd}$ at $V_{gs}$ = -5V to 15V.

switching loss and larger d$V$/d$t$ due to the smaller gate-to-drain charge. Fig. 8. (b) shows the double-pulse circuit mixed mode simulation. The switching loss of the proposed device reduces by 18.5% as shown in Fig. 8 (c).

Table 2 summarized the characteristics of V-RESURF TMOS and C-TMOS. The former shows a better performance at $E_{ox-m}$, $Q_g$ and $Q_{gd}$. In addition, compared with the C-TMOS, the V-RESURF TMOS exhibits a higher $BV$ and a lower $R_{on,sp}$ due to the assistant depletion effect of the vertical enhanced RESURF.

## IV. CONCLUSION

A 1200 V SiC trench MOS with an enhanced vertical RESURF is proposed and numerical simulated by TCAD in this article. The proposed device shows much better performance in the trade-off between the breakdown voltage and the specific on-resistance. Furthermore, the proposed device shows lower switching loss due to the smaller gate-to-drain charge.

## REFERENCES

[1] S. Mori, M. Aketa, T. Sakaguchi, H. Asahara, T. Nakamura, and T. Kimoto, "Suppression of punch-through current in 3 kV 4H-SiC reverse-blocking MOSFET by using highly doped drift layer," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 449–453, 2018, doi: 10.1109/JEDS.2018.2819681.

[2] J. An and S. Hu, "SiC trench MOSFET with heterojunction diode for low switching loss and high short-circuit capability," *IET Power Electron.*, vol. 12, no. 8, pp. 1981–1985, Jul. 2019, doi: 10.1049/iet-pel.2019.0035.

[3] A. Agarwal, K. Han, and B. J. Baliga, "600 V 4H-SiC MOSFETs fabricated in commercial foundry with reduced gate oxide thickness of 27 nm to achieve IGBT-compatible gate drive of 15 V," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1792–1795, Nov. 2019, doi: 10.1109/LED.2019.2942259.

[4] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET: Part I—History, technology, and prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 674–691, Mar. 2017, doi: 10.1109/TED.2017.2653239.

[5] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017, doi: 10.1109/TED.2017.2655149.

[6] J. Wu, H. Huang, B. Yi, H. Hu, H. Hu, and X. B. Chen, "A snapback-free and low turn-off loss reverse-conducting SOI-LIGBT with embedded diode and MOSFET," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1013–1017, 2019, doi: 10.1109/JEDS.2019.2939223.

[7] K. Nakamura, S. Kusunoki, H. Nakamura, and M. Harada, "Advantages of thick CVD gate oxide for trench MOS gate structures," in *Proc. 12th Int. Symp. Power Semicond. Devices ICs*, Toulouse, France, 2000, pp. 83–86, doi: 10.1109/ISPSD.2000.856778.

[8] R. Chen, H. Hu, Y. Lin and X. B. Chen, "A novel shielded IGBT (SIGBT) with integrated diodes," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 594–599, 2020, doi: 10.1109/JEDS.2020.3000280.

[9] M. Dai *et al.*, "A model with temperature-dependent exponent for hot-carrier injection in high-voltage nMOSFETs involving hot-hole injection and dispersion," *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1255–1258, May 2008, doi: 10.1109/TED.2008.919322.

[10] J. F. Chen, K. Tian, S. Chen, K. Wu, and C. M. Liu, "On-resistance degradation induced by hot-carrier injection in LDMOS transistors with STI in the drift region," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1071–1073, Sep. 2008, doi: 10.1109/LED.2008.2001969.

[11] X. Gong, Y. Zhang, L. Hao, H. Wu, Y. Ding, and M. Liu, "Effect of trench bottom implantation on the performance of trench MOSFET," *Proc. IEEE Int. Conf. Integr. Circuits Technol. Appl. (ICTA)*, Chengdu, China, 2019, pp. 115–116, doi: 10.1109/ICTA48799.2019.9012881.

[12] K. Wada *et al.*, "Fast switching 4H-SiC V-groove trench MOSFETs with buried P+ structure," *Proc. IEEE 26th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, Waikoloa, HI, USA, 2014, pp. 225–228, doi: 10.1109/ISPSD.2014.6856017.

[13] Y. Wang, K. Tian, Y. Hao, C. Yu, and Y. Liu, "4H–SiC step trench gate power metal–oxide–semiconductor field-effect transistor," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 633–635, May 2016, doi: 10.1109/LED.2016.2542183.

[14] A. W. Ludikhuize, "A review of RESURF technology," *Proc. 12th Int. Symp. Power Semicond. Devices ICs*, Toulouse, France, 2000, pp. 11–18, doi: 10.1109/ISPSD.2000.856763.

[15] G. Sabui and Z. J. Shen, "Analytical calculation of breakdown voltage for dielectric RESURF power devices," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 767–770, Jun. 2017, doi: 10.1109/LED.2017.2690964.