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# Methodology to Investigate Impact of Grain Orientation on Threshold Voltage and Current Variability in Tunneling Field-Effect Transistors

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**ABSTRACT** In this article, an investigation has been performed to statistically analyze the entire sub-threshold characteristics of tunnel field-effect transistor (TFET) depending on a gate work function variation (WFV). Firstly, the current variations are evaluated through turn-on voltage ($V_{ON}$) and threshold voltage ($V_T$) with help of technology computer-aided design (TCAD) simulation. Secondly, the variation of $V_T$ and $V_{ON}$ are quantitatively analyzed by coefficient of determination ($R^2$) in the regression analysis. The $R^2$ values are extracted according to the divided the gate prats. Finally, it is confirmed that the WFV of the gate parts causes the current variation in areas where tunneling is varied mainly according to the gate bias.

**INDEX TERMS** Band-to-band tunneling, tunnel field-effect transistor (TFET), work-function variation (WFV), regression analysis.

## I. INTRODUCTION

A tunnel field-effect transistor (TFET) has attracted a lot of researchers' attention to reduce power consumption in complementary metal-oxide-semiconductor (CMOS) circuits [1]–[4]. It has remarkable advantages for low-voltage operation due to its small subthreshold swing (SS) less than 60 mV/dec and low-level off-state current ($I_{OFF}$) [5], [6]. Moreover, the electrical performance of TFET can be improved dramatically by applying the high-$\kappa$/metal gate (HKMG) technology. Thus, it shows that the TFET is applicable to the real industry [7]–[10]. The weak impact of gate dielectric constant in the presence of WFV has been reported with increase in $\kappa$, [11]. However, the application of HKMG brings a work function (WF) variation (WFV) issue due to the non-uniformity of metal gate grains in size and in orientation depending on the fabrication processes [12]–[19]. Therefore, in order to apply the TFET to the real CMOS circuits, the electrical performance variations according to the WFV must be scrutinized. Although, there are several studies about the WFV effects on TFET, they have some issues to be improved. First, there are a fundamental limit in providing quantitative analysis on how much WFV effects are correlated to the electrical characteristics [17]–[20]. Second, the previous papers have focused on changes in electrical characteristics [e.g., threshold voltages ($V_T$) and on-state current ($I_{ON}$)] [17]–[20]. However, these parameters could not represent the entire subthreshold characteristics of TFET. Therefore, this article aims to analyze the effects of WFV on TFET's entire subthreshold characteristics with the help of technology computer-aided design (TCAD) simulation. Additionally, this article provides a methodology for the statistical analysis of TFETs with WFV. In Section II, the structure and dimension of studied TFET are explained. The WFV induced by the grain

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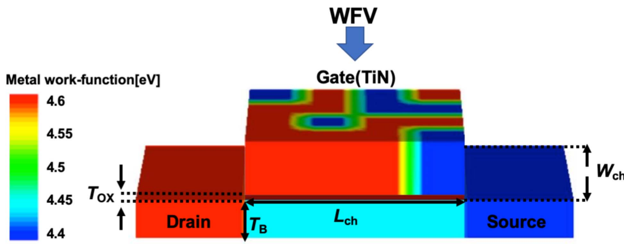


**FIGURE 1.** 3-D structure of planar TFET. The WFV is applied randomly in the gate from 4.4 eV to 4.6 eV.

**TABLE 1.** Design parameters.

| Parameters | Value |
|---|---|
| Source doping concentration ($N_S$) | $10^{20}$ cm$^{-3}$ (*p*-type) |
| Drain doping concentration ($N_D$) | $10^{20}$ cm$^{-3}$ (*n*-type) |
| Body doping concentration ($N_B$) | $10^{17}$ cm$^{-3}$ (*p*-type) |
| Gate work-function | variable |
| Channel length ($L_{ch}$) | 40 nm |
| Channel width ($W_{ch}$) | 40 nm |
| Average metal grain size | 10×10 nm$^2$ |
| Body thickness ($T_B$) | 7 nm |
| Gate oxide thickness ($T_{OX}$) | 1 nm |
| Drain voltage ($V_D$) | 0.5 V |

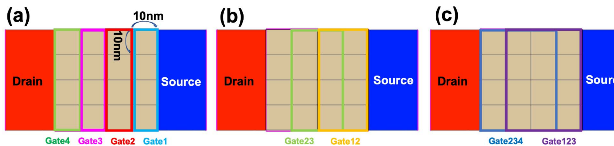


**FIGURE 2.** Top view of 3-D structure of planar TFET divided into 16 square-shaped grains. The grains are grouped as (a) single columns, (b) double columns, and (c) triple columns.

of the metal gate is set reflecting the actual gate physical properties. In Section III, the quantitative analysis is performed by using the coefficient of determination ($R^2$) in the regression analysis to monitor the whole subthreshold characteristics of the TFET. In Section IV, a band-to-band tunneling (BTBT) rate in the channel according to WFV is confirmed to validate the correlation obtained by $R^2$.

## II. SIMULATION

Three-dimensional (3-D) structure of planar TFET used for TCAD simulation is shown in Fig. 1. The simulation is carried out using Synopsys Sentaurus [21]. It features ultra-thin body thickness ($T_B$), gate oxide thickness ($T_{OX}$). And the arsenic and boron are used as the dopant atoms for n- and p-type doping to make abrupt doping profile for source and drain regions to suppress side effects (e.g., short-channel effect) [22]. All of simulations are performed at 300 K The design parameters are summarized in Table 1. A dynamic nonlocal BTBT and a Shockley-Read-Hall (SRH) generation-recombination models are used for a rigorous study. The BTBT parameters for Si tunneling model are calibrated by measured results [23], [24].

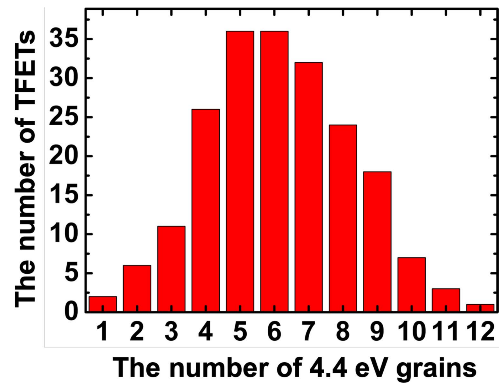


**FIGURE 3.** Histogram of randomly generated gate metal grains. The frequency of occurrence of 4.4-eV grain in 200 samples is indicated.

In detail, the BTBT model is calibrated with experimental results [28]. The BTBT generation rate per unit volume ($G$) is defined as

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right) \tag{1}$$

in the uniform electric field limit where $F_0 = 1$ V/m and $P = 2.5$ for indirect tunneling [25]. The prefactor ($A$) and the exponential factor ($B$) are Kane parameters while the $F$ is electric field [26], [27]. The extracted $A$ and $B$ parameters of the BTBT model in Si TFET are $4 \times 10^{14}$ cm$^{-3}$·s$^{-1}$ and $9.9 \times 10^6$ V/cm, respectively. In addition, a modified local-density approximation (MLDA) is applied to consider quantum effects. Finally, a WF randomize model is adopted for a statistical consideration of WFV in gate.

Fig. 2(a) shows the methods for applying WFV in the gate. The $40 \times 40$ nm$^2$ gate area is split into 16 units considering the grain size of TiN and it is assumed to be an identical square shape; the area of each unit is $10 \times 10$ nm$^2$. The sputtered TiN is mainly crystallized in <200> (60%) and in <111> (40%) which are corresponded to 4.6-eV and 4.4-eV WFs, respectively [28]. Considering these probabilities, WFV of each gate area out of 16 units is randomly assigned. As a result, two hundred TFET structures with randomly generated WFV are created. As shown in Fig. 3, the number of TFETs well follows the Gaussian distribution as a function of the number of metal grains with 4.4 eV-WF. In the distribution, the probability of 4.4 eV (mean value/total units = 38.6%) is similar to the probability of TiN crystallized in <111> (40%). It shows that the method of applying WFV to the gate is highly reliable. In order to clarify the metal grains which dominantly determine the current-voltage characteristics, they are grouped as single columns (Gate1, Gate2, Gate3 and Gate4), double columns (Gate12 and Gate23), and triple columns (Gate123 and Gate234) [Figs. 2(a), 2(b) and 2(c)]. The WFV effect is analyzed with the help of linear regression. In detail, the $R^2$ is extracted for $V_T$ and turn-on voltage ($V_{ON}$) distribution in terms of the number of 4.4 eV grains in the grouped column ($N_{Gate}$) [18]. The $R^2$ ($0 < R^2 < 1$) denotes the strength of

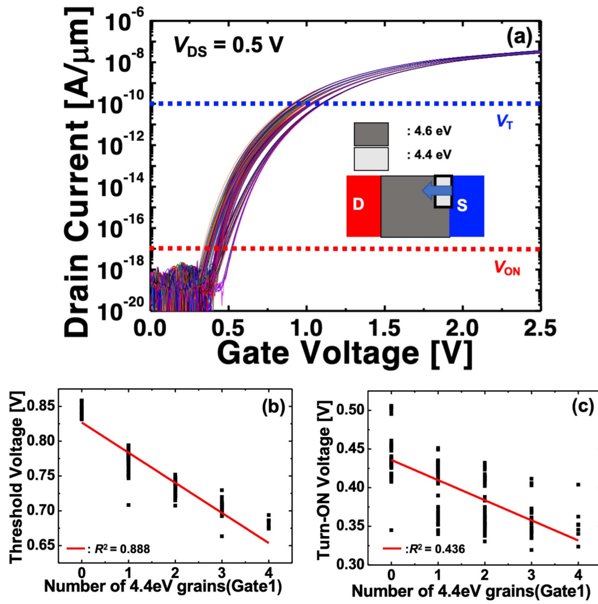


**FIGURE 4.** (a) Log ($I_d$) − $V_{GS}$ curves for two hundred samples with WFV. Number of 4.4-eV grains in Gate1 versus (b) $V_T$ and (c) $V_{ON}$.

the linear correlation between WFV in each column and $V_T$ (or $V_{ON}$) [29]. The calculation of $R^2$ value is as follow

$$SS_{\text{total}} = \sum (y_i - \bar{y})^2 \quad (2)$$

$$SS_{\text{regression}} = \sum \left(y_i - y_{\text{regression}}\right)^2 \quad (3)$$

$$R^2 = 1 - \frac{SS_{\text{regression}}}{SS_{\text{total}}} \quad (4)$$

where the $SS_{\text{total}}$ and $SS_{\text{regression}}$ are sum squared total error and regression error respectively. The $y_i$, $\bar{y}$ and $y_{\text{regression}}$ mean each data point, mean value and regression value respectively.

## III. SIMULATION RESULTS

Fig. 4(a) shows transfer curves of planar TFET for all of two hundred samples. The increase in $V_{GS}$ introduces a strong inversion caused by electrons from the drain, which results in the pinning of the channel's surface potential [30], [31]; channel potential rarely changes as a function of $V_{GS}$. The $V_T$ and $V_{ON}$ are extracted at drain current ($I_D$) of $10^{-11}$ A/μm and $10^{-17}$ A/μm, respectively. Fig. 4(b) shows $V_T$ as a function of $N_{\text{Gate1}}$. The $V_T$ is decreased as the $N_{\text{Gate1}}$ increases and 0.888-$R^2$ statically supports a high correlation between $N_{\text{Gate1}}$ and $V_T$. The reason for this high correlation is that TFET characteristics are mainly determined by WF values of metal grains near to the source region where band-to-band tunneling occurs [17]. Therefore, when the gate metal grains with 4.4-eV are located to a channel width direction in Gate1 column, a surface potential is decreased locally under the grains with 4.4-eV [inset of Fig. 4(a)]. On the other hand, unlike to the $V_T$, the $V_{ON}$ shows relatively weak correlation with $N_{\text{Gate1}}$; 0.436-$R^2$ [Fig. 4(c)]. It is noteworthy that the $V_{ON}$ of TFET is weakly affected by gate WF at

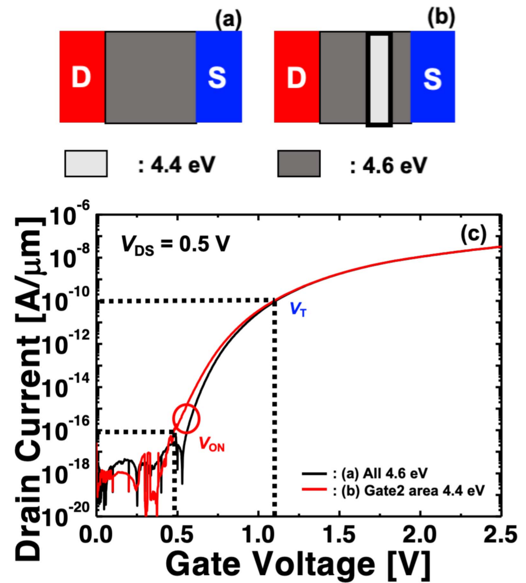


**FIGURE 5.** WFV plots for (a) WFs in all gate are set as 4.6 eV and for (b) only Gate2 region is set as 4.4 eV. (c) Transfer curves with condition of Figs. 5(a) and 5(b).

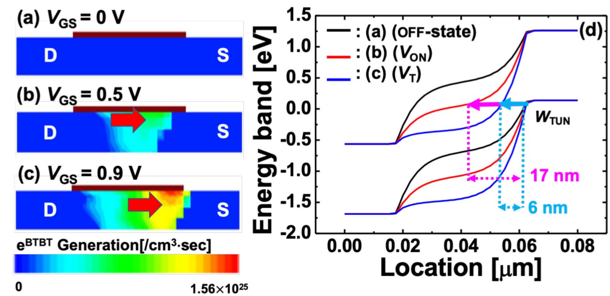


**FIGURE 6.** Electron BTBT generation rate when all gate WFs are 4.6 eV. (a) $V_{GS} = 0$ V(b) $V_{GS} = 0.5$ V (c) $V_{GS} = 0.9$ V. (d) Energy band diagrams for each bias condition in Figs. 6(a)-6(c).

the source-channel junction. According to the results of the pre-reported paper, WFV near the source area determines variation of $V_{ON}$ [17]. However, based on the weak correlation between $N_{\text{Gate1}}$ and $V_{ON}$, this argument should be reconsidered.

## IV. DISCUSSION

In order to analyze the results, two WFV cases are compared. First, WFs of all gate are set as 4.6 eV [Fig. 5(a)]. Second, WF of Gate2 is set as 4.4 eV and the other regions are set as 4.6 eV [Fig. 5(b)]. As shown in Fig. 5(c), they show the different $V_{ON}$ and the same $V_T$. Based on the result, it is clear that WF in Gate2 is a dominant factor that determines the $V_{ON}$. In order to confirm this result specifically, electron BTBT generation rate at 0 V, 0.5 V and 0.9 V of $V_{GS}$ are investigated in Figs. 6(a), 6(b), and 6(c). Comparing Fig. 5(c), each bias condition is corresponded to the OFF-state, at $V_{ON}$, and at $V_T$, respectively. In Fig. 6(b), the maximum BTBT ($\text{BTBT}_{\text{MAX}}$) region is located at the channel slightly away from the source. On the other hand, in Fig. 6(c), the $\text{BTBT}_{\text{MAX}}$ region is located at right next to the

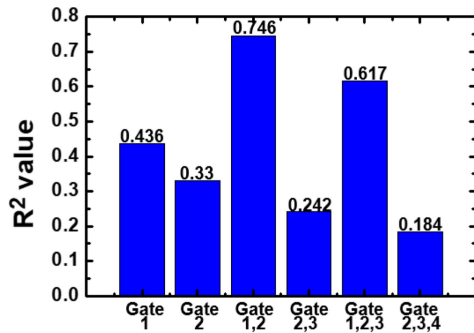


**FIGURE 7.** $R^2$ **value of** $V_{ON}$ **distributions obtained from the WFV over various gate regions.**

source-channel junction. It means that the $BTBT_{MAX}$ region is shifted from the middle of channel to the source-channel junction as $V_{rmGS}$ increases. The energy band diagrams in Fig. 6(d) verify the tunnel barrier width ($W_{TUN}$) is 17 nm for $V_{GS} = V_{ON} = 0.9$ V and 6 nm for $V_{GS} = V_T = 0.5$ V, which are corresponded to the distance from the source-channel junction to the Gate2 and to the Gate1, respectively. Therefore, the position of the WFV affecting the TFET current is moved from Gate2 to Gate1 as the $V_{GS}$ increases. In order to confrim quantitive correlation, $R^2$ values are extracted for the various cases (Fig. 7). Among these cases, it is found that $R^2$ value of Gate12 is the highest. The results confirm that the $V_{ON}$ is affected by the source-channel junction as well as by the junction in which BTBT starts to occur.

Finally, based on the simulations, we conclude two factors. First, the $V_{ON}$ parameter should be evaluated to confirm the current variation in the subthreshold region of TFET according to WFV. Because $V_T$ variation does not represent the current variation in the whole subthreshold region. Second, as the $V_{GS}$ increases, the location where the $BTBT_{MAX}$ appears changes and is moving from channel to source. Based on the $R^2$ values, the shift of the $BTBT_{MAX}$ position is confirmed by the high correlation in the double column.

## V. CONCLUSION

The effect of WFV on TFET has been studied by statistical analysis with $V_T$ and $V_{ON}$ variation to analyze subthreshold variation. The correlation between WFV and $V_{ON}$ (or $V_T$) is verified by regression analysis. It has been demonstrated that the gate part above the channel region with high BTBT rate shows high correlation. Thus, it is concluded that the TFET is affected by WFV of particular gate region rather than by WFV of whole gate. It means that only WF of several grains over the narrow source-channel junction determines the current variation of TFET. Therefore, increasing the source-channel junction area affected by WFV can be a promising solution to reduction of the dependency on the WFV.

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