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Compact Modeling of Multi-Gate MOSFETs for High-Power Applications

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ABSTRACT A compact multi-gate MOSFET model is developed for high-voltage applications. The model includes the short-channel effects specific for thin-film MOSFETs with highly resistive drain contact. The short-channel effects are drastically reduced by the drain-resistance effect, which is consistently modeled by considering the whole potential distribution along the device. The overlap length is an important device parameter, which influences on the device characteristics for high-voltage MOSFETs in general. Modeling of the related effects is realized self-consistently for the reported compact high-voltage multi-gate MOSFET model, based on the applied complete potential-distribution description. In particular, the modeling requirements for capturing the specific features of the capacitance response are explored in detail. It is further demonstrated that the developed model is applicable even for limiting the device-size requirements during the development of a multi-gate MOSFET generation.

INDEX TERMS Compact model, short-channel effects, drain resistance effect, multi-gate MOSFET, high-voltage MOSFET, capacitances, overlap length.

I. INTRODUCTION

It is common nowadays, that high voltage and low voltage devices are integrated on the same chip. This is due to application requirements, where high-voltage switching circuits have to be operated by mainly functional low-power circuits [1]–[6]. For such applications the combined circuit is usually fabricated with an identical technology for both low- and high-voltage devices to save fabrication cost. Furthermore, a channel-length reduction is mandatory to achieve high density integration of the circuits, which causes the short-channel effects such as the subthreshold deterioration. To overcome the short-channel-effect problems, the multi-gate MOSFET (MG-MOSFET) with very thin-layer structures has been industrially developed [1], [7]–[9]. However, it is still hard to reduce the short-channel effects sufficiently, even with an extremely thin channel layer [10]. Compact modeling for the thin-layer devices has been mostly done through the study of physics-based device simulations [11]–[14]. We have developed a consistently potential-based compact model for the short-channel effects in such leading-edge thin-layer MOSFETs [1], and demonstrated that the origin of the short-channel effects is the leakage current flowing between source and drain deep in the channel. The developed modeling considers the potential distributions at the source junction, in the middle of the channel and at the drain junction.

Generally, the source/drain contact region is highly doped so that no performance degradation occurs, namely a high conductivity is used to increase the current [1]. However, for thin-layer MOSFET generations, the contact-resistance effect is very much enhanced [2], [15]–[18]. In this context, it has further been demonstrated that a small reduction of the drain-doping concentration can suppress the short-channel effects quite drastically, while causing a small increase in the drain-resistance effect and in the power loss at the same time. Fortunately, a favorable compromise between short-channel-effect reduction and power-loss increase can be achieved [14].

High-voltage applications need high-voltage MOSFETs [2]–[5], [19], and such devices are particularly demanded to provide and handle the power of complete systems. The MOSFET structure has thus been

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optimized in order to support higher voltages at the drain side. The operation principle is based on a high drain-resistance effect, obtained by enlarging the drain-region length as well as reducing the drain-doping concentration. The drain-resistance effect allows an increase of the supported drain voltages, but of course limits the maximum drive current of the MOSFET.

In this investigation, our focus is given on the development of an extended compact model for MG-MOSFETs, using a Double-Gate MOSFET (DG-MOSFET) as the primarily studied device [1], [8]. The targeted high voltages are in the 2V-3V range, while the low-voltage range is up to 1.2V at maximum. In particular, we have investigated device performances as a function of the gate-source voltage V_{gs} in the interval -0.2V to 2V and as a function of the drain-source voltage V_{ds} in the interval 0V to 3V. The developed model is valid for low- and high-voltage applications, and must therefore describe both the short-channel effects and the drain-resistance effects accurately. For this purpose, a consideration of the whole potential distribution along the device is a prerequisite in our modeling approach. For high-voltage MOSFETs, it is known that the gate-overlap-length optimization is a key parameter to achieve high device performance. The influence of the overlap length on the drive currents has been verified previously [20]. Our focus is consequently given on the capacitance characteristics of the investigated high-voltage MG-MOSFET, which has a strong influence on the switching performances.

II. MODELING APPROACHES

A. STUDIED DEVICE STRUCTURE

Instead of measurements, we utilized 2D numerical device-simulation results [21], which are calculated by solving all basic device equations simultaneously. The 3-dimensional view of the investigated MG-MOSFET is schematically shown in Fig. 1a, where the cross-section of the studied high-voltage double-gate-device structure is also indicated and shown in more detail in Fig. 1b. A 3D numerical-simulation treatment becomes only important, when the channel length and the channel width are of comparable size. However, the channel width is usually at least several times wider, even when the channel length is of nano-scale dimensions, to get sufficient current flow. The width of the MG-MOSFET is given by the height of the fin, namely the extension into the z direction in Fig. 1. This height is normally much larger than L, especially when high-power applications are targeted. To sustain the applied high voltage within the device, a long lightly-doped drift region is considered for high-voltage applications [2], [5]. Though the drift-region structure could have complicated 2D configurations, the fundamental features of the drain resistance can be modeled with the simpler structure shown in Fig. 1b.

Channel-doping concentration N_A, source-doping concentration N_{DS}, channel width W, equivalent oxide thickness t_{ox}, silicon thickness t_S and source-contact length $L_{diff,s}$ are fixed for our study. Values of these quantities are listed at the bottom of Fig. 1. The overlap length L_{over} is considered independently, to investigate its effect on device performance. The total drain contact length $L_{diff,d}$ is set to 75nm, which is relatively long so that the device can be applicable for drain voltages $V_{ds} \leq 3$V.

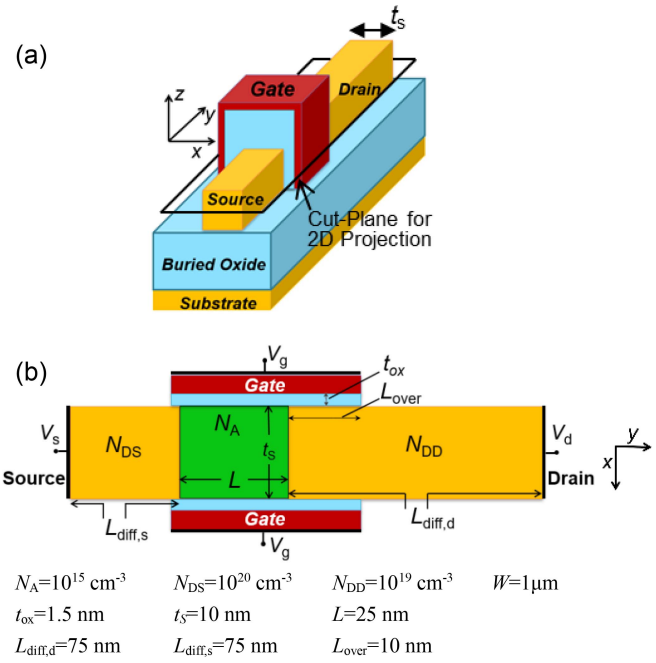

FIGURE 1. (a) FinFET device structure. (b) Studied double-gate MOSFET structure resulting from the cross section along the indicated cut-plane in (a), device parameter values are listed at the bottom.

B. MODELING OF SHORT-CHANNEL EFFECTS

Fig. 2a shows the simulated $I-V$ characteristics of the studied high-voltage DG-MOSFET. As can be seen from Fig. 2b and c, the main origin of the short-channel (SC) effects is the high current flow deep in the device around the middle between channels, which is governed strongly by the lateral electric field [1]. This deep current flow (see Fig. 2b) diminishes according to the gate voltage V_{gs} increase, namely according to the formation of inversion layers at the gate to channel interfaces. For compact modeling of the SC effects, the potential distributions for a long-channel transistor, due to the superposition of the potentials extending from source/channel and channel/drain junctions, is considered explicitly by a cubic function of the position along the channel y as [1]

$$\phi(y) = A_0 \cdot (y + B_0)^3 + C_0 \tag{1}$$

Here, the parameters A_0, B_0 and C_0 are written as functions of the electric fields induced at source/channel and drain/channel junctions, as summarized in Table 1, where β is the inverse of the thermal voltage. The minimum potential $C_0 = \phi_{min}$ is the solution of the Poisson equation for the long-channel DG-MOSFET [20], and thus independent of the drain voltage (V_{ds}). At the minimum-potential position

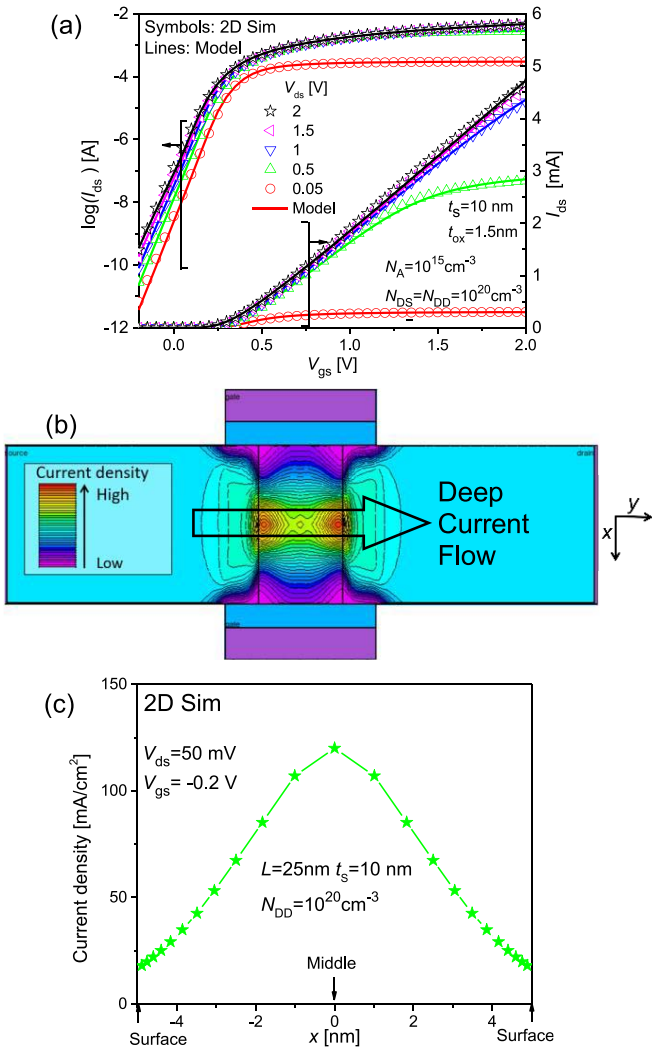

FIGURE 2. (a) $I_{ds} - V_{gs}$ characteristics only for $N_{DD} = 10^{20}$ cm^{-3}, (b) current-density cross section between the two gates along the channel direction, and (c) current flow-line densities between the two gates at $y = 0$ for $V_{gs} = -0.2$V and $V_{ds} = 50$ mV.

$y_{\min} = B_0$ flows the maximum current under the subthreshold condition. By reducing the channel length, the potential distributions from source and drain junctions start to overlap, which leads to an increase of $\phi_{\min}$ along the channel as depicted in Fig. 3. The minimum-potential increase $\Delta\phi_{\min}$ in comparison to the long-channel device is written as [1]

$$\Delta\phi_{\min}(V_{\rm gs}, V_{\rm ds}, L) = -2 \cdot A_0 \cdot \left(y_{\min} - \frac{L_0 - L}{2}\right)^3 \quad (2)$$

where $y_{\min}$ is the position of this minimum potential along the channel direction. $y_{\min}$ is determined by the balance between the fields at the source/channel and the channel/drain junctions as

$$y_{\min} = -\frac{V_{\rm di}}{E_{\rm Source} + E_{\rm Drain}} \quad (3)$$

Here, $V_{\rm di}$ is the potential difference between the drain/channel and source/channel edges, which is $V_{\rm ds}$ for a non-resistive drain region (high drain-doping concentration). The electric fields $E_{\rm Source}$ and $E_{\rm Drain}$ at source and drain junctions, respectively, are fundamentally determined by the impurity profiles at these junctions. From the compact-modeling point of view, they are modeled by the potential difference between the junctions, as summarized in Table 1.

TABLE 1. Analytical description and explanations of the parameters used in model equations.

Parameter	Quantity	Value
A_0	Potential gradient	$sign(y)\cdot(V_{\rm biSource} - \phi_{\min}) / (L_0/2)^3$
B_0	Potential-minimum position	$y_{\min}$
C_0	Potential minimum	$\phi_{\min}$
L_0	Minimum long-channel length that preserves no subthreshold degradation	Value to extract.
$V_{\rm biSource}$	Built in potential at source/channel junction	$\beta^{-1}\cdot\ln\left(\frac{N_{\rm DS}\cdot N_{\rm A}}{n_i^2}\right)$
$V_{\rm biDrain}$	Built in potential at drain/channel junction	$\beta^{-1}\cdot\ln\left(\frac{N_{\rm DD}\cdot N_{\rm A}}{n_i^2}\right)$
$E_{\rm Source}$	Maximum electric field at source/channel junction	$\frac{V_{\rm biSource} + V_s - \phi_{\min}}{XJ_0}$
$E_{\rm Drain}$	Maximum Electric Field at drain/channel junction	$\frac{V_{\rm biDrain} + V_{\rm di} - \phi_{\min}}{XJ_0}$
XJ_0	Scaling length parameter	$\sqrt{(\varepsilon_S t_S t_{\rm ox}/2\varepsilon_{\rm ox})(1+\varepsilon_{\rm ox}t_S/4\varepsilon_S t_{\rm ox})}$

The modeled $\Delta\phi_{\min}$ has been implemented into HiSIM_MG [22] to include the influence of the lateral potential distribution in the form [23]

$$V'_{\rm G} = V_{\rm gs} - V_{\rm FB} + \Delta\phi_{\min} \quad (4)$$

which is used to calculate the value of the surface potential $\phi_{\rm S}$ at the gate to channel interface by solving the Poisson equation together with the Gauss Law

$$\phi_{\rm S}(y) = V'_{\rm G} + \frac{Q_{\rm sem}(y)}{C_{\rm ox}} \quad (5)$$

where $Q_{\rm sem}$ is the total charge induced in the semiconductor channel, and is a function of $\phi_{\rm S}$. $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$ is the gate capacitance per area unit for oxide permittivity $\varepsilon_{\rm ox}$. This implicit function is solved iteratively using a 1D Newton method, where an accurate initial analytical value is used to increase the calculation speed, leading to very low cost in terms of time. Instead of solving the Poisson equation along the whole channel, only the source-side channel position and the drain-side channel position are solved by considering the quasi-Fermi distribution within the channel under the drift-diffusion approximation, which is valid under the gradual-channel approximation. Thus, all device performances are a function of the calculated potential distribution at source and drain sides.

Figure 2a also depicts the model-calculation results together with the 2D-device simulation results. Figure 4 shows the comparison between compact-model-calculation results and 2D-device simulation results for the gate-capacitance $C_{\rm gg}$. The SC effects are mostly due to the leakage current induced deep in the middle between the channels. The corresponding charge in the middle between the

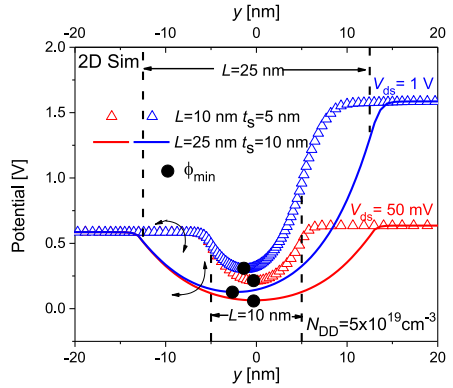

FIGURE 3. 2D numerical device-simulation results of potential distributions in the middle between the gates ($x = 0$) and along the channel of the studied scaled devices for gate voltage V_{gs} of -0.2V and channel lengths L of 10nm and 25nm. The potential minimum ϕ_{min} arises from the overlap of the source-and drain-side potentials.

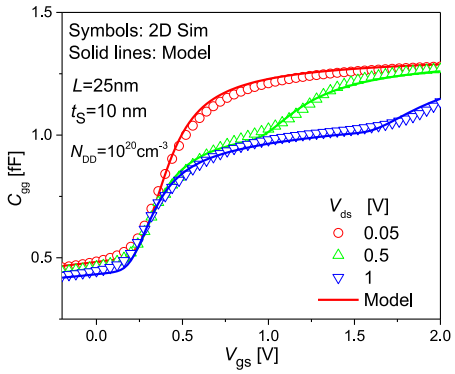

FIGURE 4. Simulated and modeled normalized $C_{gg} - V_{gs}$ characteristics for different V_{ds} values.

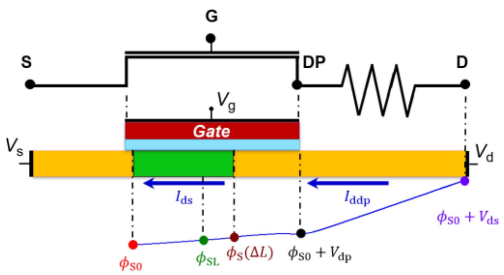

FIGURE 5. MOSFET modeling with inclusion of the bias-dependent drain-resistance effect, namely for low and enlarged N_{DD} region at high biases. $\phi_{S0/SL}$ are the surface potentials at source and pinch-off point, respectively. $\phi_S(\Delta L)$ is the potential at channel/drain junction. V_{dp} is the potential at the internal node DP. $\phi_0 + V_{ds}$ is the potential at drain contact.

channels contributes less to the capacitances for the above-threshold region. This is the reason for the quite conventional $C_{gg} - V_{gs}$ characteristics observed.

C. INCLUSION OF DRAIN RESISTANCE AND DEPLETION EFFECTS

In a low-doped drain region two effects are observable: Firstly, the drain resistance effect at high applied gate and drain biases and secondly, the effect of the depletion-region

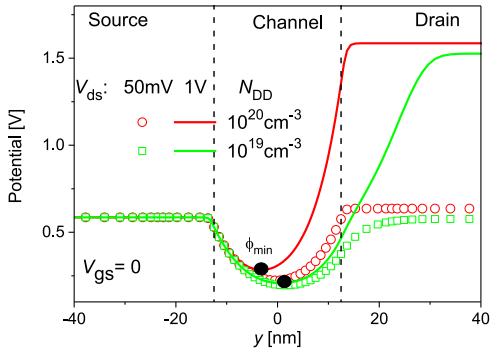

FIGURE 6. Potential distribution along the channel middle ($x = 0$) for different drain doping concentrations N_{DD} at $V_{ds} = 50$mV and 1V with fixed $V_{gs} = 0$. The studied device parameters are $L = 25$nm, $t_S = 10$nm, $t_{ox} = 1.5$nm and $N_A = 10^{15}$cm^{-3}.

expansion during subthreshold operation of short-channel devices, due to the low space-charge density in the drain region. The developed model has been extended to include both effects [14]. To understand the resistance effect of the drain diffusion region, the potential distribution along a highly resistive drain region at high applied gate and drain biases is schematically depicted in Fig. 5. It can be seen that the potential distribution extends deep into the drain region, when the drain resistance effect is increased due to a low N_{DD} and extended drain region. Modeling of the potential-distribution extension into the diffusion region is done by using the HiSIM_HV modeling concept [24], as also schematically illustrated in Fig. 5. The internal node V_{dp} around the end of the gate overlap refers to the end of the gate control. Since V_{dp} is determined by the balance between the current flow in the channel I_{ds} and that in the drift region I_{ddp}, the solution is obtained by iteratively solving the continuity relationship of the two currents at the internal node "DP". The current flow in the MOSFET channel is given by

$$I_{ds} = 2\frac{W}{L}\cdot\frac{\mu_{eff}}{\beta} \times\left[(Q_{nL}-Q_{n0})-\frac{\beta}{2}\cdot(Q_{nL}+Q_{n0})\cdot(\phi_{SL}-\phi_{S0})\right] \tag{6}$$

where β is the inverse of the thermal voltage, while Q_{nL}, ϕ_{SL} and Q_{n0}, ϕ_{S0} are the mobile charges and surface potentials at drain and source sides of the channel, respectively. On the other hand, the current flowing in the drain drift region I_{ddp} is written as [24]

$$I_{ddp} = W\cdot X_{OV}\cdot q\cdot N_{DD}\cdot\mu_{drift}\cdot\frac{V_{ddp}}{L_{drift}} \tag{7}$$

$$V_{ddp} = V_{ds} - V_{dp} \tag{8}$$

where W and X_{OV} are the width and the depth extension of the current flow under the overlap region, respectively, while L_{drift} is the length of the resistive drift region and μ_{drift} is the effective mobility of the drain resistive

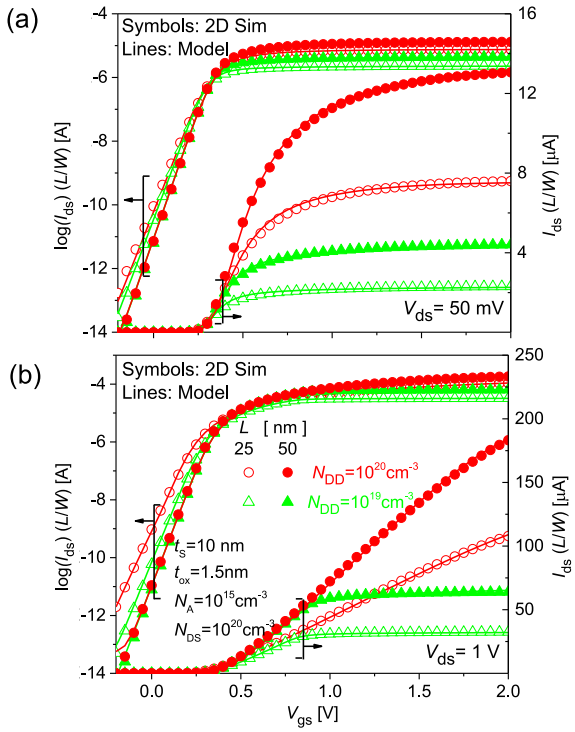

FIGURE 7. Simulated and modeled normalized *I-V* characteristics at (a) $V_{ds} = 50$ mV and (b) $V_{ds} = 1$V for different drain doping concentrations and channel lengths.

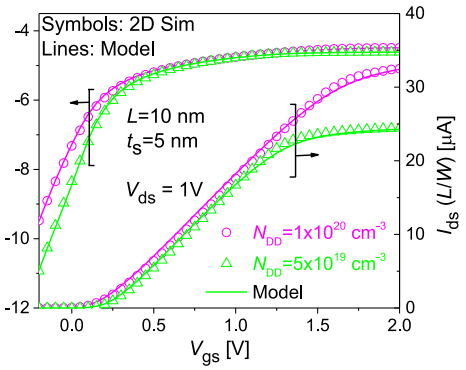

FIGURE 8. Simulated and modeled normalized $I - V$ characteristics at $V_{ds} = 1$V for different drain-doping concentrations with $L = 10$nm and $t_s = 10$nm.

part, including the velocity saturation effect [25], [26]. The impurity-concentration difference between the channel N_A and the drain drift region N_{DD} as well as the drift length L_{drift} determine the potential V_{dp}.

For the expansion of the depletion region, mainly observed during subthreshold operation of short-channel transistors, the potential difference V_{di} is modulated by the potential drop along the depletion region formed at the drain side (see Fig. 6) [14], [26], [27]

$$V_{di} = V_{dp} + V_{biDrain} - V_{biSource} - E_{Drain} \cdot W_{dep\_D}/2 \quad (9)$$

where the last term is the additional potential drop at the drain side, caused by a lower space-charge density.

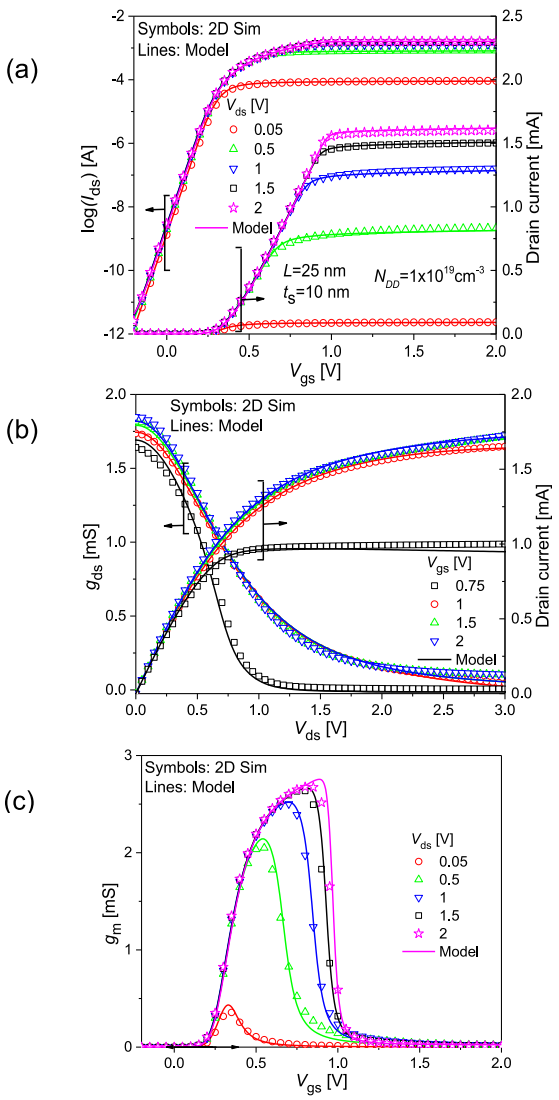

FIGURE 9. (a) Simulated and modeled $I_{ds} - V_{gs}$ characteristics of the studied device for different V_{ds} values, (b) comparison for transconductance characteristics g_m *vs.* V_{gs} for different V_{ds} values, (c) comparison of the drain current and the output-conductance characteristics for different V_{gs} values.

Fig. 7 compares the model calculation results with 2D-device simulation results for $N_{DD} = 10^{19}$ cm^{-3}. As an additional comparison, the results for $N_{DD} = 10^{20}$ cm^{-3} are depicted together. It can be seen that the subthreshold-slope degradation is improved drastically for both low and high V_{ds} with reduced N_{DD}. It is also seen that the drain-resistance effect is strongly enhanced for reduced channel length. Figure 8 shows that these features are still observable for reduced device size.

Figure 9 summarizes the accuracy of the developed model, valid for a high-voltage DG-MOSFET, in comparison to 2D-device simulation results, considering the device structure depicted in Fig. 1a with $N_{DD} = 1 \times 10^{19}$cm^{-3}. Subfigures (a) and (b) depict $I_{ds} - V_{gs}$ characteristics and transconductances g_m for different V_{ds} values, respectively. The output characteristic with I_{ds} and output conductance g_{ds} is shown for

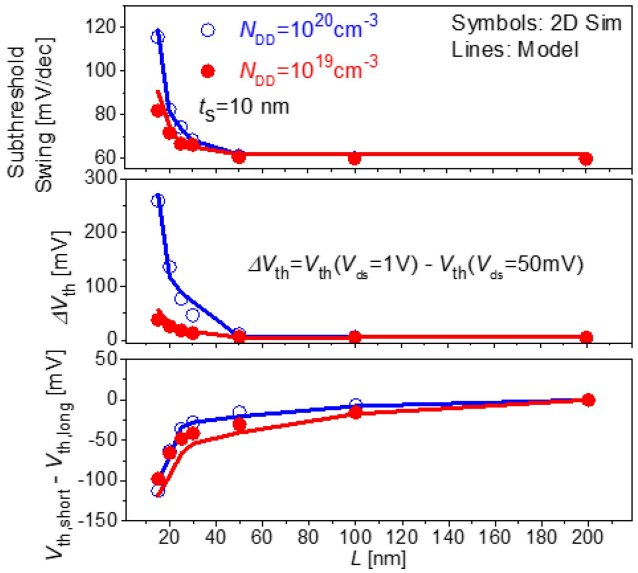

FIGURE 10. Comparison of the extracted short-channel-effect (SCE) parameters (subthreshold swing, threshold voltage reduction and threshold-voltage roll-off) for simulated and modeled device characteristics considering high and low drain-doping concentrations as a function of the channel length *L*.

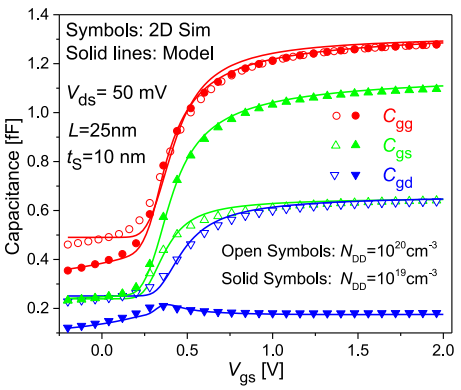

FIGURE 11. Simulated and modeled $C-V$ characteristics at V_{ds} = 50mV with N_{DS} of 10^{20} and $10^{19}cm^{-3}$.

different V_{gs} bias conditions in Fig. 9c. All characteristics demonstrate the specific features of high-voltage MOSFETs. It can be seen that the reduced $N_{DD} = 1\times10^{19}cm^{-3}$ causes a rather abrupt drain-current saturation for large V_{gs} values, resulting in a steep reduction of g_m. The $I_{ds}-V_{ds}$ characteristics in Fig. 9c show nearly no V_{gs} dependency, which is called the quasi-saturation behavior. All these resistance effects are well reproduced.

In Fig. 10 the specific SC parameters are depicted and compared with a geometrically identical device, but having larger drain doping $N_{DD} = 10^{20}$ cm^{-3}. In these comparisons, the suppression of SCEs is effectively observed, namely, improved subthreshold slope and hugely reduced V_{ds} impact on threshold voltage V_{th} are achieved, while a similar reduction magnitude in the V_{TH} roll-off is kept.

Capacitance characteristics are also evaluated and compared to 2D device simulation results. Figure 11 shows

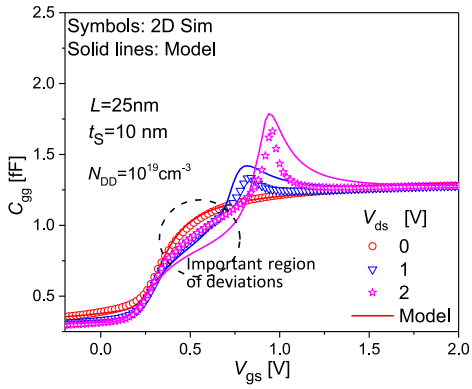

FIGURE 12. 2D-simulated and modeled $C-V$ characteristics for different V_{ds} values with N_{DS} of $10^{19}cm^{-3}$. A deviation in the incircled region (which is very important for circuit design) and for the C_{gg} peaks at higher V_{ds} is observed.

the comparison of the intrinsic capacitance part at $V_{ds} = 50$mV. The model-parameter values for the simulation are those extracted from the $I-V$ characteristics (see Fig. 7). C_{gg} is nearly identical for both drain-doping concentrations when $V_{gs} \geq V_{TH}$, while a clear difference is observed when $V_{gs} < V_{TH}$. Under the strong-inversion condition for $V_{gs} \geq V_{TH}$ the gate control is strong enough, so that all carriers are collected at the surface and influenced by the V_{gs} induced field. For $V_{gs} < V_{TH}$ on the contrary, carriers are influenced by the field induced by V_{ds}, resulting in a V_{ds} dependence.

The drain-resistance effect causes asymmetrical characteristics for C_{gs} and C_{gd} due to the asymmetrical contact formation, $N_{DD} \leq N_{DS}$. The short-channel effects are due to the punch-through current flowing deep in the middle between the channels, which is mostly observed in the subthreshold region of I_{ds}. Since the corresponding deep charge contributes only negligibly to the total capacitance, where the gate capacitance dominates, diminished short-channel effects are expected in the capacitances.

The effect of SCEs on capacitances is proportional to the change of $\Delta\phi_{min}$ with respect to the bias nodes V_s, V_d or V_g. A low N_{DD} is expected to reduce the $\Delta\phi_{min}$ increase and its rate of change. However, the high-voltage DG-MOSFET with a short-channel length shows a clear deviation of the model-calculation results for C_{gg} in comparison to 2D-device simulation results, as demonstrated in Fig. 12 (see the encircled very important region of deviations) for different V_{ds} values while keeping $N_{DD} = 1\times10^{19}cm^{-3}$. This deviation is specific for a short-channel device with lightly-doped drain contact (see also Fig. 4) and is further explained in the next section.

III. INVESTIGATION FOR HIGH VOLTAGE MG-MOSFET

A. INTRINSIC CAPACITANCE

Capacitances are derivatives of charges on nodes, and charges are a function of the potential distribution along the channel. Position-dependent charges are integrated along the channel to calculate the node charges under the drift-diffusion

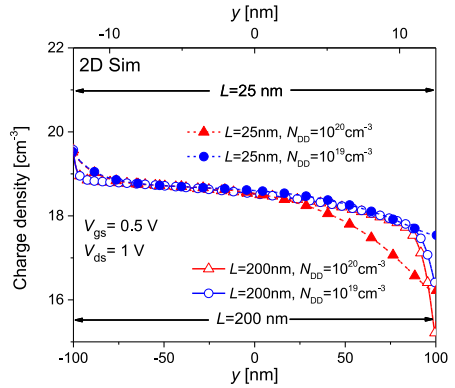

FIGURE 13. Simulated charge density at $V_{gs} = 0.5$ V and $V_{ds} = 1$V along the channel for $L = 200$ and 25nm with different N_{DD} of 10^{19} and 10^{20} cm^{-3}.

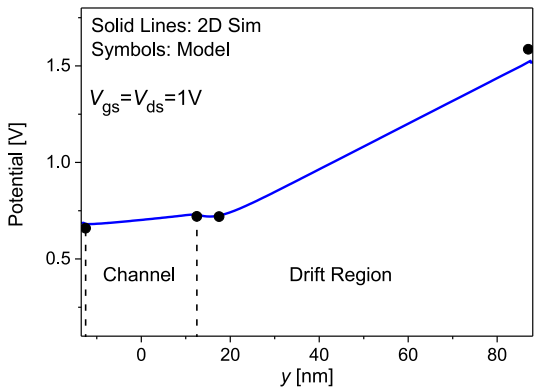

FIGURE 14. Potential comparison along the channel between simulation and modeled results for $L = 25$nm and N_{DD} of 10^{19} cm^{-3}.

approximation. Since the impurity concentration of the DG-MOSFET generation is quite low, the depletion charge is neglected to obtain a simple analytical equation for the charges

$$Q_g = 2W \int_0^L Q_i(y)dy \tag{10}$$

$$Q_g = 2WL\beta C_{ox}^{-1} I_{dd}^{-1} \cdot \left(\frac{Q_{nL}^3 - Q_{n0}^3}{3} + \beta^{-1} \cdot \frac{Q_{nL}^2 - Q_{n0}^2}{2} \right) \tag{11}$$

where

$$dy = -\frac{\mu_{eff} W}{I_{ds}} \left[Q_i(y) d\phi_S - dQ_i(y) \right] \tag{12}$$

$$I_{dd} = (Q_{nL} - Q_{n0}) - \frac{\beta}{2} \cdot (Q_{nL} + Q_{n0}) \cdot (\phi_{SL} - \phi_{S0}) \tag{13}$$

while Q_i is the inversion charge distribution along the channel.

The derivatives of the charges with respect to bias voltages derive the intrinsic capacitances [28]. Figure 4 shows that the applied approximations cause no serious problem for the highly doped N_{DD}. C_{gg} shows plateaus at 2/3 of C_{ox} for high V_{ds} values under the saturation condition. However, the plateau values are clearly higher for the resistive drift case (see Fig. 12).

The physical reason for a model underestimation of the plateau value can be extracted from a charge point of view analysis. Figure 13 shows 2D-device simulation results of the inversion-charge distribution along the channel. It can be seen that the distributions for $N_{DD} = 1 \times 10^{20}$cm^{-3} and $N_{DD} = 1 \times 10^{19}$cm^{-3} are quite different for the $L = 25$nm case. No substantial inversion-charge-density reduction is observed at the drain junction for the short-channel transistor with $N_{DD} = 1 \times 10^{19}$cm^{-3}. The reason is the resistive drift region, where most of the potential increase is sustained. In our modeling approach for the conventional highly doped drain contact, only the channel part is calculated by solving the Poisson equation, and the potential increase due to the high V_{ds} value is considered to occur at the junction causing the pinch-off condition. However, for the high voltage DG-MOSFET case, the potential distribution of not only the channel part but also of the overlap region must be consistently considered in addition, in order to reproduce the plateau levels. The reality is that the impurity profile at the channel/drain junction is hardly known, and furthermore, the quasi-Fermi potential difference among different regions is hard to incorporate self-consistently in the compact modeling. Figure 14 compares the model-calculation result of the potential distribution along the device to that of the 2D-device simulation, where a slight deviation is detected at

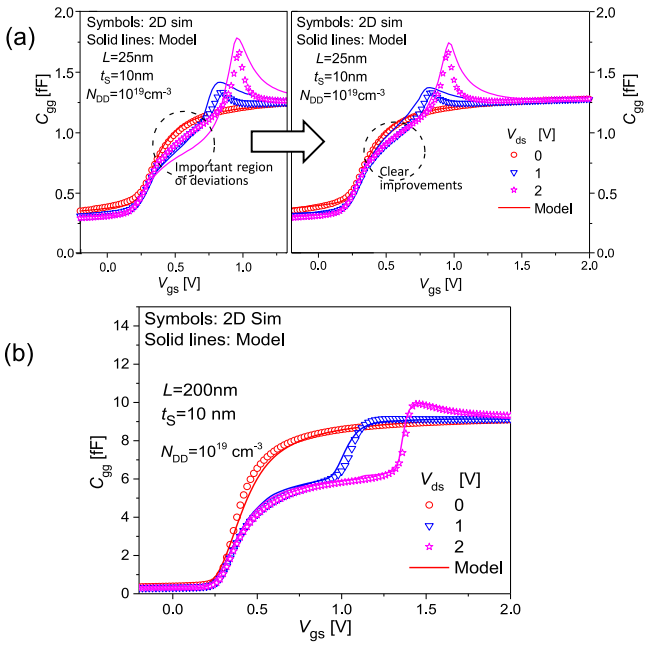

FIGURE 15. 2D-simulated $C - V$ characteristics in comparison to modeled $C - V$ characteristics with the developed capacitance-modeling improvements at different V_{ds} values with N_{DS} of 10^{19}cm^{-3} for (a) $L = 25$nm and (b) $L = 200$nm. In (a) the results without (left, see also Fig. 12) and with (right) the capacitance-modeling improvements are shown side by side. The definition of symbols and lines is the same in all subfigures.

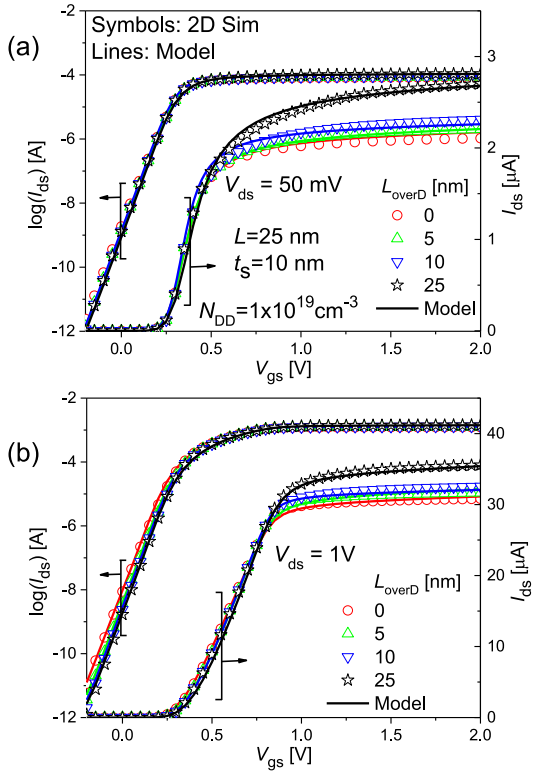

FIGURE 16. Simulated and modeled transfer characteristics for $L = 25$nm at $N_{DD} = 10^{19}$ cm^{-3} for different gate overlap lengths at (a) $V_{ds} = 50$mV and (b) 1V.

the drain contact. This small deviation causes the difference in the plateau level. Therefore, we rather approximate the inversion-charge distribution by a polynomial function of the position along the channel as

$$Q_i(y) = Q_{n0} + \frac{Q_{nL} - Q_{n0}}{L^n} y^n \tag{14}$$

which derives an analytical equation of the integrated inversion charge. The extracted exponent n is four for our studied case. Calculation results with the new improved model description are compared in Fig. 15 with 2D-device simulation results. Clear improvements in the encircled very important region for circuit design can be seen. The peaks observed in the C_{gg} characteristics indicate the transition point between the intrinsic MOSFET control and the drain resistance effect. C_{gg} often exceeds the C_{ox} value at this transition point.

B. L_{OVER} DEPENDENCE

In high-voltage MOSFETs, the overlap length L_{over} is usually quite long, in order to increase the maximum drivable drain current. However, the L_{over} length can influence the subthreshold characteristics as is demonstrated in Fig. 16 for our studied DG-MOSFET. The developed short-channel effect modeling is further extended by considering the accumulated charge within the overlap region Q_{over}, which is calculated by solving the Poisson equation between the gate and the

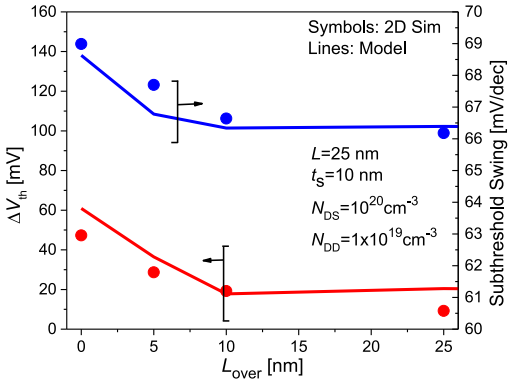

FIGURE 17. Comparison of the extracted short-channel-effect parameters for simulated and modeled device characteristics as a function of the overlap length.

overlap region. This charge contributes to the total capacitances of the high-voltage MG-MOSFET in addition to the intrinsic part. The charge changes the field E_{Drain} considered for the SC effect modeling (See Table 1). Since a slight potential increase exists within the overlap region, Q_{over} is not homogeneous along L_{over}. This is modeled by a length modulation as a function of V_{ds}. Thus, the equation for V_{di} is modified as

$$V_{di} = V_{dp} + V_{biDrain} - V_{biSource} - E_{Drain} \cdot W_{dep\_D}/2 - E_{ov} L'_{over} \tag{15}$$

$$E_{ov} = Q_{over}/\varepsilon_{Si} \tag{16}$$

$$L'_{over} = L_{over} \cdot \left(\alpha V_{ds}^{m} E_{Drain}\right) \tag{17}$$

where, α and m are model parameters for the Q_{over} distribution and the L_{over} modulation.

The $I_{ds} - V_{gs}$ characteristics in Fig. 16 shows that the subthreshold region is correctly modeled by considering the space-charge density of the drift region, while the increase of the maximum drain current, caused by the drain resistance effect, is also predicted.

Figure 17 depicts the improved subthreshold swing and ΔV_{th} modeling by including the L_{over} contribution. Good agreements reveal that the developed model can calculate the L_{over} variation accurately.

IV. CONCLUSION

A complete surface-potential-based compact model for the high-voltage multi-gate MOSFET is presented. For the modeling purpose, model equations are written on the basis of the drift-diffusion approximation, which realizes a smooth transition among different bias conditions. The model considers the short-channel effects as well as the highly resistive drain-contact-related effects by considering the potential distribution along the device explicitly. It was found that a slightly resistive drain-contact region suppresses the short-channel effects drastically. The slightly resistive drain affects also the potential distribution within the overlap region. Thus, a sufficiently long overlap length is capable to suppress the

short-channel effects as well. This leads to a diminished V_{ds} dependence of capacitances at the same time. The developed compact model has been implemented in a single model code, including all the presented equations and approaches, and was verified to be applicable for circuits containing leading-edge high-voltage multi-gate MOSFETs.

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