Received 5 August 2020; revised 1 October 2020; accepted 11 October 2020. Date of publication 14 October 2020; date of current version 10 November 2020.
The review of this article was arranged by Editor S. Ikeda.

*Digital Object Identifier 10.1109/JEDS.2020.3030923*

# 3D Simulation for Melt Laser Anneal Integration in FinFET's Contact

**TOSHIYUKI TABATA [1] (Member, IEEE), BENOIT CURVERS[1], KARIM HUET[1] (Member, IEEE), SOON AIK CHEW[2], JEAN-LUC EVERAERT[2], AND NAOTO HORIGUCHI[2] (Member, IEEE)**

1 Laser Systems and Solutions of Europe (LASSE), 92230 Gennevilliers, France
2 Semiconductor Technology and Systems Unit, imec, 3001 Leuven, Belgium

CORRESPONDING AUTHOR: T. TABATA (e-mail: toshiyuki.tabata@screen-lasse.com)

**ABSTRACT** Process integration feasibility of UV nanosecond melt laser annealing (MLA) in 14 nm node generation FinFET's contact for dopant surface segregation and activation is assessed by using a 3D TCAD simulation tool. In a n-type source/drain (S/D) in-situ phosphorous doped epilayer, Sb ion implantation is performed, considering the advantage of its surface segregation in lowering of the contact resistivity. The simulation results show that the heat sources created by the laser irradiation are confined mainly in the replacement metal gate (RMG) part, suggesting a potential interest of controlling the polarization of laser light to enlarge the process window by reducing the laser absorption in the RMG part. Also, the estimated solidification front velocity ($V$) in the MLA-induced epilayer regrowth ($\sim$4 m/s) satisfies the requirements ($\sim$1 m/s $< V <$ $\sim$15 m/s) to enable the surface segregation and metastable activation of the dopants. The surface segregation is also experimentally confirmed in the FinFET contact module.

**INDEX TERMS** Contacts, FinFET, melt laser anneal, TCAD.

## I. INTRODUCTION

Nowadays, the area of transistors is so small that metal-semiconductor contact resistivity dominates parasitic components of access resistance [1]. The improvement of the contact resistivity has therefore become more and more challenging in recent years and a target for future nodes is to achieve a value below $1 \times 10^{-9}$ ohm.cm$^2$ [2]. The required breakthrough is demonstrated for p-type contact by using gallium (Ga) as the dopant in high germanium (Ge) content silicon-germanium (SiGe) alloys [3], [4] and pure Ge [4], where a key phenomenon is dopant surface segregation during non-equillibrium solidification induced by nanosecond melt laser annealing (MLA). When a segregation coefficient of dopant in a semiconductor material containing a liquid ($l$) and solid ($s$) phase (i.e., melting) is much lower than the unity, this dopant diffuses into the $l$ phase at the $l/s$ interface. Indeed, Ga has a very small equilibrium segregation coefficient ($k_0$) in both Si (0.008 [5]) and Ge (0.071 to 0.078 [6], [7]). In the same context, antimony (Sb) can be a candidate for n-type contact because its reported equilibrium segregation coefficient is also very small in Si (0.023 [8]).

However, in the MLA-induced solidification, these $k_0$ values evolve as a function of the solidification front velocity (SFV) [9]. Since preferential placement of the dopants happens in the disordered $l$ region of the moving $l/s$ interface, a solute trapping phenomenon, which also depends on SFV (denoted as $V$ in the following) [10], has to be taken into account to discuss substitutional incorporation of the dopants in the regrown semiconductor material. The non-equilibrium segregation coefficient ($k_{ne}$) of the dopants monotonically increases when increasing $V$ (i.e., $k_0 < k_{ne}$ with $0 < V$) [9], [10]. When $V$ becomes larger than the speed of solute diffusion propagation ($V_D$), $k_{ne}$ becomes equal to the unity (i.e., $k_{ne} = 1$ with $V_D < V$) and this regime is called "complete solute trapping" leading to diffusionless solidification [10]. In our previous works [11]–[13], the degree of surpassing the solid solubility limit (SSL) of the dopants such as Sb and Ga as a function of SFV is systematically studied, using Sb-implanted Si and Ga-implanted $Si_{50}Ge_{50}$ epilayers. When $V$ becomes larger than $\sim$1 m/s, the dopant active level monotonically increases. This would be the case in real devices, where the volume of the implemented source/drain (S/D) contact epilayers is negligible

compared to the underlying Si substrate so that quite fast heat dissipation can be expected.

To enable both MLA-induced surface segregation and activation over SSL of the dopants, $V$ must satisfy $\sim$1 m/s $< V < V_D$ ($\sim$15 m/s [13]). Therefore, a process simulation able to extract SFV is necessary to assess the feasibility of MLA integration into contact activation in real devices. In addition, thermal budget management in a complex device structure is important to control the process window. In a typical replacement metal gate (RMG) flow of high-k/metal gate (HKMG) technologies, the contact anneal may come after the final gate stack formation [14], [15], where the MLA-induced epilayer regrowth has to be managed without damaging the gate and other surrounding functional modules. To that end, simulation is the only way of knowing distribution of heat sources in a device structure. The simulation of the MLA process thermal dynamics in 3D structures is challenging since it needs to solve self-consistently the heat equation coupled to the time-harmonic solution of Maxwell equations (laser light coupling), phase field, and species diffusion, including the temperature dependency of material parameters, phase change, and alloy fraction. Moreover, nanometer scale effects such as optical coupling and phase change have to be considered together with micrometer scale thermal diffusion effects for microsecond scale duration (i.e., time to return to equilibrium) with nanosecond scale time resolution. In this work, we use a TCAD package (named LIAB: LASSE Innovation Application Booster) [16] overcoming these challenges to simulate the MLA process in 3D structures by a careful optimization of the numerical meshing strategy, adapted boundary conditions, and an adaptive time-stepping algorithm. Specifically, the incident laser wave comes from the top of the simulated structure and a constant temperature of 300 K is set at the lower boundary of the system (i.e., at the bottom of a 700 µm thick coarsely meshed Si substrate). Moreover, a condition of symmetry is imposed on the left and right boundaries, which is consistent for the periodic simulation of the surrounding equivalent FinFETs. With this simulation tool, we assess the feasibility of the MLA integration in a FinFET fabrication process for dopant activation in the S/D contact epilayers.

## II. EXPERIMENTAL PROCEDURE

A 14 nm node generation FinFET fabrication process flow with RMG was used to form a n-type S/D contact module (Fig. 1(a)). The S/D epilayer was in-situ phosphorous (P) doped Si (Si:P). Ion implantation (I/I) of Sb atoms was applied with a nominal dose of about $5 \times 10^{15}$ at./cm$^2$, targeting an impurity projected range of about 5 nm from the surface of the Si:P epilayer. A UV nanosecond pulsed laser annealing (SCREEN-LASSE LT3100) was performed with stage at room temperature to enable the MLA-induced rapid regrowth of the part amorphized by I/I (a-Si:P). The simulated 3D structures is shown in Fig. 1(b), where the structural parameters such as the fin's pitch, width, and height were set at 45 nm, 14 nm, and 30 nm, respectively (more details are given in Fig. 1(c), (d), and (e)). This structure was periodically repeated in simulation. The detailed setup of our simulation is explained elsewhere [16].

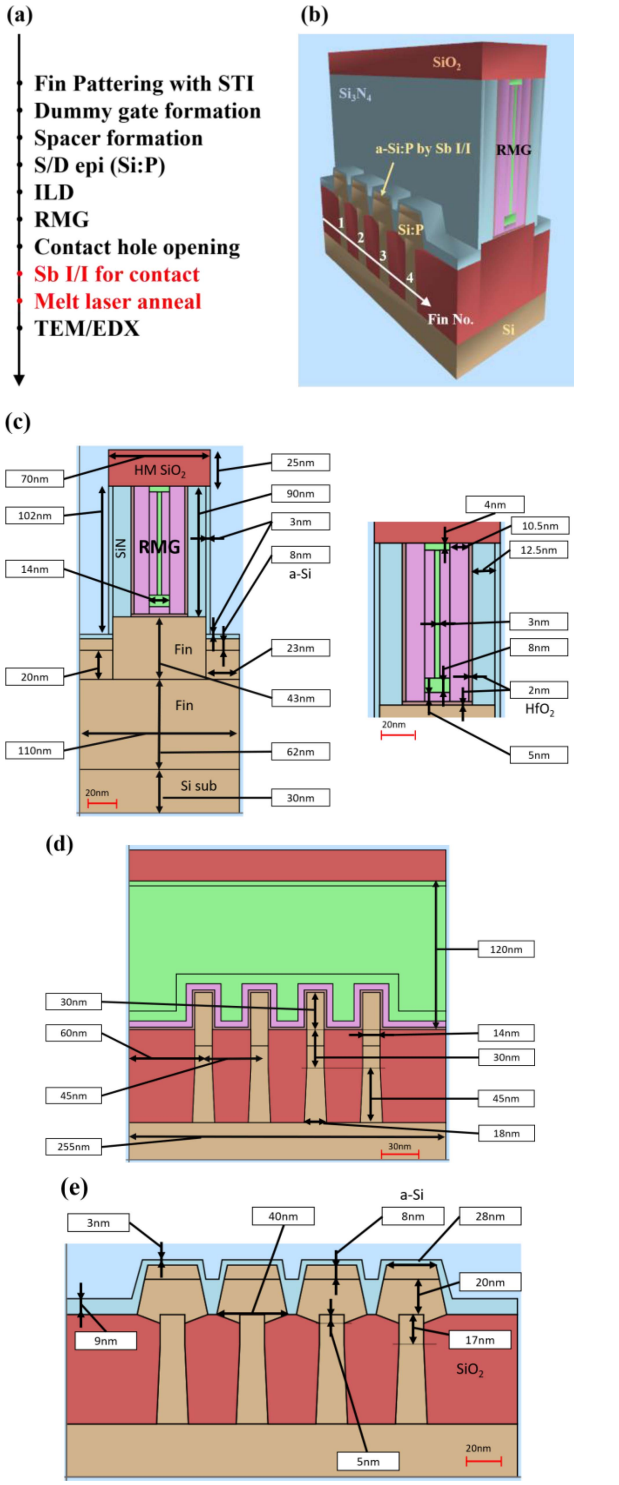


**FIGURE 1. (a) Process flow of our 14 nm node generation n-type FinFET up to contact anneal and physical characterization. (b) 3D structure used for our simulation. (c) Structural parameters with a cut on the Fin. (d) Structural parameters with a cut on the Gate. (e) Structural parameters with a cut on the S/D.**

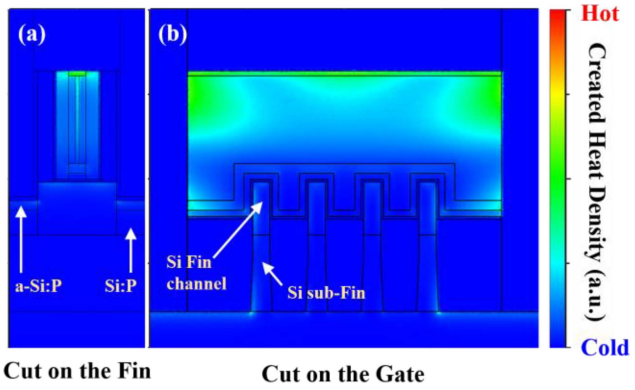


**FIGURE 2.** Color heat maps obtained by our simulation for the directions cut on (a) the Fin and (b) the Gate.

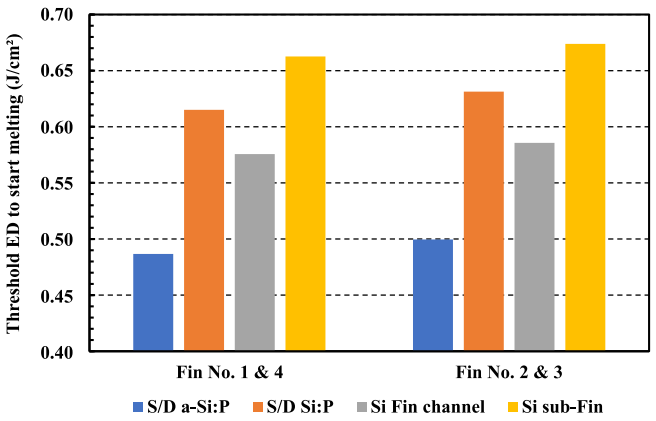


**FIGURE 3.** Extracted threshold ED values to start melting in the a-Si:P, Si:P, Si Fin channel, and Si sub-Fin on different Fin positions.

Physical characterizations such as Transmission Electron Microscopy (TEM) and Energy Dispersive X-ray (EDX) analysis were performed after MLA.

## III. RESULTS AND DISCUSSION

First, the distribution of heat sources created by the laser irradiation was extracted from the simulation along two directions: (i) cut on the Fin (Fig. 2 (a)) and (ii) cut on the Gate (Fig. 2 (b)). Most of the heat issued from the coupling between the laser light and the 3D structure is generated in the RMG metal regions. During the MLA process, this heat is transferred to the underlying Si Fin channel then to the S/D epilayers beside. This implies a potential risk of narrowing or losing the process window, because such strong heat generation in the Gate may induce degradation of the gate stack, possibly resulting in a threshold voltage shift and/or gate leakage increase in device operation.

To address this concern, the threshold laser energy density (ED) for melting the a-Si:P, Si:P, Si Fin channel, and underlying Si sub-Fin was estimated for all fin positions (described in Fig. 1(b)) as shown in Fig. 3. A similar trend as a function of increasing ED is observed regardless of the fin position. The a-Si:P melts at the lowest ED. Then, the Si Fin channel melts at a lower threshold than the Si:P. It

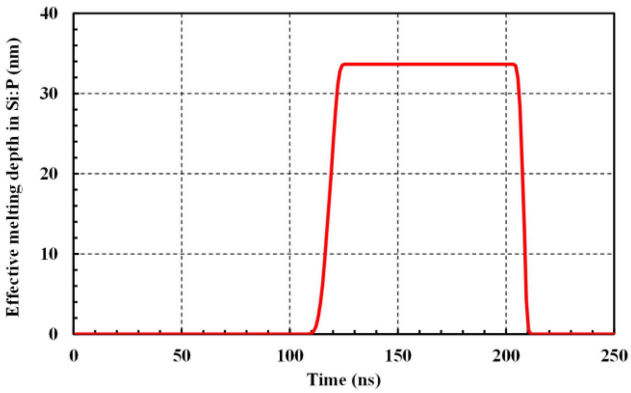


**FIGURE 4.** Extracted evolution of the melting depth in the case of the full melt of the initial Si:P epilayer. To roughly estimate the average SFV value, the maximum molten depth was divided by the time necessary to reduce the melting depth toward 0 nm.

should be noted that in our simulation the same melting point ($T_{melt}$) data ($\sim$ 1420 K and $\sim$ 1690 K in amorphous and crystalline states [17]) were used for both Si and Si:P (its nominal P concentration was about $1 \times 10^{21}$ at./cm$^3$), because the impact of doping on thermal properties was assumed to be minor. The lowest melting ED for the a-Si:P can be explained by its much lower $T_{melt}$ than the Si:P, whereas the lower melting ED of the Si Fin channel w.r.t. the Si:P is consistent with the heat transfer pathway from the heat source generated in the RMG region. To estimate a process window for MLA integration, the ED at which the a-Si:P fully melts must be at least lower than those of the beginning of the Si Fin channel and sub-Fin melting. According to our simulation, the full melt of the a-Si:P on all Fin positions can be achieved at 0.51 J/cm$^2$, leaving a comfortable margin of more than 0.05 J/cm$^2$. This process window may be enlarged by using a polarized laser light to reduce the laser light coupling (i.e., the heat generation) in the RMG part [16]. Also, when the a-Si:P melts, the RMG part reached a peak temperature higher than 1420 K (the obtained absolute temperature may be inaccurate since bulk material properties are considered for the RMG thin films in our model, but the RMG part could reach 1700 to 2000 K in a few hundred ns timescale). In contemporary 14 nm node generation FinFET HKMG technologies, a typical RMG flow may involve a high-temperature annealing (e.g., $\sim$900 °C for a few seconds [18]) as a post metallization anneal to improve the reliability of transistors. Although it is hard to predict a failure mode of possible HKMG performance degradation, the gate stack can survive such high-temperature heating thanks to the extremely short timescale of the applied MLA process (the applied laser pulse duration was in a range of 100 to 200 ns), as it has been already demonstrated experimentally on actual FinFET device structures [19]. The laser polarization may also help to avoid the gate damage.

To discuss the Sb surface segregation and activation, the SFV value in the current n-type FinFET structure was also estimated. From the evolution of the melting depth during MLA, which is shown in Fig. 4, an averaged SFV value was

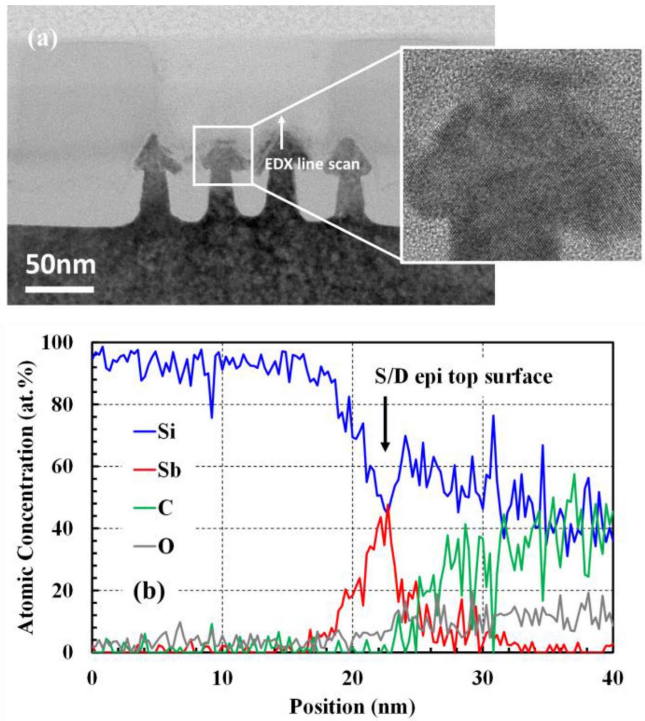


**FIGURE 5. (a) Cross-sectional TEM image of the n-type S/D contact module annealed at an MLA condition where the molten depth should be deeper than the initial Si:P epilayer thickness. (b) EDX line scan profile measured on one of the annealed Si:P S/D epilayers.**

calculated to be about 4 m/s for the initial Si:P full melt case. This value satisfies the above-mentioned requirement (i.e., $\sim$1 m/s $< V <$ $\sim$15 m/s) necessary to enable both Sb surface segregation and activation over SSL. An experimental evidence of Sb surface segregation is also presented in Fig. 5. An epitaxial-like regrowth was confirmed on a TEM image (Fig. 5(a)) at an MLA condition where the molten depth should be deeper than the initial Si:P epilayer thickness. Then, by an EDX line scan (Fig. 5(b)), a very high concentration of Sb atoms (about 40 at.%) was observed at the top surface of the regrown Si:P. Considering the diffusion coefficient of Sb in liquid Si ($1.5 \pm 0.5 \times 10^{-4}$ cm$^2$/s [20]) and the effective full melting time estimated in Fig. 4 (about 80 ns), the maximum diffusion length becomes equivalent to the initial Si:P epilayer thickness. This means that at the MLA condition of the presented TEM/EDX images the as-implanted Sb profile was once diluted in the molten Si:P when the melting front progressed deeper and deeper. Therefore, if the MLA-induced regrowth was a diffusionless process, then it would not have formed a peak of the Sb atoms in the EDX line scan only at the regrown Si:P surface. This observation supports that the mean SFV in the applied MLA process is smaller than $V_D$. A similar Sb redistribution mechanism during the MLA-induced rapid solidification is also reported in our previous work [13]. Then, one may expect a very high Sb active level which should be at least more than $\sim 2.6 \times 10^{20}$ at./cm$^3$ (equivalent to $\sim$0.5 at.%) [13] and potentially goes up to about 40 at.% (equivalent to $\sim 2 \times 10^{22}$ at./cm$^3$). This expectation in the $V$ range that we discuss in this work can be supported by a theoretical prediction of MLA-induced substitutional dopant incorporation in Si given by literature [21]. With such a high active level of the incorporated dopants at the contact interface, one may expect a very low contact resistivity which goes into a sub-$10^{-9}$ $\Omega$.cm$^2$ level [3], [4].

## IV. CONCLUSION

MLA integration in the 14 nm node generation FinFET process for contact activation was assessed by means of 3D TCAD simulation. The visualization of the heat transfer pathway is the key of tuning the process window. Also, the SFV extraction helps to configure the MLA-induced solute trapping regime for enabling the dopant surface segregation and metastable activation over SSL. In the actual FinFET structure, the MLA process dynamics were shown to be promising for contact resistivity lowering. Such approach will be also valid for future advanced CMOS devices.

## ACKNOWLEDGMENT

The authors would like to thank P. Kopalidis, D. Roh, E. Moore, R. Reece, H.-C. Tsai, and L. M. Rubin (Axcelis Technologies) for performing the ion-implantations.

## REFERENCES

[1] P. Raghavan *et al.*, "Holisitic device exploration for 7 nm node," in *Proc. CICC*, Mar. 2015, pp. 1–5, doi: 10.1109/CICC.2015.7338377.
[2] C.-N. Ni *et al.*, "Ultra-low NMOS contact resistivity using a novel plasma-based DSS implant and laser anneal for post 7 nm nodes," in *Proc. Symp. VLSI Technol.*, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573383.
[3] J.-L. Everaert *et al.*, "Sub-$10^{-9}$ $\Omega$.cm$^2$ contact resistivity on p-SiGe achieved by ga doping and nanosecond laser activation," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. 214–215, doi: 10.23919/VLSIT.2017.7998176.
[4] L.-L. Wang *et al.*, "Comprehensive study of Ga activation in Si, SiGe and Ge with $5 \times 10^{-10}$ $\Omega$·cm$^2$ contact resistivity achieved on Ga doped Ge using nanosecond laser activation," in *IEDM Tech. Dig.*, Dec. 2017, pp. 549–552, doi: 10.1109/IEDM.2017.8268441.
[5] M. Liaw and F. S. D'Aragona, "Sequential purification and crystal growth for the production of low cost silicon substrates," Motorola, Inc. Semicond. Group, Phoenix, AZ, USA, Rep. 3, Aug. 1980, doi: 10.2172/12229465.
[6] F. A. Trumbore, E. M. Porbansky, and A. A. Tartaglia, "Solid solubilities of aluminum and gallium in germanium," *J. Phys. Chem. Solides*, vol. 11, nos. 3–4, pp. 239–240, Oct. 1959, doi: 10.1016/0022-3697(59)90220-3.
[7] J. P. Garandet, "Estimation of liquid phase diffusion coefficients of gallium and antimony in Germanium from segregation data in crystal growth experiments," *J. Cryst. Growth*, vol. 310, pp. 3268–3273, Jul. 2008, doi: 10.1016/j.jcrysgro.2008.03.042.
[8] F. A. Trumbore, "Solid solubilities of impurity elements in Germanium and silicon," *Bell Syst. Technol. J.*, vol. 39, no. 1, pp. 205–233, Jan. 1960, doi: 10.1002/j.1538-7305.1960.tb03928.x.
[9] R. F. Wood, "Model for nonequilibrium segregation during pulsed laser annealing," *Appl. Phys. Lett.*, vol. 37, no. 3, pp. 302–304, Aug. 1980, doi: 10.1063/1.91914.
[10] P. Galenko, "Solute trapping and diffusionless solidification in a binary system," *Phys. Rev. E, Stat. Phys. Plasmas Fluids Relat. Interdiscip. Top.*, vol. 76, no. 3, Sep. 2007, Art. no. 031606, doi: 10.1103/PhysRevE.76.031606.
[11] T. Tabata, J. Aubin, K. Huet, and F. Mazzamuto, "Segregation and activation of Ga in high Ge content SiGe by UV melt laser anneal," *J. Appl. Phys.*, vol. 125, Jun. 2019, Art. no. 215702, doi: 10.1063/1.5096889.

[12] T. Tabata, K. Huet, F. Mazzamuto, and A. La Magna, "Surface segregated Ga, In, and Al activation in high Ge content SiGe during UV melt laser induced non-equilibrium solidification," *Jpn. J. Appl. Phys.*, vol. 58, Nov. 2019, Art. no. 120911, doi: 10.7567/1347-4065/ab55f7.
[13] T. Tabata, P.-E. Raynal, K. Huet, and J.-L. Everaert, "Segregation and activation of Sb implanted in Si by UV nanosecond-laser-anneal-induced non-equilibrium solidification," *J. Appl. Phys.*, vol. 127, Apr. 2020, Art. no. 135701, doi: 10.1063/5.0005176.
[14] D.-I. Bae *et al.*, "A novel tensile Si (n) and compressive SiGe (p) dual-channel CMOS FinFET co-integration scheme for 5nm logic applications and beyond," in *IEDM Tech. Dig.*, Dec. 2016, pp. 683–686, doi: 10.1109/IEDM.2016.7838496.
[15] C. H. Lee *et al.*, "A comparative study of strain and Ge content in Si1-xGex channel using planar FETs, FinFETs, and strained relaxed buffer layer FinFETs," in *IEDM Tech. Dig.*, Dec. 2017, pp. 820–823, doi: 10.1109/IEDM.2017.8268509.
[16] S. F. Lombardo *et al.*, "Theoretical study of the laser annealing process in FinFET structures," *Appl. Surf. Sci.*, vols. 467–468, pp. 666–672, Feb. 2019, doi: 10.1016/j.apsusc.2018.10.155.
[17] A. La Magna, P. Alippi, V. Privitera, G. Fortunato, M. Camalleri, and B. Svensson, "A phase-field approach to the simulation of the excimer laser annealing process in Si," *J. Appl. Phys.*, vol. 95, no. 9, pp. 4806–4814, Apr. 2004, doi: 10.1063/1.1690861.
[18] G. Rzepa *et al.*, "Efficient physical defect model applied to PBTI in high-$\kappa$ stacks," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 1–6, doi: 10.1109/IRPS.2017.7936425.
[19] O. Gluschenkov *et al.*, "External resistance reduction by nanosecond laser anneal in Si/SiGe CMOS technology," in *IEDM Tech. Dig.*, Dec. 2018, pp. 815–818, doi: 10.1109/IEDM.2018.8614628.
[20] H. Kodera, "Diffusion coefficients of impurities in silicon melt," *Jpn. J. Appl. Phys.*, vol. 2, no. 4, pp. 212–219, Apr. 1963, doi: 10.1143/JJAP.2.212.
[21] J. Narayan, "Interface instability and cell formation in ion-implanted and laser-annealed silicon," *J. Appl. Phys.*, vol. 52, no. 3, pp. 1289–1293, Dec. 1981, doi: 10.1063/1.329753.