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Asymmetric Low Metal Contamination Ni-Induced Lateral Crystallization Polycrystalline-Silicon Thin-Film Transistors With Low OFF-State Currents for Back-End of Line (BEOL) Compatible Devices Applications

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ABSTRACT In this work, polycrystalline-silicon thin-film transistors (poly-Si TFTs) with asymmetric low metal contamination Ni-induced lateral crystallization (LC-NILC) poly-Si channel and high-κ HfO_2 gate insulator (GI) have been successfully fabricated and demonstrated for the first time. The amounts of Ni diffused into the poly-Si film can be effectively reduced by Ni removal processes prior to NILC. The asymmetric LC-NILC poly-Si TFTs exhibit higher field-effect mobility (μ_{FE}), steeper ideal subthreshold swing (S.S.), larger ON/OFF currents ratio (I_{ON}/I_{OFF}), better uniformity, and improved C-V curves compared to traditional NILC (T-NILC) poly-Si TFTs owing to better crystallization quality and less low metal contamination. These remarkable device characteristics and the matched complementary TFTs (C-TFTs) electrical characteristics with low I_{OFF} and low operation voltages make the asymmetric LC-NILC poly-Si TFTs promising for the future back-end of line (BEOL) compatible devices applications in monolithic three-dimension integrated circuits (3D-ICs).

INDEX TERMS High-κ, HfO_2 gate insulator (GI), low metal contamination (LC), Ni-induced lateral crystallization (NILC), poly-Si thin-film transistors (poly-Si TFTs), complementary TFTs (C-TFTs), back-end of line (BEOL), monolithic three-dimension integrated circuits (3D-ICs).

I. INTRODUCTION

Recently, monolithic three-dimension integrated circuits (3D-ICs) are emerging technologies for the applications of artificial intelligence (AI) and Internet of Things (IoT) owing to its high density of device per chip area and direct connectivity of circuit with low power consumption and improved system performance [1], [2]. For monolithic 3D-ICs, low thermal budget processes are essential for fabricating back-end of line (BEOL) circuits. It had been reported that the SPC (solid phase crystallization) gate-all-around (GAA) poly-Si nano-wire (NW) transistors [3] and the laser crystallization poly-Si FinFET fabricated by chemical-mechanical planarization (CMP) [4]–[6] could potentially be used as back-end of line (BEOL) compatible devices in monolithic 3D-ICs.

It is well-known that electrical characteristics of poly-Si TFTs can be improved if the poly-Si grain size can be enlarged and the number of grain boundaries in the channel

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can be reduced. Metal-induced lateral-crystallization (MILC) with crystal filtering structures have been studied in the past to achieve better carrier mobility performance of poly-Si TFTs [7]–[9]. However, they mostly suffer the issues including poor device uniformity, large operation voltage (high power consumption), and high off-state currents (I_{OFF}) due to serious metal contamination. Previously, we have proposed the symmetric low metal contamination Ni-induced lateral crystallization (LC-NILC) polycrystalline-silicon thin-film transistors (poly-Si TFTs) with plasma-enhanced chemical vapor deposition (PECVD) SiO_x gate insulator (GI) [10]. The experimental results display that the novel LC-NILC processes can effectively reduce the accumulation and contamination of Ni in the channel region compared to the symmetric traditional NILC (T-NILC) processes.

In addition, hydrogen-related plasma passivated processes are well-known technologies to passivate the Si dangling bonds at GI/poly-Si interface, grain boundaries trap states, and intra-grain defects in the poly-Si films for improvements in electrical characteristics. Nevertheless, the weak Si-H bonds are easily broken under stress in hydrogen-related plasma passivated devices, leading to more serious reliability issues [11]. Furthermore, high-κ materials such as Al_2O_3 and HfO_2 have been used as the GI of poly-Si TFTs to enhance the gate-capacitance density, resulting in lower operation voltage and the improvement of the subthreshold swing (S.S.) without any hydrogen-related plasma treatments [12]–[14].

The main difference between symmetric LC-NILC and asymmetric LC-NILC is the design of Ni-seeding windows. The symmetric LC-NILC devices were fabricated by using two symmetric Ni-seeding windows (NIC regions) on the source-side and the drain-side. Consequentially, the front-end grain boundaries of lateral crystallization, which grows from the source-side NIC region and the drain-side NIC region, will converge in the center of the channel due to the symmetric structure of Ni-seeding windows. Compared to T-NILC, the Ni-contamination in the center of channel can be effectively reduced by LC-NILC processes. However, the experimental results showed that there still were accumulation and contamination of Ni in the center of channel for symmetric NILC devices [10].

In this work, the asymmetric LC-NILC poly-Si TFTs with single Ni-seeding windows (NIC region) on the source-side without any hydrogen-related plasma treatments have been successfully fabricated and demonstrated. The asymmetric LC-NILC poly-Si TFTs consisted of asymmetric LC-NILC processes and high-κ HfO_2 GI not only reduce contamination of Ni but also make the accumulation of Ni far away from channel and junction region, resulting in better electrical characteristics compared to symmetric LC-NILC poly-Si TFTs.

II. DEVICES DESIGN AND EXPERIMENTS

The key process flow of the asymmetric LC-NILC, asymmetric T-NILC, and SPC poly-Si TFTs is shown in Fig. 1. All devices were fabricated on Si wafers grown with a 550nm

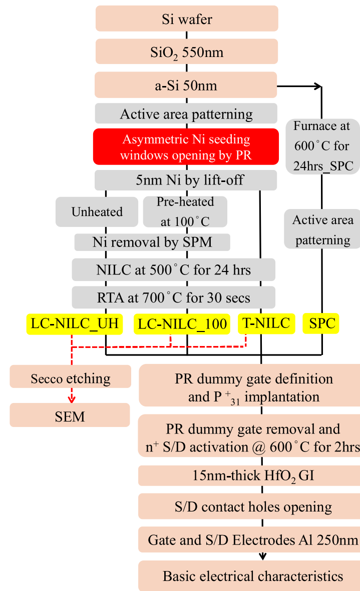

FIGURE 1. The key process flow of the asymmetric LC-NILC, asymmetric T-NILC, and SPC poly-Si TFTs.

thermal oxide layer. First, a 50nm-thick amorphous Si (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD). Then, the active region (AA) was patterned and etched by lithography and dry etching. In order to achieve crystal filtering structures, the a-Si film was patterned into the AA prior to NILC processes. After AA patterning, the asymmetric Ni seeding windows were opened by using lithography photoresist (PR). Second, a 5nm-thick Ni layer was deposited by an electron-beam evaporation and patterned by lift-off process as a seeding layer to crystallize the a-Si.

After Ni lift-off processes, the LC-NILC devices were treated with pre-heated processes by using a hot-plate under different temperatures. We discovered that Ni can be naturally reacted with the surface of poly-Si during deposition of Ni. However, the amount of Ni atoms into the a-Si thin films of Ni seeding windows before NILC should be not uniform. In order to form appropriate and uniform amount of Ni atoms into the a-Si thin films of Ni seeding windows before NILC, LC-NILC poly-Si TFTs were treated with extra pre-heated processes by using a hot-plate under an appropriate low temperature. We have studied the effects of pre-heated temperature in our previous work [10]. The experimental results show that when the pre-heated temperature is higher than 150°C, the electrical characteristics like I_{ON}, I_{OFF}, and S.S. will be significantly degraded [10]. These degradations may be due to excess amount of Ni atoms into the a-Si thin films of Ni seeding windows after high-temperature pre-heated processes. Therefore, the appropriate pre-heated temperature is set $\leq$ 100°C. In this work, the LC-NILC devices were divided into two groups: LC-NILC_UH (unheated) and LC-NILC_100 (pre-heated at 100°C).

In LC-NILC devices, the excess Ni was removed by SPM solution (H_2SO_4:H_2O_2 = 3:1 at 120°C) before NILC

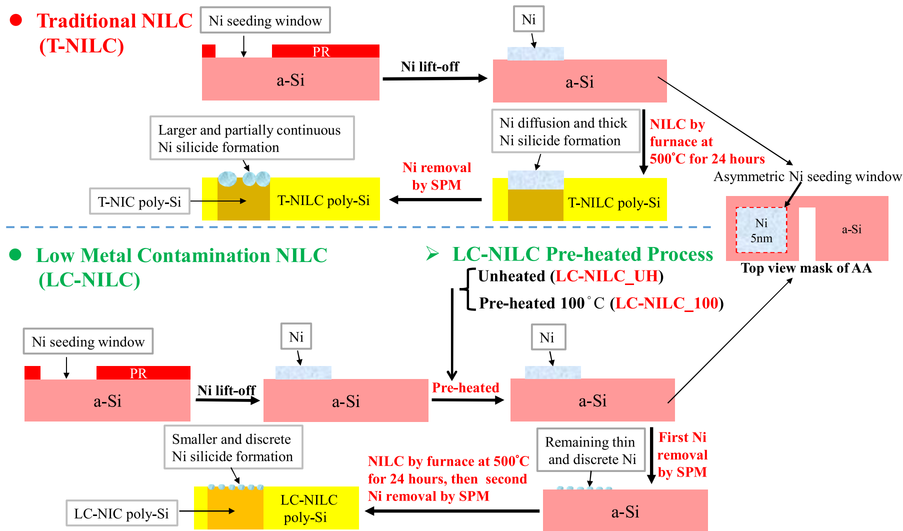

FIGURE 2. The detail comparisons of T-NILC and LC-NILC processes. The LC-NILC devices were divided into two groups: LC-NILC_UH and LC-NILC_100. Before NILC processes, the excess Ni was removed by SPM.

processes to reduce the Ni contamination. As a comparison, the traditional NILC (T-NILC) devices were fabricated as control ones without pre-heated and Ni removal processes prior to NILC. Third, the a-Si channel region of AA was laterally crystallized into a poly-Si film by NILC process by the furnace at 500°C for 24 hours in an N_2 ambient. The detail comparisons of T-NILC and LC-NILC processes are shown in Fig. 2. Ni reacted with Si atoms to form Ni silicide seeding layers during Ni deposition and sequent thermal processes. In Ni seeding window of LC-NILC devices, the excess Ni was removed, and the thin and discrete Ni was remained by the additional Ni removal processes prior to NILC processes, resulting in smaller and discrete Ni silicide after NILC processes in NIC region.

Then, a secondary recrystallization of NILC poly-Si films was performed by rapid thermal anneal (RTA) at 700°C for 30secs. This low thermal budget RTA process after NILC can enhance the grain size and improve the crystal integrity through secondary recrystallization [15]. After that, some samples were treated by Secco-etching solution ($HF + K_2Cr_2O_7 + H_2O$) for scanning electron microscope (SEM) analysis. After PR dummy gate definition, the n^+ source/drain (S/D) region was implanted with phosphorus (P^+_{31}, 5×10^{15} cm^{-2} at 10keV). Then, the PR dummy gate was removed by SPM solution and the dopants were activated by the furnace at 600°C for 2 hours in an N_2 ambient. Finally, a 15nm-thick HfO_2 gate insulator (GI) was deposited by Atomic Layer Deposition (ALD) at 250°C. After the S/D contact holes patterning, a 250nm-thick Al layer was deposited by thermal evaporation system as the gate and S/D electrodes. In order to study the effects of grain size in electrical characteristics, we also have fabricated the conventional solid phase crystallization (SPC) poly-Si TFTs with the same 15nm-thick HfO_2 GI. The SPC poly-Si channel film was crystallized by the furnace at 600°C for 24 hours

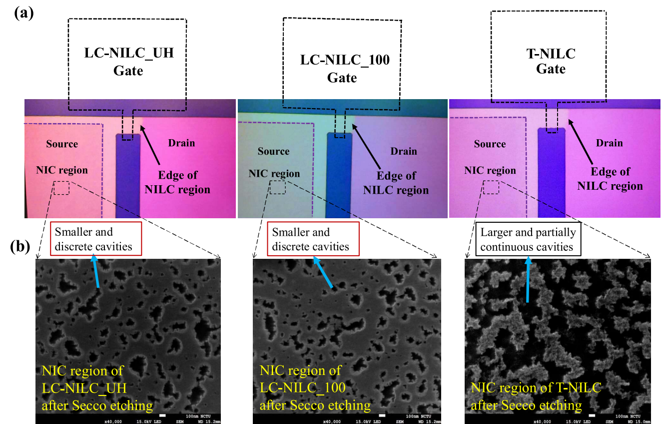

FIGURE 3. (a) The OM images of AA after NILC processes and (b) the SEM micrographs of Secco-etched poly-Si films in NIC region of Ni seeding window for LC-NILC_UH, LC-NILC_100, and T-NILC.

in an N_2 ambient. In this work, all devices were fabricated without any hydrogen-related plasma passivated processes.

III. RESULTS AND DISCUSSION

Figure 3 display (a) the optical microscope (OM) images of AA after NILC processes and (b) the SEM micrographs of Secco-etched poly-Si films in NIC region of Ni seeding window for LC-NILC_UH, LC-NILC_100, and T-NILC. In order to completely crystallize the a-Si into poly-Si in the channel region, we control the NILC time to adjust the edges of the NILC region beyond the gate edges near the drain side. In Fig. 3 (a), the growth rates of lateral crystallization in LC-NILC devices are almost the same as that in T-NILC. The pre-heated and Ni removal processes of LC-NILC devices are utilized to control less diffusion of Ni atoms into the a-Si thin films of Ni seeding windows. These results indicate that the LC-NILC processes do not reduce the growth rate of

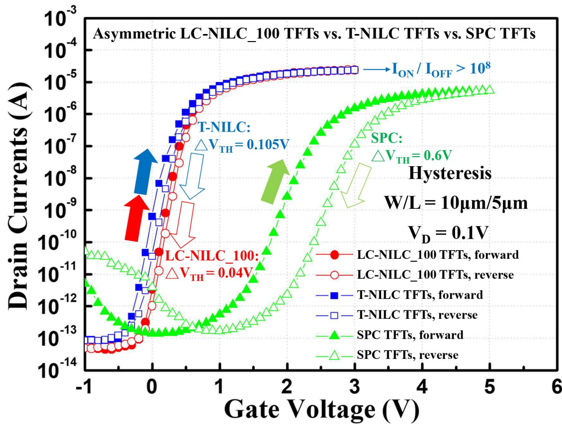

FIGURE 4. The transfer and hysteresis characteristics of LC-NILC_100, T-NILC, and SPC poly-Si TFTs.

lateral crystallization compared to T-NILC. In Fig. 3 (b), the Ni silicide were selectively etched by Secco-etching solution, resulting in these cavities in Ni seeding windows (NIC region). The NIC region of LC-NILC devices with smaller and discrete cavities that the fewer Ni residues in the Ni seeding windows of LC-NILC devices owing to the additional Ni removal processes prior to NILC processes. On the other hand, the SEM micrographs clearly indicate that there are larger and partially continuous cavities in the NIC region of T-NILC after Secco-etching treatments. The T-NILC devices without the extra Ni removal processes will remain the excess Ni residues in the Ni seeding windows, and then lead to more metal contamination in the channel and junction regions after NILC, which is the main reason for degradation of field-effect mobility (μ_{FE}) and high IOFF in T-NILC devices.

For low power consumption complementary TFTs (C-TFTs) applications, the real ON/OFF currents ratio (I_{ON}/I_{OFF}) under low gate operation voltages is a key parameter. Besides, measurement of hysteresis characteristics is also a convenient method to determine trap states at the interface between GI/poly-Si channels. Figure 4 shows the measured transfer and hysteresis characteristics of LC-NILC_ 100, T-NILC, and SPC poly-Si TFTs at $V_D = 0.1V$. Compared to SPC poly-Si TFTs, the LC-NILC_100 and T-NILC poly-Si TFTs exhibit steeper S.S. and smaller threshold voltage (V_{TH}), resulting in lower gate operation voltage. I_{OFF} is defined as the minimum OFF-currents (I_{min}) and I_{ON} is defined as the maximum ON-currents at $V_G = 3V$. It is noteworthy that the I_{ON}/I_{OFF} of LC-NILC_100 and T-NILC poly-Si TFTs are both larger than 10^8 as shown in Fig. 4.

It is well-known that the I_{OFF} of poly-Si TFTs is much higher than that of single-crystal Si MOSFETs, primarily because of traps and defects in the grain boundaries. The grain boundaries will generate leakage currents at the drain junction through the thermionic-field emission assisted by the high density of tail states within the poly-Si energy bandgap [16]. In Fig. 4, the n-channel SPC poly-Si TFTs always suffer from higher I_{OFF} due to smaller grain sizes and more grain boundaries in the SPC poly-Si films, resulting in poorer S.S., larger gate operation voltage, lower I_{ON}/I_{OFF}, smaller μ_{FE}, and more serious hysteresis characteristics compared to LC-NILC_100 and T-NILC poly-Si TFTs. It is worth noting that the LC-NILC_100 poly-Si TFTs display the best hysteresis characteristics ($\Delta V_{TH} = 0.04V$) owing to the less metal contamination and better crystallization quality.

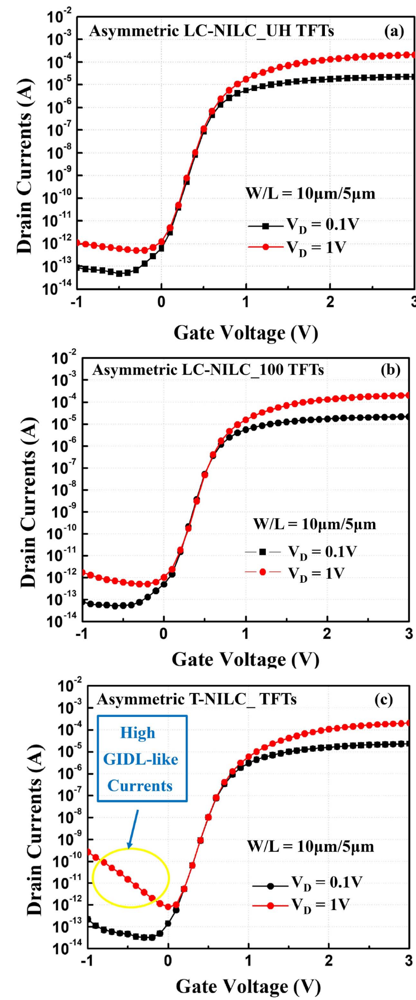

FIGURE 5. The measured transfer curves of (a) LC-NILC_UH, (b) LC-NILC_100, and (c) T-NILC poly-Si TFTs. All devices show almost the same electrical characteristics except the off-state GIDL-like currents at large drain bias ($V_D = 1V$) in T-NILC poly-Si TFTs.

Figure 5 exhibits the measured transfer curves of (a) LC-NILC_UH, (b) LC-NILC_100, and (c) T-NILC poly-Si TFTs. All devices show almost the same electrical characteristics except the off-state gate-induced drain leakage (GIDL)-like currents at large drain bias ($V_D = 1V$), which may be attributed to the more metal contamination in the channel and junction regions for T-NILC poly-Si TFTs, even such thin 5nm Ni layer. In this work, the uniformity was studied by extracting of electrical parameters, such as V_{TH}, S.S., μ_{FE}, and I_{ON}/I_{OFF}. Figure 6 displays the box charts of (a) V_{TH}

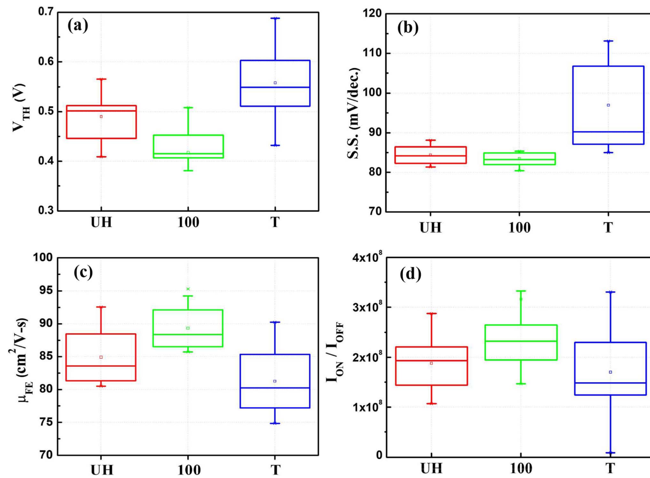

FIGURE 6. The box charts of (a) V_{TH} (b) S.S. (c) μ_{FE}, and (d) I_{ON}/I_{OFF} ($V_D = 0.1V$) for LC-NILC_UH, LC-NILC_100, and T-NILC poly-Si TFTs. The higher uniformity and better electrical characteristics can be achieved in LC-NILC poly-Si TFTs compared to T-NILC poly-Si TFTs owing to the extra Ni removal processes, resulting in less metal contamination and better crystallization quality.

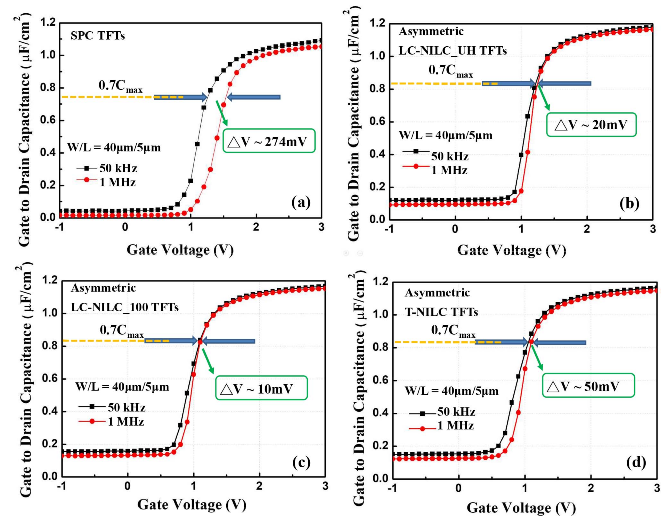

FIGURE 7. The measured C–V curves of (a) SPC, (b) LC-NILC_UH, (c) LC-NILC_100, and (d) T-NILC poly-Si TFTs with different frequencies. The LC-NILC devices have smaller ΔV than that in T-NILC and SPC poly-Si TFTs, which are consistent with the results of measured transfer curves and hysteresis characteristics.

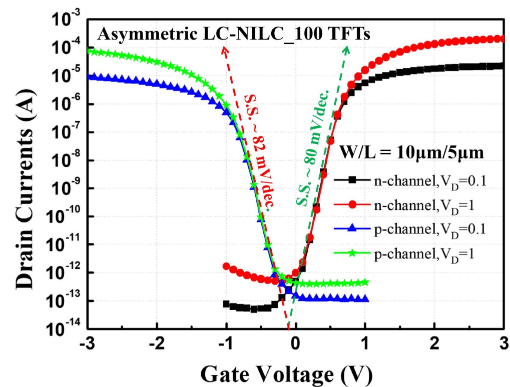

FIGURE 8. The measured complementary transfer curves of n-channel and p-channel LC-NILC_100 poly-Si TFTs with HfO_2 GI. There are matched complementary electrical characteristics with low I_{OFF} and low operation voltages.

(b) S.S. (c) μ_{FE}, and (d) I_{ON}/I_{OFF} ($V_D = 0.1V$) for LC-NILC_UH, LC-NILC_100, and T-NILC poly-Si TFTs. The distribution range of box charts represents the electrical uniformity of devices. The more concentrated the distribution range, the higher the electrical uniformity in the poly-Si TFTs. It is apparent that the higher uniformity and better electrical characteristics can be achieved in LC-NILC devices compared to T-NILC poly-Si TFTs owing to the extra Ni removal processes prior to NILC, resulting in less metal contamination and better crystallization quality. Furthermore, the LC-NILC_100 poly-Si TFTs were treated with extra pre-heated processes by using a hot-plate under an appropriate low temperature compared to LC-NILC_UH poly-Si TFTs. In Fig. 6, the box charts evidently indicate that the best uniformity and electrical characteristics are obtained in LC-NILC_100 poly-Si TFTs owing to the appropriate and uniform amount of Ni atoms into the a-Si thin films of Ni seeding windows before NILC. The LC-NILC devices with improved hysteresis characteristics, steeper S.S., reduced off-state GIDL-like currents, higher I_{ON}/I_{OFF}, and higher $\mu_{FE}$are more suitable for low power consumption C-TFTs applications compared to T-NILC and SPC poly-Si TFTs.

In order to verify the trap states in poly-Si TFTs, C–V measurement method was employed [17]. The variation in the C–V results as a function of the frequency allows us to identify the trap states at the interface of GI/channel or the grain boundary of poly-Si. The measured C–V curves of (a) SPC, (b) LC-NILC_UH, (c) LC-NILC_100, and (d) T-NILC poly-Si TFTs with different frequencies are shown in Fig. 7. The gate to drain capacitance (C_{GD}) was measured with a floating source. In Fig. 7 (a), the measured C–V curves of SPC poly-Si TFTs were obviously stretched out and significantly shifted in the positive direction with increasing frequency. The stretched out C-V curves may be attributed to more trap states at interface of GI/poly-Si channel and the parallel shifted C-V curves are due to larger trap states at the grain boundary of SPC poly-Si compared to LC-NILC devices [17]. The voltage shifts (ΔV) can be defined as the flat-band voltages ($\sim 0.7C_{max}$) differences between high/low frequencies. The measured C–V curves of LC-NILC devices are slightly stretched out and less shifted with increasing frequency. The LC-NILC devices have smaller ΔV than that in that in T-NILC and SPC poly-Si TFTs, which are consistent with the results of measured transfer curves, extracted electrical parameters, and hysteresis characteristics.

We also have fabricated p-channel LC-NILC_100 poly-Si TFTs for C-TFTs applications. Figure 8 illustrates the measured complementary transfer curves of n- and p-channel LC-NILC_100 poly-Si TFTs with HfO_2 GI. The proposed

n-channel LC-NILC TFTs can be integrated with p-channel LC-NILC TFTs as C-TFTs. The match of complementary electrical characteristics with steep S.S., low I_{OFF}, and low operation voltages in n- and p-channel LC-NILC poly-Si TFTs is observed to meet the requirement for C-TFTs applications. They offer new opportunities of designing low power consumption BEOL C-TFTs logic circuits.

IV. CONCLUSION

The combination of high-κ GI and n-/p-channel asymmetric LC-NILC poly-Si TFTs has been proposed for the first time. The experimental results display that the asymmetric LC-NILC devices have better electrical characteristics including the off-state GIDL-like currents, hysteresis, uniformity of basic parameters, and voltage shifts of C–V curves with different frequencies compared to the T-NILC and SPC poly-Si TFTs. These results suggest that asymmetric LC-NILC devices with low operation voltages and low leakage currents are the promising candidates to serve as the low power consumption BEOL compatible devices in monolithic 3D-ICs.

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