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Modeling of HCD Kinetics Under Full $V_G - V_D$ Space, Different Experimental Conditions and Across Different Device Architectures

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(Invited Paper)

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ABSTRACT A SPICE compatible compact modeling framework is discussed for Hot Carrier Degradation (HCD) stress spanning the entire drain (V_D) and gate (V_G) voltage space and wide range of temperature (T). It can model the HCD time kinetics measured using different methods such as shift in threshold voltage (ΔV_T), linear (ΔI_{DLIN}) and saturation (ΔI_{DSAT}) drain current and charge pumping current (ΔI_{CP}), for off and on-state stress. The model is validated using measured data from conventional, Lightly Doped Drain (LDD) and Drain Extended (DE) MOSFETs, FinFETs and Gate All Around Nano Sheet (GAA-NS) FETs. Parametric drift due to Bias Temperature Instability (BTI) stress in the presence of V_D is included. Impact due to Self-Heating (SH) and BTI-HCD coupling are considered. SPICE compatibility is shown by cycle-by-cycle simulation of various Ring Oscillator (RO) circuits.

INDEX TERMS HCD, BTI, self-heating, MOSFET, DEMOS, FinFET, GAA-NS FET, channel length and oxide thickness dependence, voltage and temperature dependence, SPICE, ring oscillator simulation, inverter, NAND, NOR.

I. INTRODUCTION

Hot Carrier Degradation has re-emerged as a crucial issue in modern n- and p- channel FETs having High-K Metal Gate (HKMG) gate insulator stack [1]–[3]. Although devices are typically tested at $V_G = n * V_D$ stress condition ($n \leq 1$) during process qualification, the V_G and V_D biases vary from 0V to VDD during an actual circuit operation [1], [4]. It is therefore necessary to develop a SPICE compatible compact model to evaluate parametric drift due to HCD for the full $V_G - V_D$ stress condition, including $V_G <, =$ and $> V_D$. If present, BTI [5], [6], SH [7] and HCD-BTI coupling [8] in the presence of SH can further complicate the modeling efforts.

Several features of experimental HCD kinetics published in the last ~40 years are reviewed in our recent reports (refer to the original references for details) [9], [10]. Notably, the peak HCD stress condition is shifted from $V_G \sim V_D/2$ to $V_D = V_D$ and the T activation of HCD is shifted from negative to positive as the technology is scaled from conventional or LDD based long channel MOSFETs to short channel MOSFETs, FinFETs and GAA-NS FETs. Although physical explanations are provided for the above HCD behavior changes from classical to modern era [11]–[14], in our opinion the issues are not well understood at this moment and hence need more work. HCD time kinetics show power-law dependence for conventional MOSFETs and modern FETs, while non-power-law and self-saturating trend is reported for LDD MOSFETs. However, the time kinetics of HCD shows universality across devices, stress conditions and measurement probes when scaled along the time axis in a log-log plot [15]. This universality is subsequently used to develop a SPICE compatible HCD compact model that is continuous in the full $V_G - V_D$ space and validated against measured data from different technologies and experimental conditions [16], [17].

Positive BTI (PBTI) in n-channel FETs became important with the advent of planar HKMG technology [5], [18], but it may [1], [3] or may not [2] be a concern in modern n-channel FETs. On the other hand, Negative BTI (NBTI) continues to remain as a major concern in modern p-channel

FETs [1]–[3], [19], [20]. SH effect becomes important due to higher thermal resistance of modern FETs [7], [21], which is known to impact HCD kinetics [22]. Moreover, SH can also aggravate BTI, and the net parametric shift for device level HCD test can become mix of BTI and pure HCD contributions [8]. The as-measured data do not show the typical time kinetics universality in such cases [23]. Technology-CAD (TCAD) is enabled to calculate the BTI contribution under non-zero V_D and SH [24], and to isolate the contribution due to pure HCD under device-level test [23]. Note that TCAD is indispensable in estimating BTI under HCD test condition, without triggering any HCD related effects. The isolation helps build separately calibrated BTI and HCD compact models and a coupled BTI-HCD framework, which has been validated using measured data under full $V_G - V_D$ space and wide range of T across different technologies [3], [23]–[25]. Once extracted, the pure HCD time kinetics is universal in the full $V_G - V_D$ space [23]. The coupled BTI-HCD compact model is used for cycle-by-cycle SPICE simulations of different gate type (inverter, NAND, NOR) RO and other complex circuits under real-life operation [26], [27].

This article presents a comprehensive review of past reports from our group on HCD universality [15], pure HCD compact model that is valid across full $V_G - V_D$ space [16], [17], adding BTI coupling related modifications to the pure HCD model to handle modern FETs including SH effect [23], [25], and cycle-by-cycle simulation of different gate based RO circuits in the presence of BTI and HCD [26].

The HCD universality is shown in Section II. The compact HCD model is briefly described in Section III, and validated using measured data in Section IV. The isolation of HCD and BTI contributions across different technologies is discussed in Section V. SPICE circuit simulation is discussed in Section VI. Finally, the paper is concluded in Section VII.

II. UNIVERSALITY OF HCD

The universality of HCD time kinetics is first proposed for scaling V_D dependent data at $V_G \sim V_D/2$ condition [28], and is now widely accepted [29]–[31]. In our recent report [15], it has been demonstrated across different probes (I_{DSAT}, I_{CP}, I_{DLIN}, V_T), device architectures and experimental conditions. The V_D dependence of the time-axis scaling factor is also shown to be similar across different published reports.

Fig. 1 (a) shows the time-scaled I_{DSAT} kinetics from different published sources: V_D variation at fixed V_G ($V_G < V_D$) and also at $V_G = V_D$, different T [31], V_G and V_D variations for off- and on-state modes [13], L_{CH} and V_D variations at $V_G = V_D$ [12], and multiple L_{CH} at DC and pulsed ($V_X \sim 0.6 * V_D$) conditions at fixed V_D [4] for planar MOSFETs. FinFET results at multiple T under DC and pulsed ($V_X \sim 0.8 * V_D$) conditions but at fixed V_D are also shown [1]. Remarkably, the time-axis scaled HCD time kinetics shows an "universal" shape (within measurement

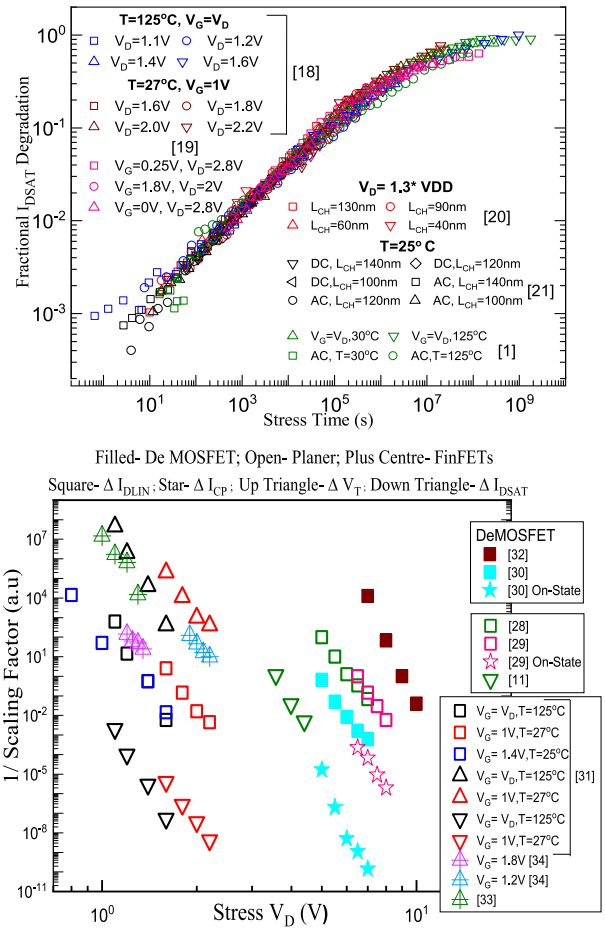

FIGURE 1. (a) Fractional I_{DSAT} degradation after time-axis scaling to universal time kinetics curve, and (b) time-axis scaling factor (1/S) versus stress V_D, for off- and different on- state HCD stress modes, for different measurement probes and different device technologies, from [15].

uncertainty), in spite of different experimental conditions and device technology.

The Voltage Acceleration Factor (VAF) associated with the inverse of the time-axis scaling factor (S) is plotted versus V_D in Fig. 1 (b), for the following sets of data:

a) I_{DLIN} from long L_{CH} planar MOSFETs at $V_G \sim V_D/2$ stress condition, high V_D (>3V) range [28], [29]
b) I_{CP} from long L_{CH} planar MOSFET at $V_G \sim V_D/2$ stress condition, high V_D range [29]
c) I_{DSAT} from moderately long L_{CH} planar MOSFET at $V_G = V_D$ stress condition, high V_D range [11]
d) I_{DLIN} and CP in DEMOSFETs under on and off-state stress, high V_D range [30]–[32]
e) V_T, I_{DLIN} and I_{DSAT} from short L_{CH} planar devices at fixed V_G ($V_G < V_D$) and $V_G = V_D$ stress conditions, low V_D (<3V) range [31]
f) V_T from short L_{CH} FinFETs stressed at different V_G to V_D ratio, low V_D range [33], [34].

Similar power-law VAF is obtained across different devices and probing methods in the on-state stress mode, observed for low to moderately high V_D range and various V_G to V_D ratios. It emphasizes the robustness of the

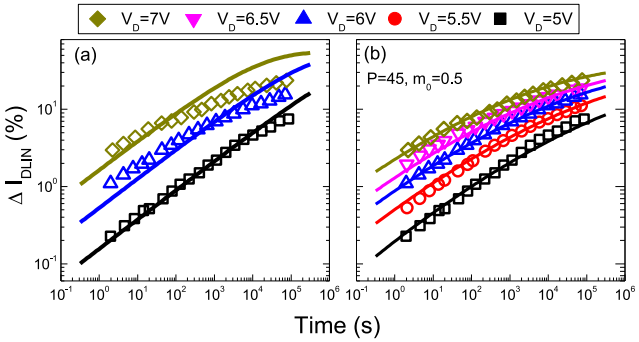

FIGURE 2. Modeling of measured ΔI_{DLIN} time kinetics at different V_D for on-state HCD stress (data from [28]) using standard and modified compact models, from [16].

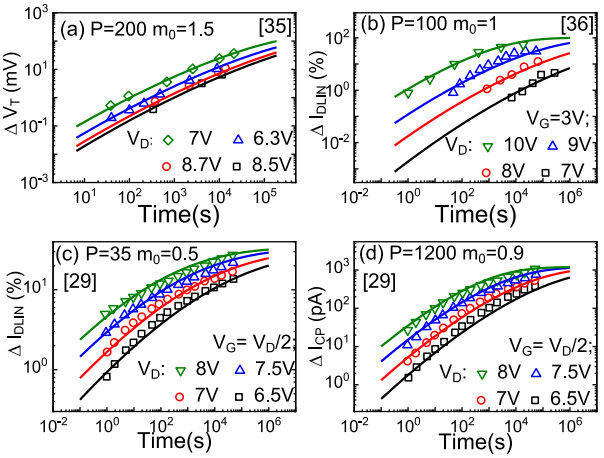

FIGURE 3. Modeling of measured (a) ΔV_T, (b, c) ΔI_{DLIN} and (d) ΔI_{CP} time kinetics from conventional [35], [36] and LDD [29] long L_{CH} MOSFETs for on-state HCD stress at different V_D, from [16].

unique underlying physical mechanism for on state HCD across technologies and stress V_D. The off-state mode shows a larger VAF than the on state. The HCD universality motivates a SPICE compatible compact model as discussed and validated hereinafter.

III. COMPACT HCD MODEL DESCRIPTION

HCD time kinetics has been modeled by the following self-saturating equation [34]:

$$\Delta P = P\left[1 - e^{\{-(\frac{t}{\tau})^m\}}\right] \quad (1)$$

where ΔP is the device parameter shift and P is the maximum value, t is stress time, t depends on stress conditions (V_G, V_D, substrate bias (V_B) and T) and also device dimensions (L_{CH} and oxide thickness, T_{OX}), and m governs the kinetics at early time before the onset of saturation. ΔP increases for lower τ and vice-versa.

Fig. 2 (a) compares the time evolution of I_{DLIN} degradation between data from [28] and model from Eq.1. Measured data are represented by symbols and model calculation by lines in all plots in this article. It is clearly evident that the model fails to match data across wide V_D range (it is possible to choose m to match either low or high V_D data). Similar results are also obtained for other datasets, but not shown here for brevity.

To improve model accuracy, Eq. (1) is modified using a time varying m as follows [16]:

$$m = m_0 e^{\left[-\left(\frac{t}{\tau_m}\right)^k\right]} \quad (2)$$

where m_0 is an adjustable parameter while both τ_m (1e5s) and k(0.036) are held fixed across all cases modeled in [16]. Fig. 2 (b) compares the time evolution of I_{DLIN} degradation between data from [28] and model from Eq.1 that is modified by Eq.2. It is now evident that the model works well across wide range of V_D and stress time. Hence, the modified model is used for all dataset shown in this work, using only two device specific parameters P and m_0. The details of τ modeling is discussed in our other publications [3], [16], [17], [23], [25] and hence kept out of this report. The model validation is shown in the next section [16], [17].

IV. HCD MODEL VALIDATION

Fig. 3 models the measured HCD time kinetics from various long L_{CH} devices and measurement probes, for high V_D stress: (a) ΔV_T [35] and (b) ΔI_{DLIN} [36] from conventional MOSFETs and (c) ΔI_{DLIN} and (d) ΔI_{CP} from LDD MOSFETs [29], for on-state stress.

The model can explain non- (or soft-) saturating power-law [35], [36] and self-saturating non-power-law [29] time kinetics across various reports.

Note that the devices in [35] have power-law time dependence for different T_{OX} and stress V_D (higher V_D is used for thicker T_{OX}), and a slight soft-saturation at higher time is seen at higher V_D in [36]. On the other hand, devices in [28]–[32], [36], [37] show non-power-law time kinetics with continuous saturation as the stress V_D is increased (fixed L_{CH} and T_{OX} for a given report). The P and m_0 values are device specific. Note that the drain junction profile impacts the DP shape and hence m_0, with higher $m_0$for abrupt junction [35], [36] and lower m_0 for gradual junction [28]–[32] devices. Due to different scanned spatial locations, the shape and m_0 are different between I_{DLIN} and CP probes even for the same device [29]. The model can also handle off-state stress, refer to [16] for details.

Fig. 4 models the measured HCD time kinetics from shorter L_{CH} planar devices probed using (a, b) V_T, (c, d) I_{DSAT} and (e, f) I_{DLIN} [31]. The time kinetics is power law and shows soft-saturation at long time. The V_D dependence at various V_G/V_D combinations is modeled at different L_{CH} and T. Identical m_0 is used for various measurement probes and stress conditions, while τ is varied (since it depends on V_G, V_D, T and L_{CH}) to model different stress conditions, refer to [16] for details.

Fig. 5 models the measured HCD time kinetics in (a, b) bulk and (c, d) SOI FinFETs, probed using (a) V_T at

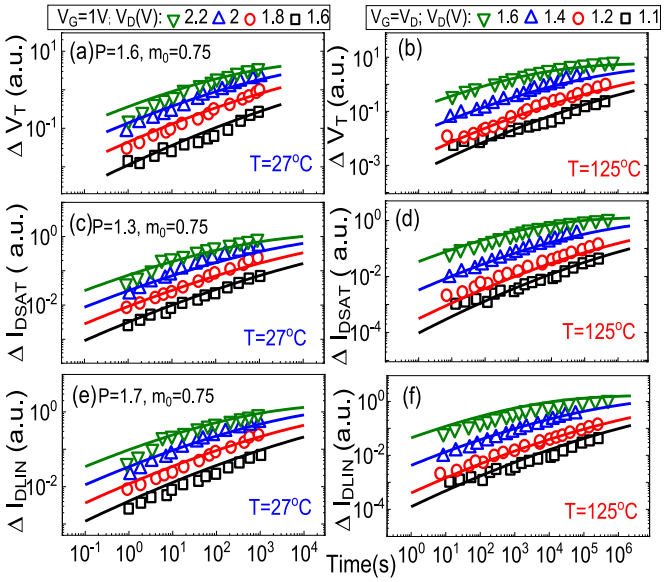

FIGURE 4. Modeling of measured (a, b) ΔV_T, (c, d) ΔI_{DSAT} and (e, f) ΔI_{DLIN} time kinetics at (a, c, e) room and (b, d, f) high T, for short L_{CH} MOSFETs for on-state HCD stress at different V_D, from [16].

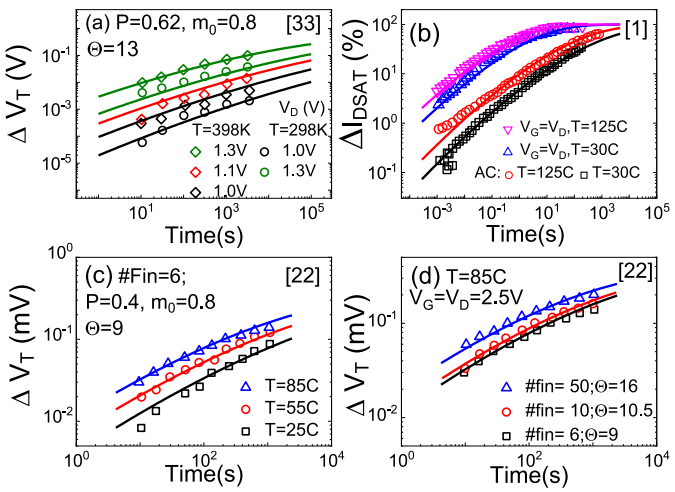

FIGURE 5. Modeling of measured FinFET time kinetics: (a) ΔV_T at various stress V_D and T [33], (b) DC and AC ΔI_{DSAT} at different T [1], and ΔV_T for different (c) fin count at fixed T and (d) T at fixed fin count [22].

different stress V_D and T [33], (b) I_{DSAT} at fixed V_D but different T under DC and AC stress [1], and V_T for (c) different fin number (at fixed T) and (d) different T (at fixed #fin) [22]. The power-law time dependence with (a, c, d) soft and (b) hard saturation at longer time can be modeled, refer to [16] for details.

Fig. 6 plots the measured and modeled lifetime, *i.e.*, the time to reach particular degradation, as a function of V_G for various stress (a) V_D and (b) T, using data from [11]. The bell-shaped V_G dependence of degradation ($\sim$1/lifetime) at $V_G \leq V_D$ and the monotonically increasing degradation at $V_G > V_D$ are modeled as V_D and T are varied. This device shows higher lifetime at higher T (classical HCD). Fig. 6

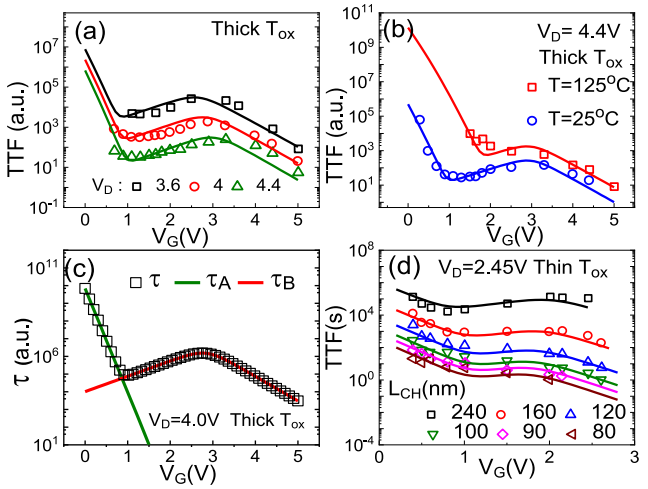

FIGURE 6. Modeling the V_G dependence of measured lifetime for different (a) V_D and (b) T, by using (c) contributions from different τ subcomponents. Similar exercise in (d) to model L_{CH} variation. Details of τ modeling and parameters are listed in [16].

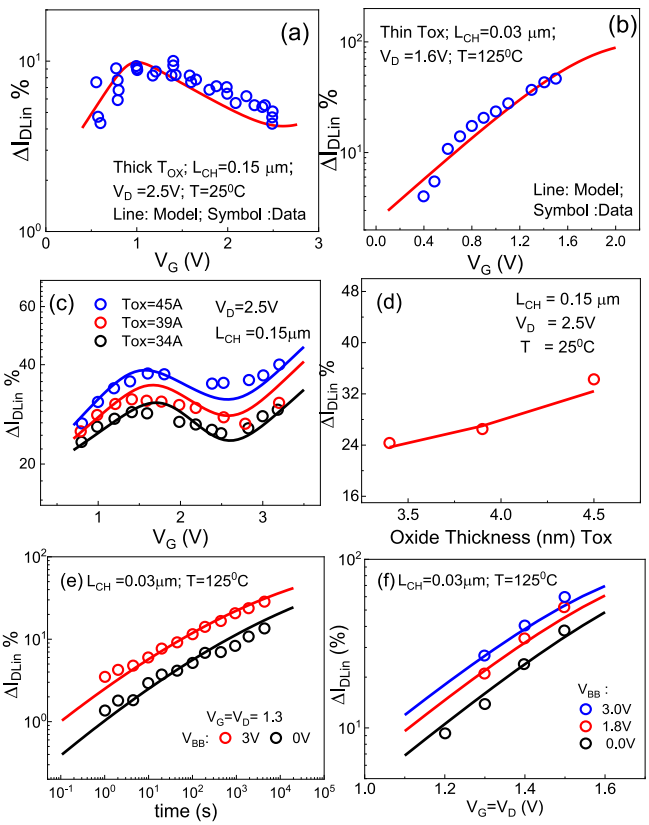

FIGURE 7. Modeling of measured $\%I_{DLIN}$ degradation in FDSOI devices (data from [38]–[40], modeling in [17]): Fixed time data versus V_G for (a) thick (b) thin oxide devices and (c) different Tox devices, and (d) at fixed V_G versus T_{OX}. Also shown the body bias effect on degradation: (e) time kinetics and (f) V_G dependence for $V_G = V_D$ case.

(c) plots the V_G dependence of t and its subcomponents (τ_A, τ_B and τ_C, see [16] for details) as a function of V_G. Fig. 4 (d) plots the measured and modeled lifetime versus V_G in

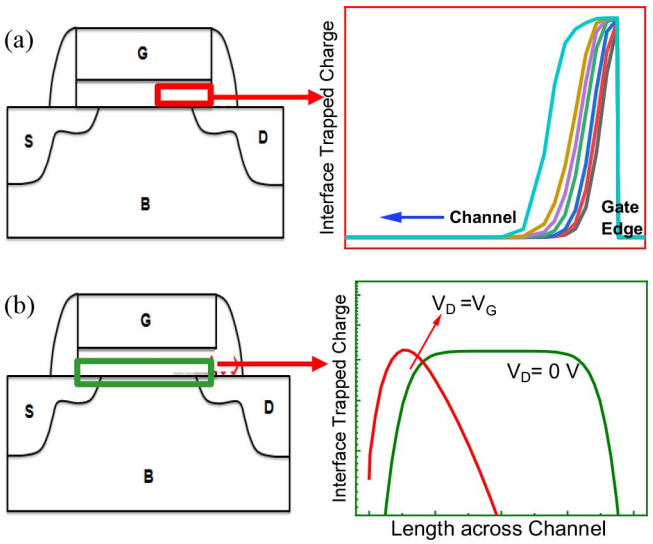

FIGURE 8. Schematic of a MOSFET with regions marked for trap generation under (a) HCD (different time) and (b) BTI (different V_D) stress. Refer to [24], [41] for details.

thinner T_{OX} devices having different L_{CH} [11]. The parameters governing t subcomponents are identical between the panels (a) and (d), except those related to the V_G dependence, as T_{OX} is different, refer to [16] for details. The model explains the transition from bell-shaped to monotonic V_G dependence of HCD (for $V_G \leq V_D$) as L_{CH} is scaled.

The model is also validated against FDSOI devices, data from [38]–[40]. Fig. 7 plots the measured and modeled fixed-time ΔI_{DLIN} for (a) thick (bell shaped) and (b) thin (monotonic) oxide devices as a function of V_G. Fig. 7 (c) and (d) plot the measured and modeled fixed-time ΔI_{DLIN} for different values of T_{OX}. Note that body biasing (V_{BB}) is often used in FDSOI devices for speed versus power tradeoff. Fig. 7 (e) plots the measured and modeled ΔI_{DLIN} time kinetics and Fig. 7 (f) plots the fixed time data versus VG at different V_{BB}. Refer to [17] for further details.

V. HCD AND BTI DECOUPLING

In this part, a step-by-step BTI-HCD decoupling procedure is demonstrated on ultra-fast measured ΔV_T kinetics in N and P channel planar MOSFETs [25] and GAA NSFETs [3] and P channel SiGe FinFET [23]. The complete BTI-HCD model is validated for $V_G < V_D$, $V_G = V_D$, and $V_G > V_D$ stress conditions at multiple V_D and T. Note that the relative contributions of BTI and pure HCD on overall ΔV_T during HCD stress would vary as the stress condition (V_G, V_D and T) is varied.

Fig. 8 illustrates the spatial trap generation profile along the channel in the presence of V_D for (a) HCD and (b) BTI [24], [41]. HCD is always localized near the drain end. The BTI is localized near the source end in the presence of V_D, as vertical electric field reduces near drain. SH effect is considered as it is important for confined channel devices.

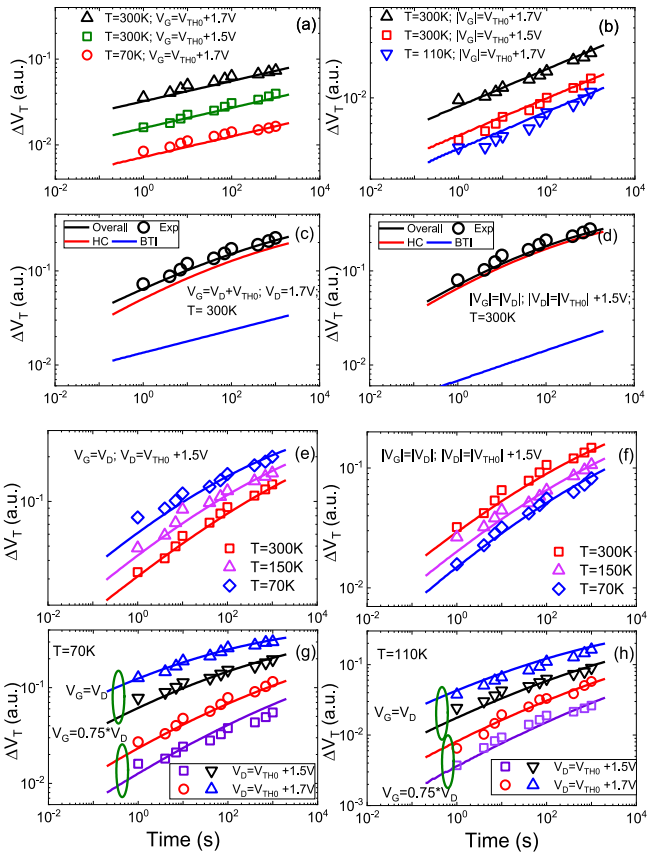

FIGURE 9. Modeling of measured ΔV_T time kinetics from planar devices (left panels N and right panels P FETs): (a, b) Pure BTI stress under multiple V_G and T, (c, d) HCD stress and underlying BTI and pure HCD subcomponents, and HCD stress at (e, f) fixed V_G, V_D but different T, and (g, h) different V_G, V_D but fixed T, from [25].

Fig. 9 models the measured ΔV_T time kinetics from N (left panels) and P (right panels) channel planar MOSFETs stressed under wide T (70K-300K) range. Fig. 9 (a, b) plots pure PBTI and NBTI for varying stress V_G and T. Fig. 9 (c, d) plots HCD and underlying BTI and pure HCD subcomponents for stress using fixed V_G, V_D and T (note that HCD is denoted as overall degradation with BTI and pure HCD contributions). Fig. 9 (e, f) plots HCD at fixed V_G, V_D but varying T. It is interesting to note the difference in T activation of HCD in N and P channel MOSFETs. For NMOS, the T activation is negative, while for PMOS, it is positive. However, for pure BTI, the T activation is positive for both devices. Thus, a careful decomposition of underlying contributions from different components is critical. Fig. 9 (g, h) plots HCD at multiple V_G/V_D ratios and varying V_D but low T. A detailed analysis is shown in [25].

Fig. 10 models the measured ΔV_T time kinetics from SiGe p-FinFETs (from a proprietary IBM process) [23], device details are listed in Table 1. Only five adjustable parameters are used to model measured data at various V_G/V_D stress conditions and fin length (FL). Left panels plot the underlying contributions from different subcomponents (electron/hole trapping and trap generation from pure

TABLE 1. Device details and description examined are listed.

Device Type	FF_A	FF_B	FF_C
Description	IL1; FL 20 nm #fin 12; Low N	IL2; FL 20 nm #fin 24; High N	IL2; FL 20 nm #fin 24; High N

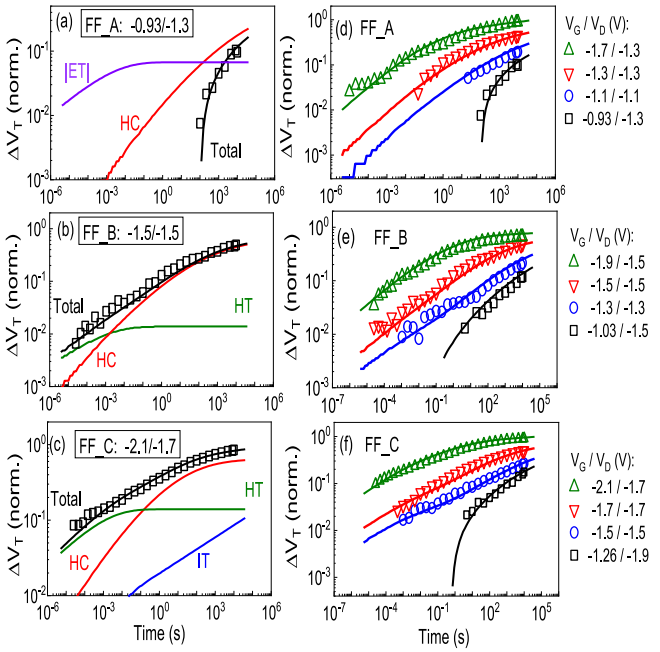

FIGURE 10. Modeling of measured ΔV_T time kinetics from SiGe p-FinFETs with different process and FL as listed in Table 1. Left panels show subcomponents and overall ΔV_T from different devices and stress conditions (V_G to V_D ratio). Right panel shows stress V_G and V_D variations in different devices, from [23].

BTI and pure HCD) and overall ΔV_T for fixed V_G and V_D stress (but different V_G to V_D ratios). Fig. 10 (a) plots FF_A data for $V_G < V_D$ case, it necessary to consider electron trapping in this case to model the steep slope at short time stress. Fig. 10 (b) plots FF_B data for $V_G = V_D$ case, hole trapping is present due to high N% in the gate stack. Fig. 10 (c) plots the FF_C data for $V_G > V_D$ case, contribution from BTI induced interface trap generation is seen due to high vertical fields. Right panels plot overall ΔV_T from different V_G and V_D stress for these devices. The detailed modeling of measured data and parameter list are discussed in [23].

Fig. 11 models the measured ΔV_T time kinetics from N (left panels) and P (right panels) channel stacked GAA-NS FETs (from a proprietary IBM process) [3]. Fig. 11 (a, b) plots pure PBTI and NBTI at different stress V_G and T. Note that the slopes of PBTI at long time is higher (n >0.16). This is due to generation of bulk traps in the oxide, see [6] for details. Fig. 11 (c) through (h) cover HCD stress under the entire $V_G - V_D$ span, (c, d) $V_G < V_D$, (e, f) $V_G = V_D$ and (g, h) $V_G > V_D$. Time evolution of the BTI and pure HCD sub-components are shown for the lowest dataset. Pure HCD

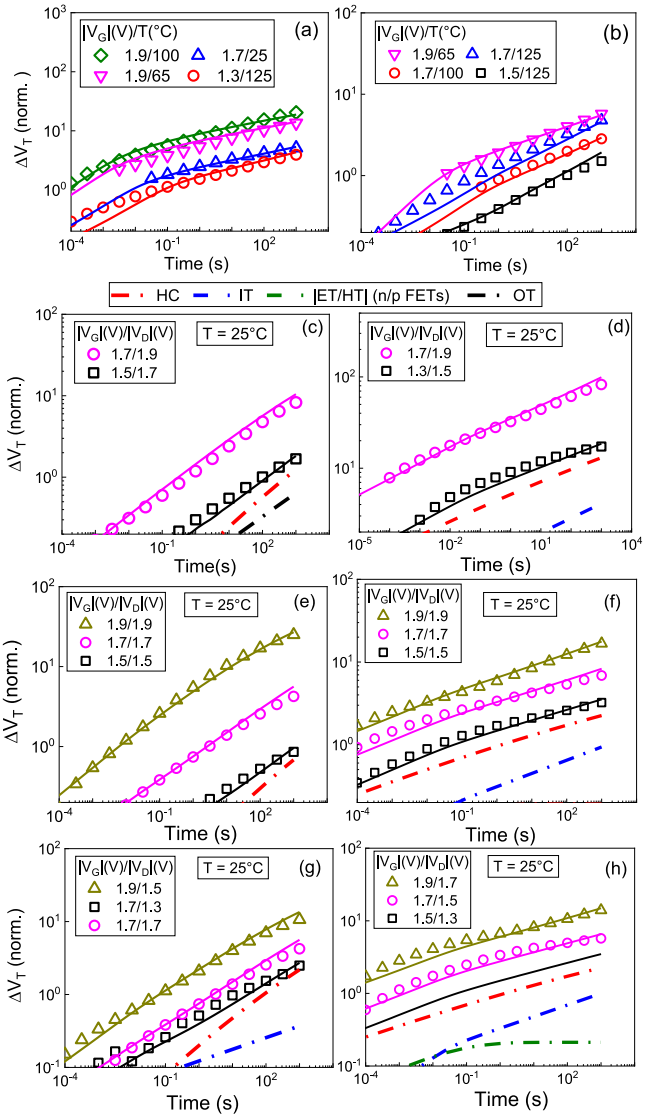

FIGURE 11. Modeling of measured ΔV_T time kinetics from GAA-NS devices (left panels N and right panels P FETs): (a-b) Pure BTI stress under multiple V_G and T, and (c-g) HCD stress at different V_D and different V_G to V_D ratios, as (c, d) $V_G < V_D$ (e, f) $V_G = V_D$ (g, h) $V_G > V_D$, from [3].

dominates in all cases, although BTI contribution becomes significant at $V_G > V_D$. Further details of data analysis and parameter values are discussed in [3].

Fig. 12 (a) demonstrates the time-axis scaling universality of the extracted pure HCD component in the entire $V_G - V_D$ space for SiGe p-FinFETs (from Fig. 10). Note that the as-measured data do not show this universality [23]. Fig. 12 (b-d) plot the V_D dependence of t for different V_G/V_D ratios for (b) P-SiGe FinFETs having different FL, and (c) N and (d) P GAA NS FETs. Interestingly, the V_D dependence of t is identical across different V_G/V_D ratios, and is seen for different devices.

VI. SPICE SIMULATION OF RO CIRCUITS

A cycle-by-cycle analysis is performed to capture the effect of BTI and HCD respectively during the on-off and transition

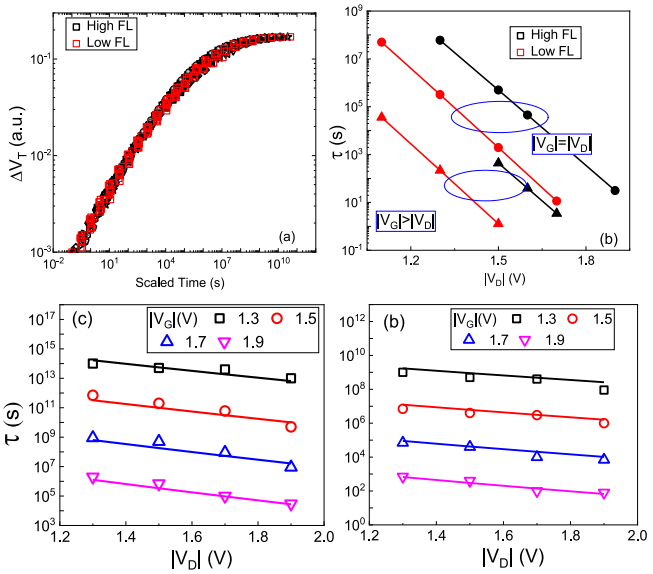

FIGURE 12. **(a) Time evolution of the extracted pure HCD component at different stress V_D and V_G/V_D conditions for P-SiGe FinFETs having different FL, note the time-axis is scaled to demonstrate universality. The V_D dependence of t (Eq.1, used to model pure HCD data) for (b) SiGe P-FinFET and (c) N and (d) P GAA NS-FET.**

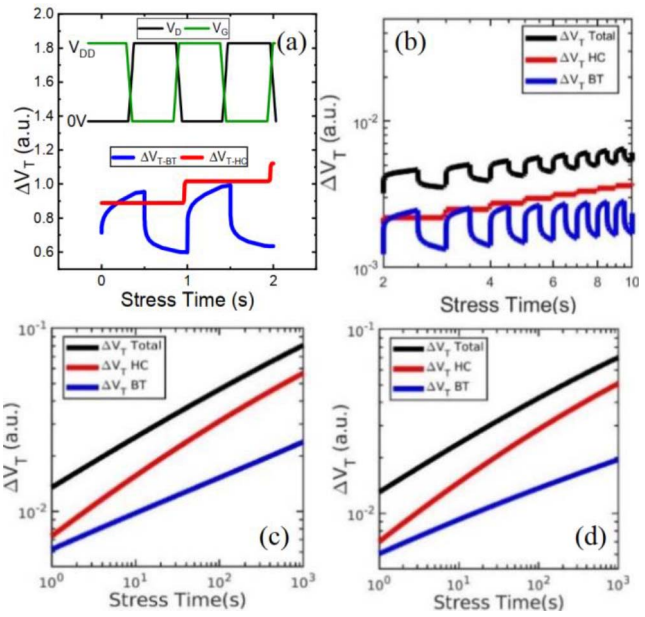

FIGURE 13. **Model simulated ΔV_{T-HC} and ΔV_{T-BT} for (a) two successive cycles and (b) many cycles over longer time, for low *f* inverter like AC pulse in P-SiGe FinFET. Calculated overall ΔV_T and underlying ΔV_{T-HC}, ΔV_{T-BT} (c) with and (d) without correlation between HCD and BTI, from [26].**

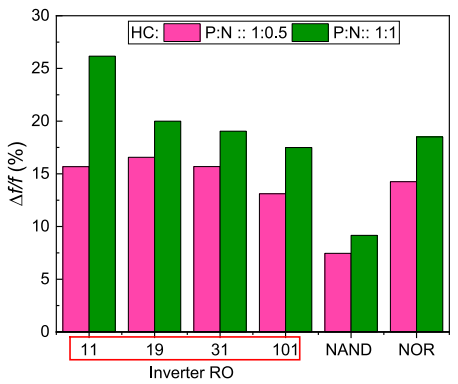

FIGURE 14. **Simulated RO *f* degradation (%) to study the impact of N FinFET HCD strength variation while keeping NBTI and HCD constant for P FinFET, from [26].**

phases of the AC waveform. Actual RO circuits clock in the ~GHz frequency range, and therefore the analysis is done for a small time (~100ns – 1ms) and extrapolated to end-of-life [26]. However, low frequency (*f*) simulations are shown purely for the purpose of demonstrating the cycle-by-cycle mixed BTI-HCD framework.

Fig. 13 plots the model simulated pure HCD (ΔV_{T-HC}) and BTI (ΔV_{T-BT}) contributions for (a) two successive cycles and (b) many cycles over longer time, under low *f* inverter like AC pulse in P-SiGe FinFETs with parameters calibrated with data from Fig. 10. Note, the time transformation concept is used for continuity across segments, and that of residue is used for the recovery of NBTI [26]. Note, the overall degradation is HCD dominated in this case (BTI is small in SiGe p-FinFET [23]).

Fig. 13 also shows the BTI-HCD coupling effect, where the calculated ΔV_{T-BT} (lower envelope after recovery), ΔV_{T-HC} and resultant ΔV_T (c) without and (d) with coupling is shown as a function of time. The inclusion of coupling results in reduction in the magnitude and time slope (n) of all quantities of interest (ΔV_{T-BT}, ΔV_{T-HC} and hence overall ΔV_T).

Fig. 14 plots the *f* degradation of different RO circuits from the cycle-by-cycle framework. Inverters with different stages (that vary the HCD to BTI contribution [1]), NAND and NOR based ROs are considered. Simulations are done with varying HCD strength in N-FinFET but keeping constant degradation parameters for P FinFET. The inverter-based ROs with lower # of stages are more prone to HCD, and show larger impact of the reduction in N-HCD component. However, this effect is less in inverter-based ROs with more # of stages, NAND and NOR, as they undergo relatively fewer on/off transitions and are BTI dominated. Note, the cycle-by-cycle simulation would be necessary to properly estimate the relative BTI and HCD contributions to overall degradation of different RO circuits, refer to [26] for further details.

Fig. 15 plots *f* degradation at different T for Static RO (only BTI) and Dynamic RO (BTI+HCD) stress using the calibrated data from Fig. 9. RO clock at 70K is higher and thereby more # of transitions are seen w.r.t 300K.

The overall RO degradation is lower at 70K in this particular case. This can be explained with the contribution of BTI and HCD T activations for both N and PFET. Due to positive T activation of BTI in PFET and NFET and HCD in PFET, the overall effect on *f* degradation is less at 70K in spite of higher HCD, see [25] for details.

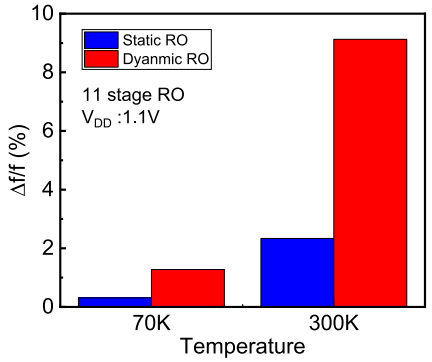

FIGURE 15. **Simulated *f* degradation (%) at 70K and 300K for Static and Dynamic RO based on device data of Fig. 9, from [25].**

The HCD compact model is used to simulate the ageing of SRAM array with Sense Amplifier and Write Driver (the BTI is modeled using a physics-based simulator [6]) under actual processor workloads, refer to [27] for further details.

VII. CONCLUSION

A compact model for HCD time kinetics is proposed, which works for conventional and LDD planar MOSFETs, DEMOS, FDSOI, FinFETs and GAA-NS FETs. The model is validated against measured data across extensive range VD, for off- and on-state stress at different VG/VD ratios, different T (including the SH effect if applicable), body bias, as well as variations in LCH and T_{OX}. Data from various probing techniques such as VT, IDLIN, IDSAT and I_{CP} have been modeled. The model is able to handle non-saturated (with different time slope n), soft- and hard-saturated time kinetics from various published reports. The model is used to decompose measured ΔV_T time kinetics during HCD stress at different V_G, V_D and T into pure HCD, BTI and electron/hole trapping subcomponents, if applicable. The universality of HCD time kinetics for different probes and stress conditions is shown across device architectures, for only HCD and mixed HCD-BTI (after decomposition) cases. Since the model is SPICE compatible and valid for the entire $V_G - V_D$ space, it has been used for cycle-by-cycle RO simulations, to properly estimate the relative contributions of HCD and BTI for different test cases.

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