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3D TCAD Analysis Enabling ESD Layout Design Optimization

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ABSTRACT On-chip electrostatic discharge (ESD) protection design for integrated circuits (ICs) is a challenging design-for-reliability problem. Since ESD events involve very high current transients in very short time period, current crowding is unavoidable, which leads to local overheating and creates local hot spots, resulting in ESD thermal failures. Therefore, layout design plays a critical role in practical ESD protection designs, which cannot be addressed by 2D TCAD ESD simulation. This article reports a comprehensive ESD simulation analysis by comparing true 3D TCAD with 2D TCAD, using exemplar diode ESD devices in a 55nm CMOS, which reveals 3D ESD discharging behaviors upon ESD layout variations. It concludes that true 3D TCAD ESD simulation is a powerful technique to enable ESD layout design optimization in real-world ESD protection designs.

INDEX TERMS 2D, 2.5D, 3D, TCAD, diode, ESD, HBM, layout.

I. INTRODUCTION

ESD protection is an essential part for all IC products due to the major reliability concerns associated with ESD failures [1], [2]. It has been widely understood that on-chip ESD protection is very challenging because ESD events involve complex coupling effects at process, device and circuit levels in electrical, thermal and time domains. Significant efforts have been devoted to ESD protection simulation using both ECAD and TCAD tools for ESD protection design optimization [3]–[9]. However, ESD protection design prediction remains a major IC reliability design challenge, especially at advanced IC technology nodes. Because ESD discharging involves substantial energy and is very fast, meanwhile IC substrates normally have poor thermal conductivity, transient local overheating becomes a signature for ICs under ESD stressing, which leads to hot spots within IC dies, resulting in ESD-induced thermal failures. Due to ununiform and inefficient thermal conduction under ESD stressing, ESD thermal failure is very sensitive to physical geometries of ESD protection device structures, where the edge/corner current and thermal crowding effects become a serious design concern. Consequently, ESD layout design becomes critical to success of practical ESD protection designs, which cannot be addressed by circuit or 2D TCAD simulation. Over years, advances in TCAD ESD simulation have greatly improved ESD design practices [3]–[7]. Unfortunately, widely used 2D and pseudo-3D (a.k.a., 2.5D) TCAD ESD simulation techniques are not useful in understanding ESD layout effects and achieving ESD layout optimization [3]–[7]. This article, an extension to our report at IEEE EDTM 2020 [10], reports a comprehensive study of using true 3D TCAD ESD protection simulation to thoroughly understand the ESD layout effects and, hence, to provide a practical 3D TCAD-based ESD layout design optimization method.

II. ESD DEVICES CREATION BY 2D, 2.5D & 3D TCAD

This section discusses the advantage of using true 3D TCAD for ESD simulation over using 2D and 2.5D TCAD simulation. As an example, p+/Nwell (PPNW) ESD diode structures are designed in a foundry 55nm CMOS technology. Real-world process recipes were used for accurate TCAD simulation to create the PPNW ESD diode structures, which was followed by TCAD simulation for human body model (HBM) ESD discharging in forward biasing mode. As a start, the focus of this article is on layout-related heat crowding and thermal failure effect under HBM ESD stressing by 3D TCAD ESD simulation and analysis, hence providing practical ESD layout design guidelines.

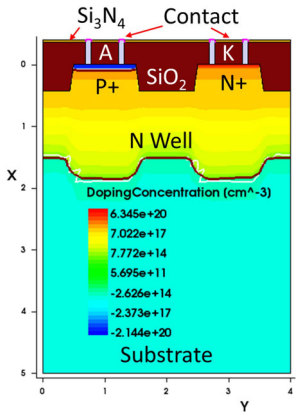

FIGURE 1. A 2D PPNW ESD diode structure created by 2D TCAD in 55nm CMOS.

Other 3D ESD complexities, such as transient voltage overshoot under charged device model (CDM) ESD zapping are not addressed [11], [12]. In TCAD process simulation to generate the PPNW ESD didoes, it follows the full actual process flow recipes of the commercial 55nm CMOS process flow from front-end to back-end including photoresistor mask generation, shallow trench isolation (STI) etching, deposition, chemical-mechanical polishing (CMP), Nwell and active region implantation and annealing, SiO_2 and Si_3N_4 isolation, and metal contacts, etc. Synopsys Sentarus Process TCAD tool was used to create the PPNW ESD didoes in three different simulation methods. First, 2D TCAD process simulation was used to create a 2D PPNW diode structure as shown in Fig. 1. Second, pseudo-3D (2.5D) TCAD simulation was conducted to create a pseudo-3D PPNW ESD diode device as depicted in Fig. 2. 2.5D TCAD simulation basically extends a cross-sectional ESD device in Fig. 1 in the 3rd dimension (Z-direction) to create a 3D-look ESD diode, having everything uniform in the 3rd dimension, hence named pseudo-3D simulation because a real-world 3D ESD device can never be uniform in any dimension (doping, etc.). Pseudo-3D process simulation has been widely used to balance simulation accuracy and TCAD run time, which can be significant. Third, true 3D TCAD simulation was performed to create the real-world 3D ESD diodes, as fabricated in a foundry, shown in Fig. 3. The 3D ESD diode structure has three dimensions: X-dimension represents the device depth (H), defining vertical details including the Si substrate thickness. Y-dimension defines the length (L) of the ESD diode structure. Z-dimension defines the width (W) of the ESD diode structure. The 3D ESD diode in Fig. 3 shows all structural and compositional details of the PPNW structure including the substrate, Nwell, P+ and N+ diffusions, PN junction, SiO_2, Si_3N_4, STI and metal contacts (tungsten plugs). The exemplar PPNW ESD structure has physical dimensions of L = 4μm (device Length), W = 11μm (device Width) and H = 5μm (device Depth, truncated). The 2D/2.5D/3D ESD diodes have the same dimensions for a fair TCAD comparison. The 3D ESD PPNW structure features 12 evenly placed contact holes filled with tungsten

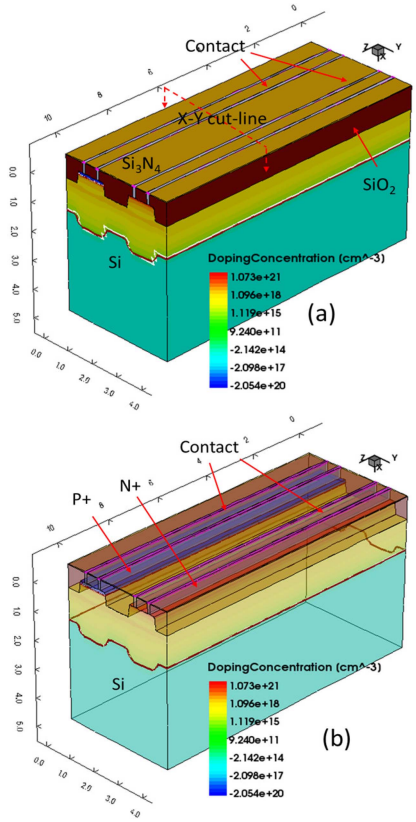

FIGURE 2. A pseudo-3D PPNW ESD diode structure created by 2.5D TCAD simulation: (a) a 3D view, and (b) a 3D transparent view.

plugs in the layout, 6 for the P+ electrode and 6 for the N+ electrode, designed in two lines in a uniform way. Transient TCAD ESD discharging simulation was then conducted for the three ESD PPNW structures using standard HBM ESD pulse waveforms as incoming ESD stimuli, and the ESD discharging performance was compared among the 2D, 2.5D and 3D ESD diodes.

III. 3D VS. 2D/2.5D TCAD ESD SIMULATION

Because ESD protection is very sensitive to device geometries (layout) and transient ESD discharging generates local hot spots that will lead to internal ESD thermal failures, it is obvious that true 3D TCAD ESD simulation should be more accurate than 2D/2.5D TCAD simulation. On the other hand, it is well known that the device mesh grid generated for an ESD structure can substantially affect TCAD ESD simulation results, mainly due to the complex electro-thermal-process-device-circuit-layout coupling effects of an ESD protection structure. However, too "fine" a device mesh grid may require unbearable TCAD run time while improving simulation accuracy. Hence, a good balance must be made between TCAD simulation time and accuracy. Transient HBM ESD simulation by TCAD was first conducted to understand the ESD performance impact of device mesh generation using three splits: Fine mesh, Finer mesh and Finest mesh. The mesh grid is non-uniform for a device. The

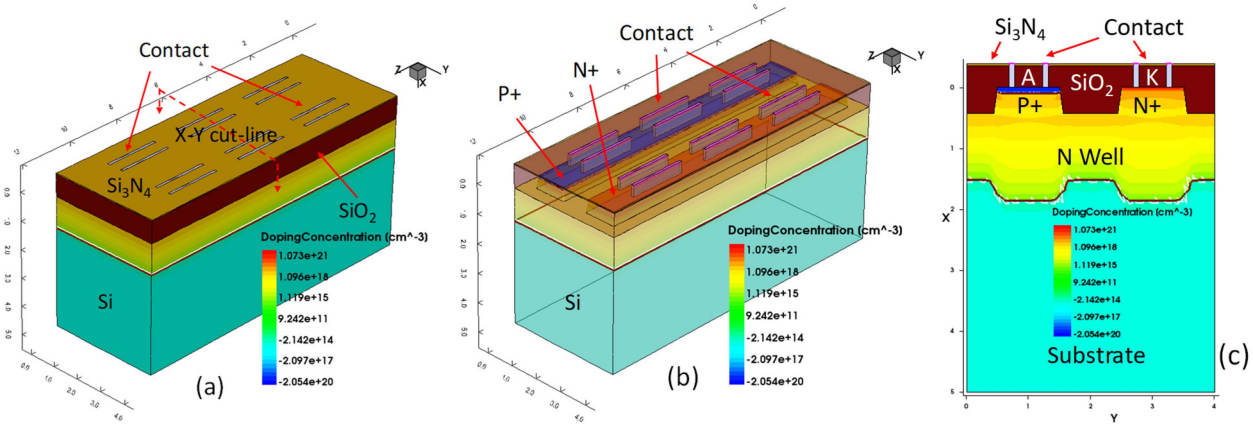

FIGURE 3. A real-world 3D ESD PPNW diode generated by true 3D TCAD process simulation contains 12 evenly placed contact plugs for two diode terminals (P+/N+): (a) 3D ESD diode view, (b) 3D ESD diode in transparent view, (c) X-Y cross-section view (equivalent to Fig. 1).

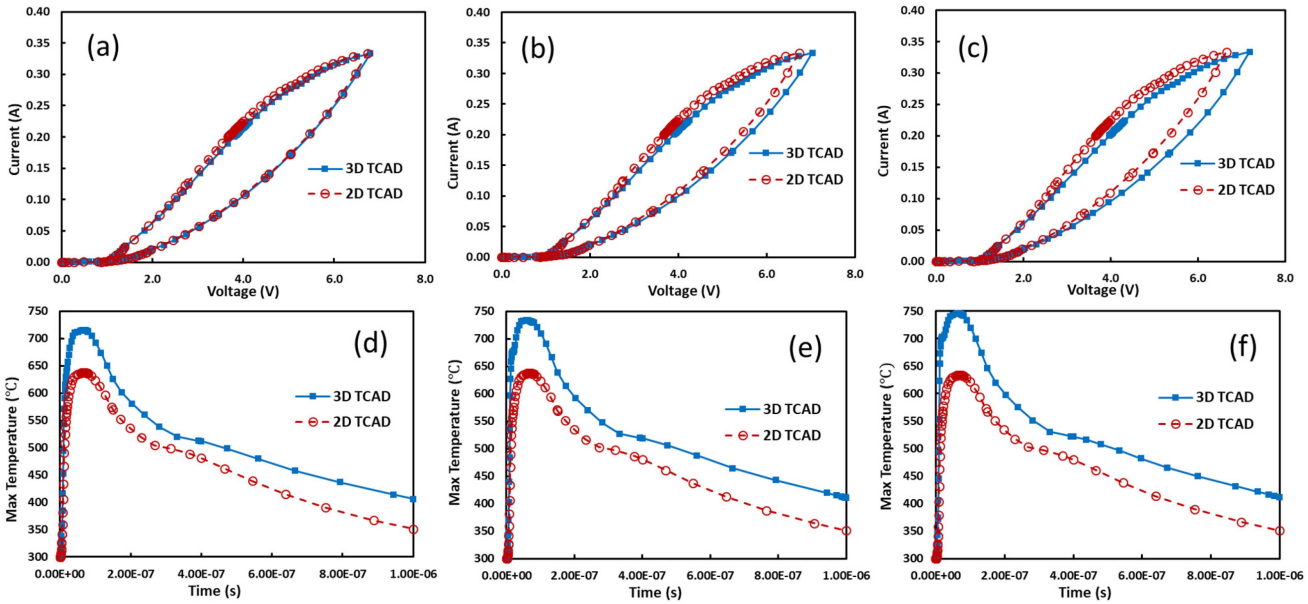

FIGURE 4. Transient ESD discharging I-V-T-t curve comparison by 500V HBM ESD simulation for the 2D and 3D ESD diodes with varying mesh densities shows dependence of ESD behaviors on the TCAD mesh grids: (a) I-V curves for Fine mesh, (b) I-V curves for Finer mesh, and (c) I-V curves for Finest mesh; (d) $T_{MAX} - t$ curves for Fine mesh, (e) $T_{MAX} - t$ curves for Finer mesh, and (f) $T_{MAX} - t$ curves for Finest mesh.

global mesh is sparse with direction-dependent maximum edge length (maxcoarse) of 1.0μm and direction-dependent minimum edge length (mincoarse) of 0.5μm. Smaller mesh sizes were defined by maxfine and minfine parameters using the same refinement method for P+ and N+ regions: maxfine = 0.2μm, 0.2μm & 0.1μm, and minfine = 0.1μm, 0.05μm & 0.02μm, respectively, for the fine, finer, finest meshes. The mesh grid at silicon-oxide interface was set with a minimum size (minnormsize) and a growth rate (mingrowth): mininomsize = 0.05μm, 0.02μm & 0.01μm, and mingrowth = 2, respectively, for finer, finer, finest meshes. 2D and 3D TCAD ESD simulations under HBM 500V stressing were compared for the same ESD PPNW structure to evaluate their sensitivity to mesh density. The thermal boundary conditions, specified in TCAD "Thermode", are adiabatic except for the electrodes set as 300K with surface resistance of 5e-7Ω. Fig. 4 depicts the transient ESD discharging I-V-T-t behaviors for the three ESD device splits, including ESD discharging I-V curves and the maximum lattice temperature in time domain ($T_{MAX} - t$) under same level of HBM ESD stressing by both 2D and 3D TCAD ESD simulation. In general, a higher mesh density will improve TCAD simulation accuracy. Fig. 4a/b/c readily shows that, at lower mesh density, 2D TCAD ESD simulation offers almost same level of ESD I-V accuracy as that by 3D TCAD ESD simulation. Therefore, a density mesh is not necessary for 2D TCAD ESD simulation. As the device mesh density increases, the difference in ESD I-V behaviors between 2D and 3D TCAD ESD simulation becomes obvious, and 3D TCAD ESD simulation is clearly more accurate. However, improvement in

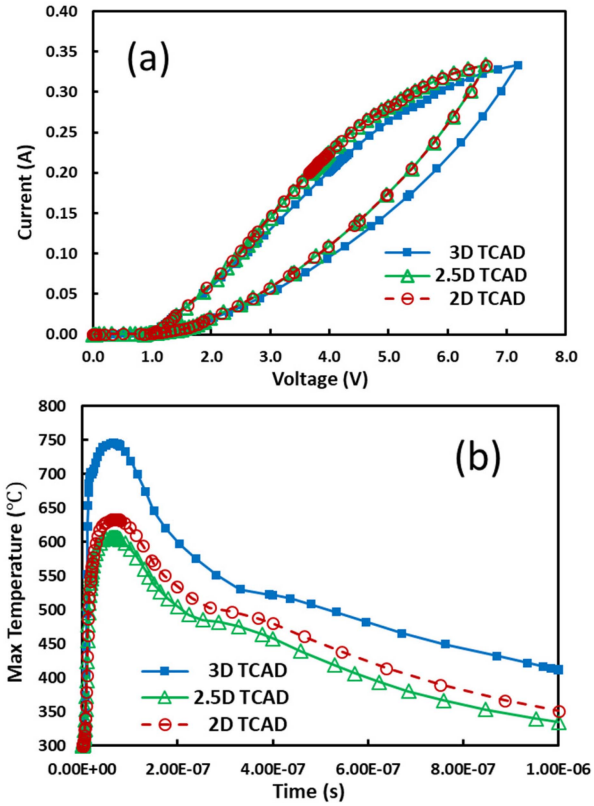

FIGURE 5. Transient ESD I-V-T-t comparison for PPNW ESD diode between 2D, 2.5D and 3D TCAD simulation: (a) ESD discharging I-V curves, and (b) ESD T_{MAX} – t curves.

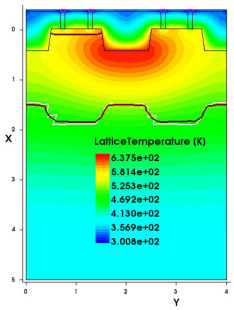

FIGURE 6. Temperature map for the ESD diode by 2D TCAD: X-Y cross-section view. (hot spots revealed by color codes).

ESD I-V accuracy of 3D TCAD over 2D TCAD seems to gradually saturate as the device mesh density continues to increase. Similarly, Fig. 4d/e/f clearly shows substantial improvement in simulation accuracy in ESD $T_{MAX} - t$ characteristics from 2D TCAD to 3D TCAD, and again, the accuracy improvement tends to saturate as the mesh density reaches to certain level. This comparison clearly states that an optimum (threshold) device mesh density should be identified in 3D TCAD ESD simulation to achieve highest simulation accuracy without suffering from an unbearable increase in TCAD ESD simulation time, a critical factor in using 3D TCAD for practical ESD protection designs. On the other hand, improved ESD simulation accuracy of 3D TCAD over 2D TCAD is attributed to the fact that true 3D TCAD simulation can address the ESD geometric effects (e.g., edges and corners of devices, diffusion regions and isolations, as well as contact layout features, etc.). The transient and nonuniformity nature of ESD discharging makes local current/thermal crowding and hot spots unavoidable in ESD devices under ESD stressing, which simply cannot be meaningfully addressed by 2D/2.5D TCAD ESD simulation because of its uniformity nature. The observed T_{MAX} difference in the same PPNW ESD structure simulated by 3D TCAD is at least ~ 100°C higher than that from 2D TCAD, attributed to local overheating in hot spots. Typically, in TCAD ESD simulation, ESD thermal failure criterion is set to the Si melting temperature of ~ 1688°C and the corresponding maximum thermal breakdown current (I_{t2}) reflects the HBM ESD protection capability. Further, Fig. 5 compares ESD discharging I-V-T-t characteristics for the same PPNW ESD diode by 2D, 2.5D and 3D TCAD ESD simulation. Between 2D and 2.5D TCAD simulation, the transient ESD discharging I-V behaviors shows no difference due to the same uniformity in the 3rd dimension (i.e., Z-dimension). For transient $T_{MAX} - t$, 2.5D TCAD gives slightly lower T_{MAX} than that by 2D TCAD, which is possibly because 2.5D TCAD uses a required "real" size ESD device (i.e., W-size in Z-axis, though uniform in Z-dimension) while 2D TCAD uses a tiny unit-sized ESD device, hence slightly more edge/corner effect weight is expected for each default 2D unit under ESD stressing, meaning little more local overheating. On the other hand, it is readily observed that the ESD I-V curve for 3D TCAD is substantially different from that by 2D/2.5D TCAD, and the larger ESD discharging resistance (R_{ON}) is apparently attributed to local ESD discharge crowding effect associated with the true ununiform (Z-direction) 3D ESD device, consequently, much higher $T_{MAX} \approx 745$°C is observed for 3D TCAD than $T_{MAX} \approx 630$°C in 2D TCAD simulation. The transient thermal behaviors can be further examined by the temperature maps shown in Figs. 6, 7 & 8, which clearly depict the varying device geometrical impacts on ESD discharging thermal distribution per 2D, 2.5D & 3D TCAD ESD simulation. Specifically, the lateral cross-section views (X-Y plane) in Fig. 6, Fig. 7b and Fig. 8b show similar T-map from 2D, 2.5D and 3D TCAD simulation. However, the X-Z cross-section views in Fig. 7d and Fig. 8d clearly depict the sharp difference in ESD discharging thermal distribution along Z-dimension between 3D TCAD and 2.5D TCAD simulation where 2.5D misleadingly shows a uniform current/thermal distribution due to the uniform extension of the ESD device in Z-dimension, while 3D TCAD accurately reveals the ununiform ESD thermal distribution in Z-direction, reflecting the 3D ESD edge/corner effect. Of course, 2D TCAD cannot reveal Z-direction behavior at all. The top views in Fig. 7a/c and Fig. 8a/c again confirm the fundamental difference between 2.5D and 3D TCAD simulation where true 3D TCAD accurately depicts the significant ESD geometrical impact (i.e., layout effect), while 2.5D TCAD only shows uniform thermal distribution

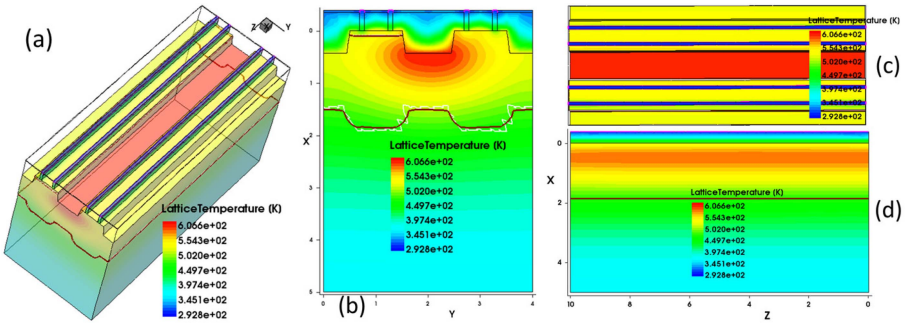

FIGURE 7. **Temperature map for the ESD diode by 2.5D TCAD: (a) pseudo-3D transparent view, (b) X-Y cross-section view, (c) top view (Y-Z cross-section), and (d) X-Z cross-section view. (hot spots revealed by color codes).**

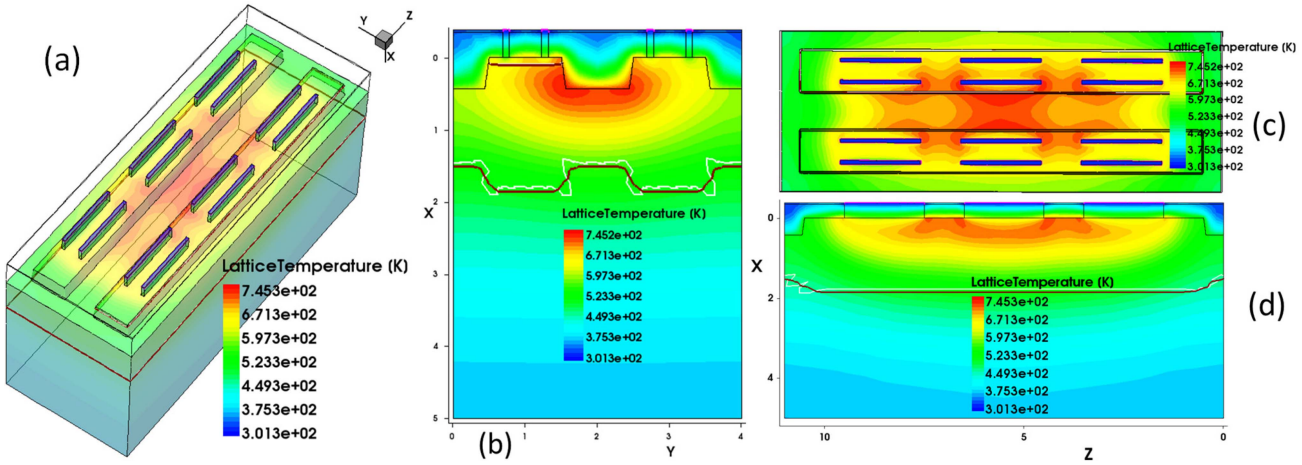

FIGURE 8. **Temperature map by 3D TCAD: (a) 3D transparent view, (b) top view (Y-Z cross-section), (c) X-Z cross-section view, and (d) X-Y cross-section view. (hot spots revealed by color codes).**

in Z-direction. From Fig. 8, 3D TCAD ESD simulation also suggests that central ESD heat crowding occurs due to the common uniform contact layout practices, which will be further discussed in the next section for ESD layout design optimization.

IV. ESD LAYOUT DESIGN OPTIMIZATION BY 3D TCAD

Since ESD discharging performance is highly sensitive to the physical payout of ESD structures, we developed a new 3D TCAD based practical ESD layout design optimization technique, which is depicted using four different ESD layout splits for the same PPNW ESD diode structure in 55nm CMOS. These ESD diode splits have the same structures created by 3D TCAD process simulation, except that the contact layout patterns are designed differently to reflect the 3D ESD discharging current routing effects: Split-1 (Base-4x3) is a reference device with "normal" top contact plug layout as shown in Fig. 9a and Fig. 10a, which has 2 parallel contact lines for P+ and N+ terminals, respectively, each line has 3 contact holes filled with tungsten plugs. All contact plugs are laid evenly in Split-1. Split-2 (Edge-4x1) is same as Split-1 except that only the contact plugs at the edge of the ESD structure (one end in Z-direction) are electrically connected, hence there are only 2 contacts in P+ and

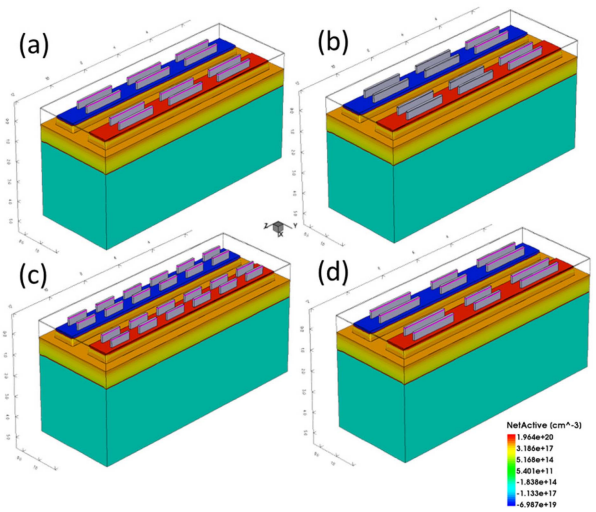

FIGURE 9. **Four 3D ESD diode splits with varying contact layout designs by 3D TCAD ESD simulation: (a) Split-1: Base-4x3, (b) Edge-4x1, (c) Even-4x6, and (d) Uneven-4x3. The tungsten plug marked by a pink bar on top is electrical-connected to route ESD discharge current.**

N+ diffusions to conduct ESD current, as shown in Fig. 9b and Fig. 10b. Compared to Split-1, the contact layout in Split-2 means to show the ESD edge crowding effect. Split-3

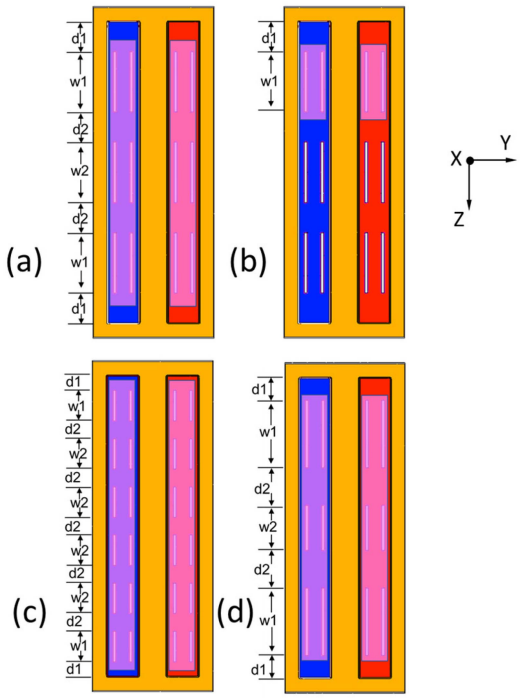

FIGURE 10. **Top views for the four 3D ESD diode splits in Fig. 9 with varying dimensions: (a) Split-1: Base-4x3, (b) Edge-4x1, (c) Even-4x6, and (d) Uneven-4x3. The contacts marked by pink layers are actual electrodes that are electrical-connected to conduct ESD currents, hence determines the actual ESD discharging routes on a chip.**

TABLE 1. **Key dimensions for the four layout splits.**

Splits	*w1 (μm)*	*w2 (μm)*	*d1 (μm)*	*d2 (μm)*
Split-1 Base-4x3	2	2	1	1
Split-2 Edge-4x1	2	-	1	-
Split-3 Even-6x4	1	1	0.5	0.6
Split-4 Uneven-4x3	2.25	1.5	0.75	1.25

(Even-4x6) is similar to Split-1, however, has 6 smaller tungsten plugs in each contact line, but still evenly distributed, as shown in Fig. 9c and Fig. 10c. Split-4 (Uneven-4x3) is similar to Split-1, however, the center contacts are smaller than that in Split-1, hence an uneven contact layout design showing less effective central contact area for ESD discharging, as depicted in Fig. 9d and Fig. 10d. Table 1 summaries the key contact layout dimensions including different contact length sizes (w1 & w2 in Z-direction), contact spacing (d2 in Z-direction) and spacing from the edge of a diode contact to the end of diffusion regions (d1 in Z-direction). The contact layout size variations are designed to reflect the ununiform ESD discharging current and thermal distribution, leading to ESD weak points in ESD structures due to layout effect.

3D TCAD ESD simulation using HBM ESD pulse stimuli of same strength was conducted for the four layout

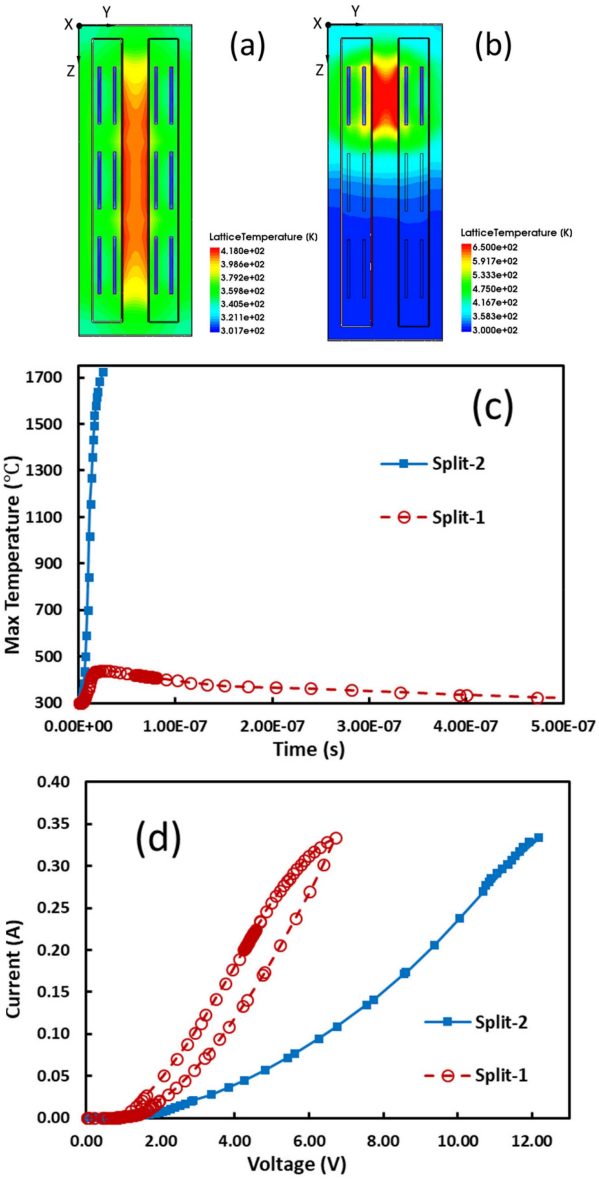

FIGURE 11. **Comparison of transient ESD I-V-T-t characteristics for Split-1 and Split-2 devices under 500V HBM ESD zapping by 3D TCAD ESD simulation. (a) Top view for thermal map of Split-1, (b) Top view for thermal map of Split-2, (c) T_{MAX} – t curves, and (d) ESD I-V curves. (hot spots revealed by color codes).**

splits. Fig. 11 compares the transient ESD I-V-T-t behaviors for Split-1 and Split-2 devices, mainly to study the edge effect in Split-2, which has to route the large ESD discharging current within the ESD diode structure to one end of the structure with only 2 tungsten plugs for P+ and N+. Fig. 11a depicts the top view of temperature maps, which clearly shows that severe ESD current crowding occurs at one edge of the ESD structure for Split-2, leading to local overheating that will definitely cause early ESD failure at the device edge. It is also observed that Split-1 shows higher ESD discharging current density in the center area even though the contacts are evenly placed along the Z-dimension. As shown in Fig. 11b, while Split-1 maintains fairly low

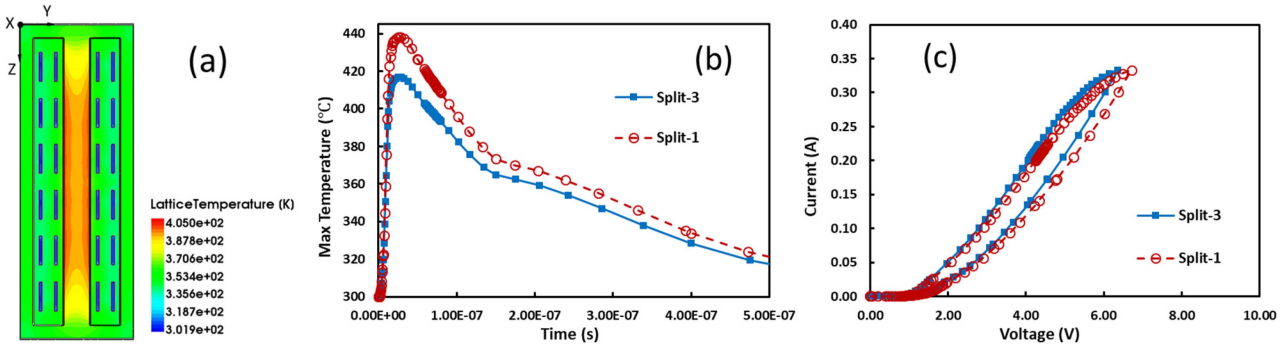

FIGURE 12. Transient ESD discharging behaviors for Split-3 devices under 500V HBM ESD zapping by 3D TCAD simulation: (a) top view (Y-Z cross-section) of temperature map for Split-3 structure, (b) transient $T_{MAX} - t$ curve comparison for Split-1 and Split-3, and (c) transient ESD discharging I-V curve comparison for Split-1 and Split-3. (hot spots revealed by color codes).

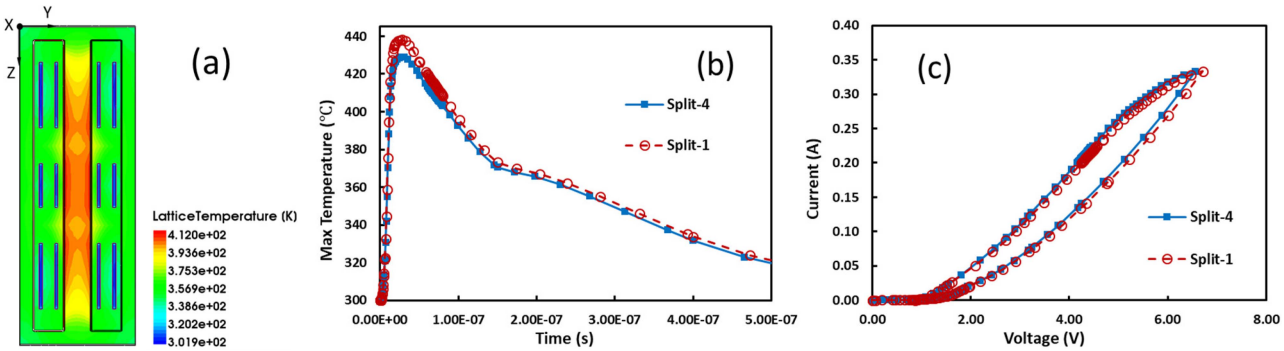

FIGURE 13. Transient ESD discharging behaviors for Split-4 devices under 500V HBM ESD zapping by 3D TCAD simulation: (a) top view (Y-Z cross-section) of temperature map for Split-3 structure, (b) transient $T_{MAX} - t$ curve comparison for Split-4 and Split-1, and (c) transient ESD discharging I-V curve comparison for Split-4 and Split-1. (hot spots revealed by color codes).

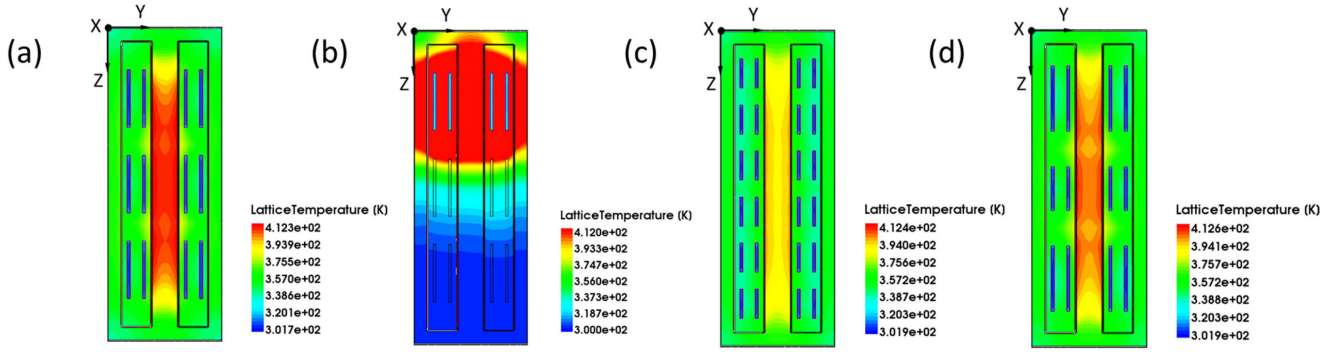

FIGURE 14. Top view temperature maps for all four splits shown in the same temperature scale (from 300°C to 412°C) provide an easy comparison view: (a) Split-1, (b) Split-2, (c) Split-3, and (d) Split-4. (hot spots revealed by color codes).

temperature (peaks $\sim$ 420°C) during the HBM zapping, while Split-2 shows a sharp spike in temperature ($>$ 1688°C) due to local overheating at the edge, quickly leading to ESD thermal failure. Fig. 11c presents the transient ESD discharging I-V curves for Split-1 and Split-2, which show a much higher ESD discharging R_{ON} for Split-2 due to overheating at the edge. Obviously, ESD designers should avoid the ESD edge effect due to poor contact layout design practices.

Fig. 12 compares Split-3 with Split-1. In Split3, 12 more contacts for P+ and N+ were added, and each contact size reduced to half area of Split-1 (i.e., the total areas for Split-3 and Split-1 remains the same). Due to more contacts evenly distributed across the ESD device (in Z-dimension), Split-3 is much more efficient in discharging large HBM ESD pulse, even though each contact size in Split-3 is smaller than in Split-1. Fig. 12a shows a fairly even and low temperature distribution for Split-3. Figs. 12b&c show a lower R_{ON} and hence lower T_{MAX} for Split-3 ($\sim$ 415°C) compared to Split-1 ($\sim$ 440°C). It again shows the layout impact on ESD protection performance.

Fig. 13 depicts the transient ESD discharging I-V-T-t behaviors for Split-4, which features a relative smaller

contact plugs in the center area in order to alleviate the central overheating observed in Split-1 (Fig. 11a). Fig. 13 a&b clearly shows the improvement in ESD discharging of Split-4 over Split-1 in both T-map and T_{MAX}. Though ESD discharging R_{ON} for Split-4 and Split-1 are similar (Fig. 13c), however, the relatively relaxed center overheating due to the uneven central contact layout leads to lower T_{MAX} in Split-4 compared to Split-1 (Fig. 13b). While the temperature maps in Figs. 11/12/13 use separate temperature scales for a better individual view to clearly show the varying thermal distribution along Z-direction determined by individual ESD contact layout, Fig. 14 presents the top view temperature maps for the four splits in the same temperate scale, which offers an easy comparison picture of ESD layout impacts on ESD discharging behaviors. In general, this comprehensive ESD layout analysis by 3D TCAD simulation readily reveals that ESD layout strategy is extremely critical in ESD protection designs and poor ESD layout will lead to severe edge/corner crowding effect, hence local overheating that results in ESD weak points and poor ESD robustness. True 3D TCAD ESD simulation is a powerful tool to understand real-world 3D ESD discharging behaviors, hence provides useful ESD design insights to achieve ESD protection design optimization, as well as to offer practical ESD layout design guidelines.

V. CONCLUSION

On-chip ESD protection design becomes extremely challenging for advanced IC technologies at sub-28nm nodes. ESD protection is extremely sensitive to ESD layout designs due to unavoidable edge/corner effects under ultrafast and heavy ESD stressing. Using ESD design examples in 55nm CMOS, this article presents a new true 3D TCAD ESD simulation method to understand 3D ESD layout design impacts on ESD protection performance. The study proves that careful 3D TCAD ESD simulation can accurately address the 3D ESD geometrical effects and hence provide useful layout design guidelines to achieve ESD design optimization and prediction.

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