Received 11 June 2020; revised 1 August 2020 and 16 September 2020; accepted 21 September 2020. Date of publication 28 September 2020; date of current version 9 October 2020. The review of this article was arranged by Editor M. Mouis.

Digital Object Identifier 10.1109/JEDS.2020.3026993

Electrical Characteristics of LDD and LDD-Free FinFET Devices of Dimension Compatible With 14 nm Technology Node

YUCHEN DU, MD KHALED HASSAN, RI-AN ZHAO, XINGGONG WAN, AND MANOJ JOSHI

GLOBALFOUNDRIES, Malta, NY 12020, USA

CORRESPONDING AUTHOR: Y. DU (e-mail: yuchen.du@globalfoundries.com)

ABSTRACT FinFET devices with and without LDD implantation has been studied for dimensions compatible with leading 14nm technology node. Devices without LDD have better electrostatic characteristics with SS = 65mV/dec and DIBL = 33mV. The nFET transistors with no LDD have device Vtsat mismatch reduction by 20%, together with retained device reliability of HCI as compared to devices with LDD. A full range of device Vtsat flavors is enabled in this experiment, presenting excellent device performances at different operating voltages of 0.55V, 0.8V and 1.2V. All results indicates that devices with no LDD and one less mask in FinFET architecture achieve lower cost, compelling performance and area scaling compared to devices with LDD, for high performance and low power applications.

INDEX TERMS FinFET, 14nm, LDD, Vtsat mismatch, SS, DIBL.

I. INTRODUCTION

FinFET transistors with outstanding electrical transport behavior in 14nm CMOS technology have been successfully demonstrated in high-volume production for low power and high performance applications [1]–[4]. High drive current combined with low power consumption, as well as simplified fabrication process with minimized impact on intrinsic silicon electrical properties have become mainstream in today's semiconductor industry. The feasibility of extending transistors with superior device performance, together with retained reliability needs to be illustrated for future advanced CMOS technology. In this perspective, an undoped fin structure was proposed earlier as a potential way to overcome mobility/device mismatch degradation caused by scattering [3], [5]. The lightly doped-drain (LDD) portion is to lessen impact ionization and hot carrier injection (HCI) prior to highly doped junction [6]. However, the introduction of donors into the source/drain region caused scattering degradation. In line with this direction, the experiment was designed to study the LDD-free technology so as to reduce unfavorable scattering degradation, as well as to simplify the process. In this work, electrical characteristics of LDD and LDD-free FinFET devices with a dimension compatible with leading 14nm technology node have been studied. Furthermore, our research indicates the device without LDD implantation has better characteristics in terms of electrostatistic and Vtsat mismatch, as well as comparable device reliability of HCI.

II. FABRICATION AND PROCESS

FinFET devices of dimension compatible with leading 14nm technology node were fabricated on 300mm silicon substrate.

Silicon fins were formed to achieve higher on-state current and better leakage control. In this experiment, we have studied a full range of device Vtsat flavors from regular (RVT), low (LVT), to super low (SLVT). RVT, LVT and SLVT devices reflect the standard for most SoC application.

Device design in this experiment has concentrated on two groups which has and has no LDD implantation, respectively. Comprehensive electrical transport behaviors, as well as device reliability were collected in this experiment to demonstrate improved device characteristics and comparable reliability in device group with no LDD implantation.

III. RESULT AND DISCUSSION

Excellent device behaviors have been observed on the transfer curves of the device without LDD, shown in Figure 1(a). Inspecting the transfer behavior of the SLVT nFET device at

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

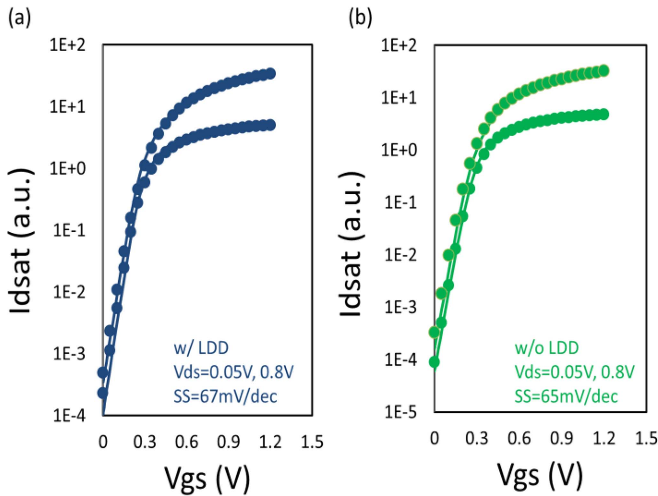

FIGURE 1. Transfer characteristics of devices in the dimension compatible with leading 14nm technology node of SLVT nFET in (a) with LDD device and (b) without LDD device, with Vds = 0.05V and 0.8V. Solid data points and lines represent electrical tested results, and TCAD simulations, respectively.

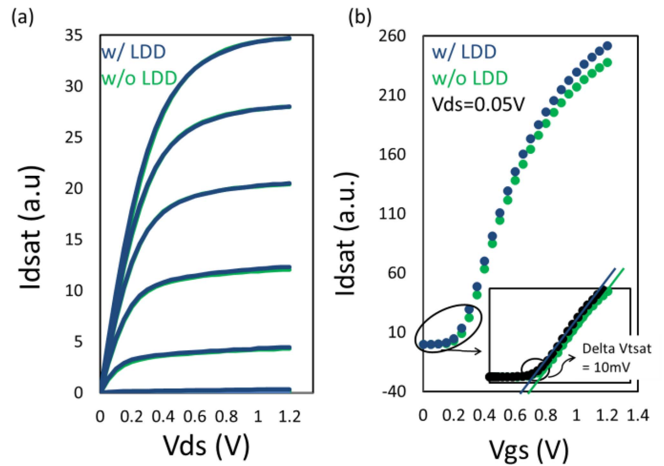

FIGURE 2. (a) Output characteristics of SLVT nFET for both w/ LDD and w/o LDD devices. Vgs varies from 0V to 1.2V, with a step of 200mV. (b) Transfer characteristics of SLVT nFET in linear scale, with a Vds of 0.05V. Threshold voltage extracted from linear extrapolation indicates only a ∼ +10mV Vtsat shift in device without LDD. Devices in the dimension compatible with leading 14nm technology node.

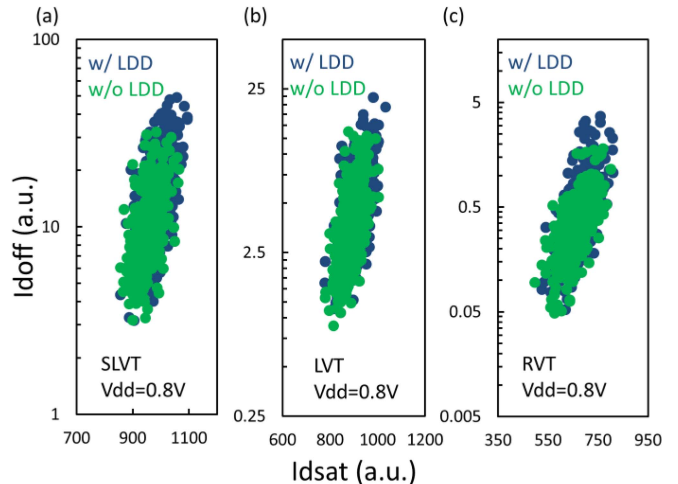

FIGURE 3. Device performance readout of nFET Idoff vs Idsat in (a) SLVT at Vdd = 0.8V, (b) LVT at Vdd = 0.8V, (c) RVT at Vdd = 0.8V. All suggest comparable device performance between two device groups.

Vds = 0.05V and 0.8V, superior electrostatic of core transistors with on/off ratio $>10^5$ was achieved. The SLVT device with sub-threshold swing of ∼67mV/dec has showed the state of the art short channel effect (SCE) immunity. Device without LDD, shown in Figure 1(b), shows similar on/off ratio behavior. More importantly, sub-threshold swing (SS) in device group without LDD has even better value of ∼65mV/dec. In both groups at normalized Vgs-Vtsat, on-state resistance which contains both channel resistance and contact resistance extracted at small Vds are comparable. Device with LDD-free expects to have higher on-state resistance due to changed junction where the parasitic contact resistance between junction and channel is reduced. However, experimental results in Figure 2(a) show the comparable value of on-state resistance in both groups, suggesting that S/D implants designed for LDD-free retain low contact resistance as well as on-state resistance. Threshold voltage extracted from linear extrapolation at low Vds bias, shifts toward the direction of the positive gate voltage, as ascribed in Figure 2(b). The ∼ +10mV shift in Vtsat can be explained by removal of the donor implantation from the channel of n-type transistor, which is equivalent to applying acceptor implantation in nFET for threshold voltage adjustment purpose.

A statistical study of key parameters is necessary and important so as to receive a solid understanding of device characterizes in all Vtsat flavors of nFET. Figure 3(a), (b), and (c) show the devices performance in different Vtsat flavors at Vdd = 0.8V. Clearly, at an operating voltage of 0.8V, nFET all flavors show comparable device performance in two groups, where with and without LDD devices electrical data points overlap each other. It should be noted that, for each Vtsat flavor, the device without LDD locates slightly on the colder side of Idoff/Idsat that is directly attributed to the Vtsat shift as mentioned previously. SLVT nFET device performance at lower operating voltage (Vdd = 0.55V) and higher operating voltage (Vdd = 1.2V) have also been evaluated and presented in Figure 4 (b) and (c). The consistent device performance in SLVT nFET transistors demonstrates an operating voltage independent behavior, both low power application, as well as high performance applications. We also studied ring oscillator (RO) performance Iddq vs Freq with respect to different device flavors in both groups. As shown in Figure 5(a) (b) (c), two device groups demonstrate a comparable RO performance.

Compared to the device with LDD, which has SS of ∼67mV/dec and a DIBL of 36 mV, the device without LDD implantation has better off-state characteristics with SS = 65mV/decade and DIBL = 33mV, shown in

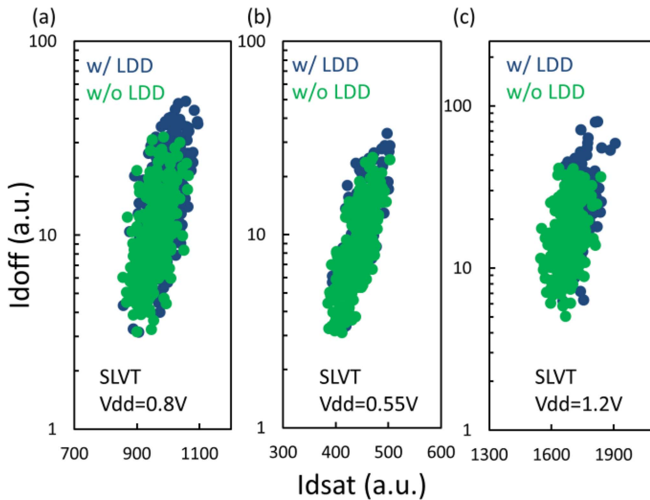

FIGURE 4. Device performance readout of nFET Idoff vs Idsat in (a) SLVT at Vdd = 0.8V (b) SLVT at Vdd = 0.55V, and (c) SLVT at Vdd = 1.2V. All suggest comparable device performance between two device groups.

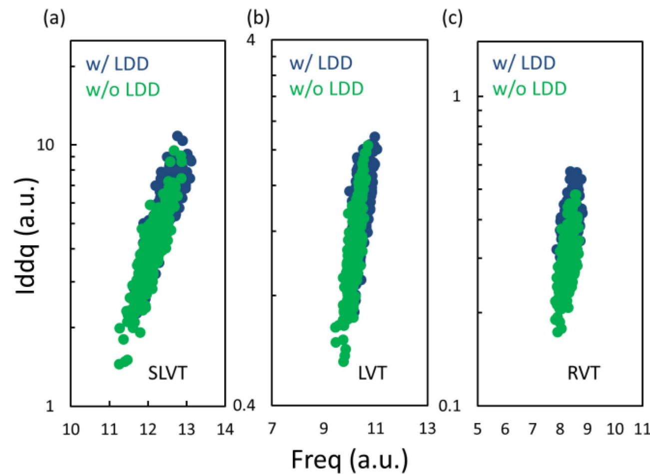

FIGURE 5. Device performance readout of RO Iddq vs Freq in (a) SLVT at Vdd = 0.8V, (b) LVT at Vdd = 0.8V, (c) RVT at Vdd = 0.8V. All suggest comparable device performance between With LDD and Without LDD devices.

Figure 6(a). The observation of excellent subthreshold behavior in LDD-free group can be fairly attributed to the junction push-out when LDD implantation has been removed from junction/channel regime. As shown in Figure 6(b), the device without LDD enjoys an improved DIBL when running at smaller overlap capacitance. Overlap capacitance Cov, which quantitatively describes the overlap region between gate and drain, is an important index of SCE. To corroborate our experimental findings that Without LDD group benefits better off-state characteristics and to determine the individual contribution from device architecture, TCAD simulation was introduced and performed to support electrical testing results. As depicted in Figure 7(a) and (b), junction profiles of the two groups are plotted overlapped on each other. We observe that the junctions close to the silicon-oxide interface are further apart from each other in the LDD-free device where the

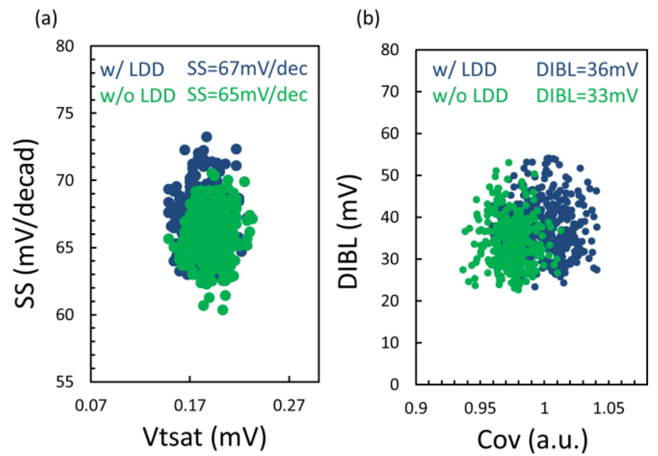

FIGURE 6. Statistical studies of off-state characteristics, in terms of (a) SS vs Vtsat, and (b) DIBL vs Cov in both device groups.

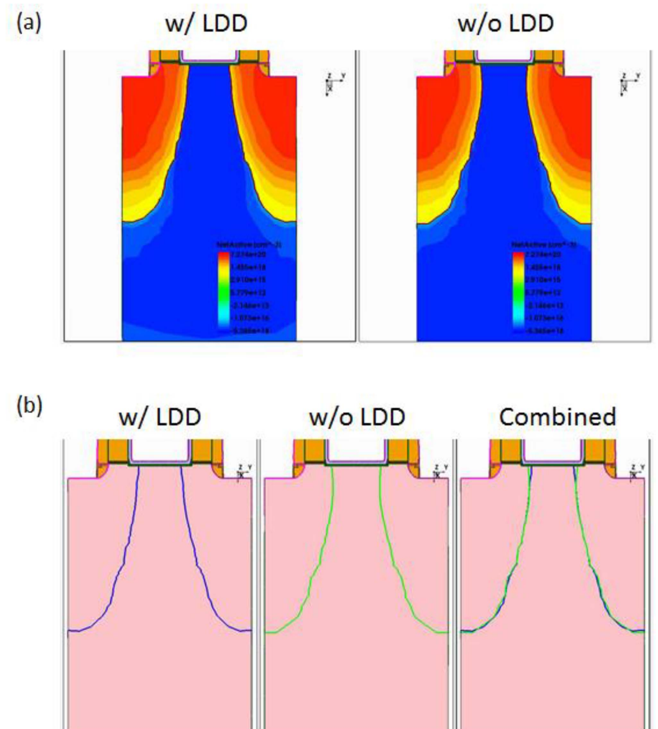

FIGURE 7. (a) Cross-section of TCAD junction profile in SLVT nFET for both groups. TCAD decks are calibrated with real process TEM images at every major process steps and include all high temperature thermal budgets to capture dopant activation and diffusion. (b) The overlapped plot compares junction profiles of both of the devices.

Cov is smaller as compared to the device with LDD implantation. Our theoretical results are consistent with experiment, confirming that off-state electrostatic characteristic benefits LDD-free device with smaller gate/junction overlap.

Device analog characteristics are also compared in both groups. A reduction of device Vtsat mismatch (AVT) by 20% in nFETs, is presented in Figure 8(a) when devices is without LDD implantation. At different normalized areas of device physical structure, devices without LDD all show significant sigma Vtsat reduction in standard deviation. One

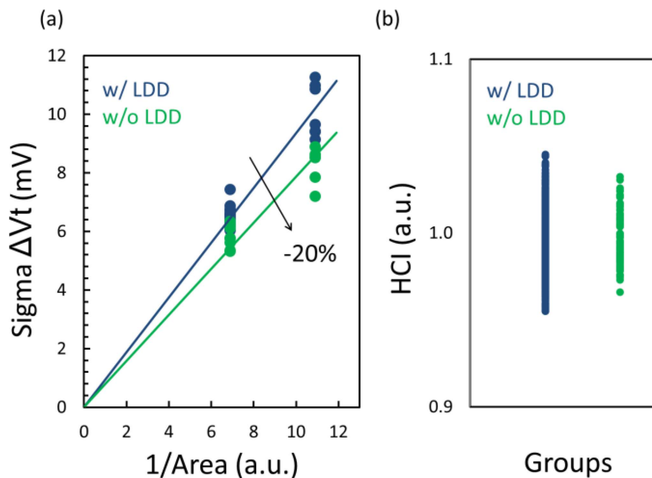

FIGURE 8. (a) AVT varies with normalized device area in w/o LDD device gains a ∼−20% reduction of device Vtsat mismatch. (b) Inline VRS measured HCI for both device groups, where w/ LDD and w/o LDD devices share similar HCI.

of the main advantages of having no LDD is to have less implantation and therefore, improved random dopant fluctuation and Vtsat mismatch [3], [5]. LDD-free is in line with current multi-work function purpose which is to utilize undoped fins to benefit device characteristic in terms of mobility and logic/SRAM mismatch by eliminating dopant scattering [3], [5]. Key device reliability has also been examined and characterized in Figure 8(b). HCI was tested by inline voltage ramp stress (VRS) [7]. During the VRS test, drain voltage Vds was ramped up with the gate voltage Vgs synchronously. A specific Vds was recorded when the Idsat shifted by 10%. As presented in Figure 8(b), HCI values between two groups, with and without LDD, are comparable. HCI can be surely retained in FinFET architecture [8].

IV. CONCLUSION

Device characteristics comparison between two device groups, with LDD and without LDD implantation, has been experimentally studied on FinFET structure with a dimension compatible with leading 14nm technology node. In contrast of previous planar FETs, FinFET technology reveals its immunity to HCI effect. A latter research can be further expanded to different fin width and gate underlap area so as to optimize the junction profile to achieve better device reliability/performance in sub-14nm gate length device suites [9]. Experimental results in device group without LDD implantation show improved electrostatic characteristic, reduced device Vtsat mismatch, and retained device reliability of HCI as compared to device group with LDD.

REFERENCES

[1] J. Singh *et al.*, "Analog, RF, and ESD device challenges and solutions for 14 nm FinFET technology and beyond," in *Proc. Symp. VLSI Technol. (VLSI-Technol.) Digest Tech. Papers*, Honolulu, HI, USA, 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894378.

[2] H. C. Lo *et al.*, "A 12 nm FinFET technology featuring 2nd generation FinFET for low power and high performance applications," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2018, pp. 215–216, doi: 10.1109/VLSIT.2018.8510632.

[3] S. Narasimha *et al.*, "A 7 nm CMOS technology platform for mobile and high performance compute application," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 295.1–29.5.4, doi: 10.1109/IEDM.2017.8268476.

[4] S.-Y. Wu *et al.*, "A 7 nm CMOS platform technology featuring 4th generation FinFET transistors with a 0.027 um^2 high density 6-T SRAM cell for mobile SoC applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 2.6.1–2.6.4, doi: 10.1109/IEDM.2016.7838333.

[5] M. Togo *et al.*, "Multiple workfunction high performance FinFETs for ultra-low voltage operation," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2018, pp. 81–82, doi: 10.1109/VLSIT.2018.8510641

[6] C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation–model, monitor, and improvement," *IEEE J. Solid-State Circuits*, vol. 20, no. 1, pp. 295–305, Feb. 1985, doi: 10.1109/JSSC.1985.1052306.

[7] B. Zhu *et al.*, "TCAD simulation on FinFET n-type power device HCI reliability improvement," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2019, pp. 1–4, doi: 10.1109/IRPS.2019.8720558.

[8] X. Wan, B. Zhu, M. Mohan, K. Wu, D. Choi, and A. Gondal, "HCI improvement on 14nm FinFET IO device by optimization of 3D junction profile," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2019, pp. 1–4, doi: 10.1109/IRPS.2019.8720526.

[9] J. H. Stathis *et al.*, "Reliability challenges for the 10 nm node and beyond," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, 2014, pp. 20.6.1–20.6.4, doi: 10.1109/IEDM.2014.7047091.