Received 22 August 2020; revised 11 September 2020; accepted 16 September 2020. Date of publication 21 September 2020; date of current version 4 November 2020. The review of this article was arranged by Editor A. Nathan.

Digital Object Identifier 10.1109/JEDS.2020.3025545

Heterostructure Ge-Body pTFETs for Analog/RF Applications

SAYANI GHOSH [1,2], KALYAN KOLEY [3] (Senior Member, IEEE), SAMAR K. SAHA [4] (Life Fellow, IEEE), AND CHANDAN K. SARKAR [1] (Senior Member, IEEE)

1 Nano Device Simulation Laboratory, Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata 700032, India
2 Department of Electronics and Communication Engineering, University of Engineering and Management, Kolkata 700160, India
3 Department of Electronics Engineering, Indian Institute of Technology Dhanbad, Dhanbad 826004, India
4 Department of Process, Device, and Compact Modeling, Prospicient Devices, Milpitas, CA 95035, USA

CORRESPONDING AUTHOR: S. GHOSH (e-mail: sayani.ghs@gmail.com)

This work was supported in part by Department of Science and Technology, Government of India.

ABSTRACT This article presents a systematic study on the analog and radio-frequency (RF) performance of type-II staggered heterostructure *p*-channel tunnel field-effect transistors (*p*TFETs) with Ge (Germanium) channel and different compound semiconductor source. In order to study the figure-of-merits (FOMs) of analog and RF performances, various Ge-channel *p*TFETs are designed with Ge, GaAsP, SiGe, and InAlAs sources. The numerical simulation data show an improvement in the FOMs of analog performance such as drain current (I_{ds}), transconductance (g_m), transconductance-generation-factor (g_m/I_{ds}), and intrinsic gain ($g_m R_o$) of the devices with compound semiconductor source compared to Ge-source *p*TFET devices. Similarly, an improvement in the RF FOMs such as gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances, maximum frequency of oscillation (f_{MAX}), and cutoff frequency (f_T) is observed for the devices with GaAsP, SiGe, and InAlAs source compared to Ge-source *p*TFETs. The simulation results also show that the common-source amplifiers, designed with Ge-heterostructure *p*TFETs, exhibit a significant enhancement in gain and Gain-Bandwidth product of the circuit.

INDEX TERMS Tunnel field-effect transistors, p-type germanium body, RF/analog performance, NQS effect, device simulation.

I. INTRODUCTION

As the CMOS technology scales down to its ultimate scaling limit of metal-oxide-semiconductor field-effect transistor (MOSFET) miniaturization, the power dissipation and chip area have become critical issues [1], [2]. Thus, in the current and next generation technology nodes, the energy efficient devices with low power, high speed, and high on chip packing density are of great demands [3]. Besides power dissipation, the scaled MOSFET devices are, also, constrained by the theoretical limit of subthreshold swing (SS) of 60 mV/decade of current at room temperature [4]. This limitation of SS in the conventional MOSFETs causes a significant increase in the off-state leakage current (I_{off}) and power dissipation [2]. In order to, surmount the limitations of MOSFETs in the next generation technology node, the tunnel field-effect transistors, referred to as the "TFETs," show a great potential to replace the conventional MOSFETs due to their carrier injection mechanism by inter-band or band-to-band tunneling (BTBT) in contrast to the thermal injection of carriers in MOSFETs [1], [5]. The inter band tunneling provides a large tunneling barrier for the current carriers in the off-state of the device and lowers the value of SS bellow 60 mV/decade at 300K [5], [6]. As a result, the value of I_{off} is significantly lower than that of the MOSFETs with identical dimensions resulting in lower power dissipation. However, in the on-state, the BTBT at the source-channel junction provides on current (I_{on}) and higher I_{on}/I_{off} ratio as required for IC chip design. In spite of the above described advantages of TFETs, the silicon (Si) TFETs suffer from low I_{on} and therefore, low operational speed due to their high effective mass and large bandgap [7]. Hence, the materials with small bandgap (E_g)

are needed to obtain high I_{on}, [5], [8]. Thus, recently, germanium (Ge) has drawn a lot of attentions to design *p*-type TFETs (*p*TFETs) to achieve higher I_{on} due to its lower values of bandgap and effective mass and higher value of hole mobility compared to Si [9]–[13].

Again, in addition to Ge body, the value of I_{on} can be further improved by source-channel tunnel-junction engineering. The reported data show that I_{on} of TFETs depends highly on the doping levels and abruptness as well as on the effective bandgap at the source-body tunnel-junction [14]. As the effective band gap decreases, the tunneling barrier decreases, hence tunneling rate increases, which ameliorate the on current [15]. This low tunneling barrier source-body tunnel-junction TFETs can be achieved by using type-II staggered heterojunction [14]. Experimental data show that the staggered heterostructure TFET devices improve tunneling probability at the source-body junction [16]–[18]. Though different heterostructure Ge-TFETs and tunneling mechanisms have been reported to improve the performance of these devices [8], [12], however, to the best of authors' knowledge, the study on the analog/RF performance including non-quasi-static (NQS) effect of the heterostructure Ge-TFETs has not been reported. Therefore, in this work, different staggered heterojunction *p*TFETs are designed with GaAsP, SiGe, and InAlAs source and Ge-body and drain to evaluate the analog/RF performance of these devices [19].

The objective of this article is to evaluate the analog/RF performance of staggered heterostructure Ge-*p*TFET devices and compare that with the Ge source and body, hereafter, referred to as the "all Ge-*p*TFET" devices. In order to achieve this objective, first of all, we have designed different device structures with Ge-body and Ge, $Si_{1-x}Ge_x$, $In_{1-x}Al_xAs$, and $GaAs_xP_{1-x}$ sources. Then we describe the simulation methodology to generate the static and dynamic characteristics of the devices to extract the relevant device parameters. The parameters used to evaluate the analog performance of the devices include drain current (I_{ds}), transconductance (g_m), transconductance-generation-factor (g_m/I_{ds}), output-resistance (R_o), and intrinsic gain (g_mR_o). And, the parameters extracted to evaluate the RF performance of the same devices include intrinsic gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances, gate-to-drain intrinsic resistance (R_{gd}), transport delay (τ_m), maximum frequency of oscillation (f_{MAX}), and cutoff frequency (f_T). Next, the optimization technique of the mole-fraction of the selected source materials is discussed. Finally, the figure-of-merits (FOMs) for the analog/RF performances of the Ge-body *p*TFETs with $Si_{1-x}Ge_x$, $In_{1-x}Al_xAs$, and $GaAs_xP_{1-x}$ sources are compared with that of the all Ge-*p*TFETs.

II. DEVICE ARCHITECTURE

Fig. 1 shows two-dimensional cross-section of an ideal symmetric double gate (DG) *p*TFET device structure used in this study. The structure includes two gates each with effective gate oxide thickness (EOT), t_{ox}, channel length, L_{gate}, *n*-type Ge-body with thickness t_{body}, *p*+ Ge drain, and *n*+ source. In this study, different *p*-type TFETs with Ge-body and Ge *p*+ drain are designed with different compound semiconductors (GaAsP, SiGe, and InAlAs) as *n*+ sources. The technology parameters used in device design are listed in Table 1. Typically, TFETs have equal source and drain concentration, however, in this study *p*+ drain doping concentration (5×10^{18} cm^{-3}) is kept lower than the *n*+ source doping concentration (10^{20} cm^{-3}) to combat the reverse tunneling of electrons at drain/body junction for positive gate bias (ambipolar conduction) [20]. During numerical simulation, very low body doping concentration of 1×10^{16} cm^{-3} is used to inhibit random dopant fluctuations. We have assumed ideal TFET device structures with abrupt source-body and drain-body junctions.

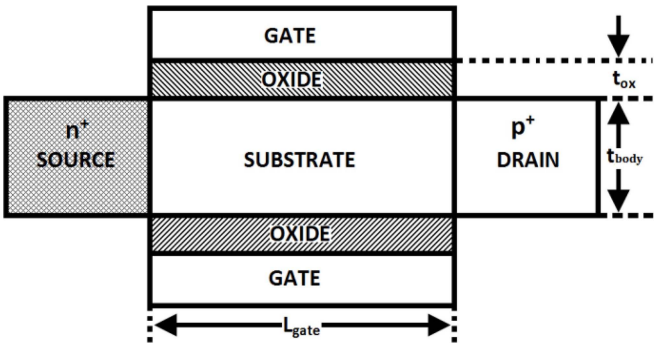

FIGURE 1. Two-dimensional cross section of an ideal double gate *p*TFET device structure. In the figure, t_{body} is the thickness of the *n*+ source, *n*-type Ge body, *p*+ Ge drain, and t_{ox} is the gate oxide thickness. Different devices are designed using Ge, $Si_{1-x}Ge_x$, $In_{1-x}Al_xAs$, and $GaAs_xP_{1-x}$ source materials.

TABLE 1. Values for technology parameters.

Parameters	Values
N^+ Source Doping, N_s	1×10^{20} cm^{-3}
N Body Doping, N_{ch}	1×10^{16} cm^{-3}
P^+ Drain Doping, N_d	5×10^{18} cm^{-3}
EOT (t_{ox})	1.2 nm
Gate Metal Work Function	4.7 eV
Gate Length, L_{gate}	50 nm
Body Thickness, t_{body}	25 nm

The technology parameters shown in Table 1 are used to generate heterostructure Ge-*p*TFETs with different source materials for numerical device simulation using common-gate configuration. The devices are then appropriately biased to investigate the improvement in I_{on} compared to all Ge-pTFETs. Then the RF performances of these heterostructure TFETs are, also, analyzed to assess the feasibility of heterostructure Ge-*p*TFETs in RF applications [20]. The voltages applied to the gate and drain electrodes with reference to the source are V_{gs} and V_{ds}, respectively. The simulation methodology is described in Section III.

III. SIMULATION METHODOLOGY

In this study, the Sentaurus technology computer-aided design (CAD) tool is used for simulation of the devices described in Section II [21]. In the simulation process,

the drift-diffusion carrier transport model along with doping dependent Masetti mobility model is used to include the effect of impurity scattering. The tunneling current is determined by Kane's non-local BTBT model [22]. The drain current I_{ds}, obtained by volume integration of the band-to-band generation rate (G_{btb}) is given as [23]

$$I_{ds} = q \int G_{btb} dV \tag{1}$$

The expression for G_{btb} as a function of energy band gap (E_g) and maximum applied electric field (E) at the source/body tunnelling junction is given by [23]

$$G_{btb} = \mathrm{A}\frac{|E|^2}{\sqrt{E_g}} \exp\left[-B\frac{E_g^{3/2}}{|E|}\right] \tag{2}$$

In Eq. (2), A and B are the parameters that can be optimized to account for the effective mass of a material. We also, have used Shockley Read Hall (SRH) generation-recombination model to compute the active carrier life time and high-field model to account for velocity saturation of carriers. The grid spacing of the simulation structure for numerical device simulation is optimized considering the trade-off between the accuracy of simulation results and convergence [24]. Since GaAsP, SiGe, and InAlAs have considerable lattice mismatch with Ge-body TFETs, the strain induced deformation potential model MLDA is used to consider the strain induced effect due to lattice mismatch at the tunnelling junction. Furthermore, the MLDA, also, models the structural confinement [2], [5] at the semiconductor–oxide interface and surface quantization effects. All simulation is performed at ambient temperature, $T = 300$ K.

For Ge-TFETs device simulation, the default physical constants implemented in Sentaurus device CAD tools are inadequate to achieve accurate simulation data. Therefore, some of the most critical physical parameters are used from the experimentally verified reported data [25], [26] as presented in Table 2.

Using the above described models and physical constants, the device simulation is performed to generate current-voltage ($I-V$) and capacitance-voltage ($C-V$) characteristics of Ge-*p*TFETs with different source materials under different biasing conditions. From the simulation data, the analog FOMs are extracted at gate voltage (V_{gs}) varying from 0 to – 1.1 V at a constant drain voltage, $V_{ds} = -0.8$ V. And, RF FOMs are extracted at $V_{gs} = -1.1$ V and $V_{ds} = -0.8$ V. In this article, the value of threshold voltage (V_{th}) is extracted from the $I_{ds} - V_{gs}$ plots at $V_{ds} = -0.8$ V and I_{ds} of 10^{-7}(A/μm); the value of I_{on} is extracted at the biasing condition, $V_{gs} = -1.1$ V and $V_{ds} = -0.8$ V; and I_{off} is extracted at $V_{gs} = 0$ and $V_{ds} = -0.8$ V.

Before generating $I-V$ and $C-V$ characteristics, the mole fraction of each compound semiconductor source material is optimized to achieve best I_{on}/I_{off} ratio and average SS of Ge-pTFET devices as described in Section IV.

TABLE 2. Values of simulation model parameters [25], [26].

Para meters	Definitions	Values		Units
		electrons	holes	
tau_{min}		0	0	s
tau_{max}	SRH Doping- and Temperature-dependent Parameters (Scharfetter)	4×10^{-5}	4×10^{-5}	s
N_{ref}		10^{14}	10^{14}	cm^{-3}
Υ		0.85	0.85	-
T_{α}		-1.5	-1.5	-
T_{coeff}		2.55	2.55	-
E_{trap}		0	0	eV
μ_{min1}	Mobility due to Impurity Scattering (Doping Dependence)	60	60	cm^2/Vs
μ_{min2}		0	0	cm^2/Vs
μ_1		20	40	cm^2/Vs
Pc		10^{17}	9.23×10^{16}	cm^{-3}
Cr		8×10^{16}	2×10^{17}	cm^{-3}
Cs		3.43×10^{20}	10^{20}	cm^{-3}
A		0.55	0.55	-
B		2.0	2.0	-
V_{sat0}	High lateral field mobility (HighField Dependence)	6×10^6	6×10^6	cm/s
μ_{max}	Mobility due to Phonon Scattering (Constant Mobility)	3900	1900	$cm^2 V^{-1} s^{-1}$
exponent		2.5	2.2	-
B	High Transversal Field dependant Mobility (Enormal Dependence)		1.993×10^5	cm/s
C			4.875×10^3	$cm^{5/3}V^{-2/3}s^{-1}$
N_0			1	cm^{-3}
λ			0.0317	-
k			1	-
δ			1.705×10^{11}	cm^2 / V. s
A			1.5	-
α⊥			0	cm^{-3}
N1			1	cm^{-3}
υ			1	-
η			2.0546×10^{30}	$V^2 cm^{-1} s^{-1}$
l_{crit}			10^{-6}	cm

IV. OPTIMIZATION OF MOE FRACTION

In order to set an optimized value of mole fraction, x for Ge, Al, and As of the $Si_{1-x}Ge_x$, $In_{1-x}Al_xAs$, and $GaAs_xP_{1-x}$ source materials, the simulated values of *SS* and I_{on}/I_{off} ratio are plotted for respective Ge-pTFET as a function of the mole fraction as shown in Fig. 2. It is observed from Fig. 2(a) that for $Si_{1-x}Ge_x$ source, as mole fraction increases, the value of *SS* increases whereas, I_{on}/I_{off} ratio decreases. To achieve a lower value of *SS* and a higher value of I_{on}/I_{off} ratio, the mole fraction is fixed at the optimized value of 0.2. For $In_{1-x}Al_xAs$ source, both SS and I_{on}/I_{off} ratio change rapidly with mole fraction as shown in Fig. 2(b). Therefore, a moderate value of $x = 0.4$ is set for Al mole fraction to achieve the highest possible value of I_{on}/I_{off} ratio for the lowest possible value of *SS*. For $GaAs_xP_{1-x}$ source material, on the other hand, both *SS* and I_{on}/I_{off} ratio decreases with the increase in the value of mole fraction as shown in Fig. 2(c). Thus, there is a trade-off between *SS* and I_{on}/I_{off} ratio in selecting a suitable value of x for $GaAs_xP_{1-x}$ source. In this

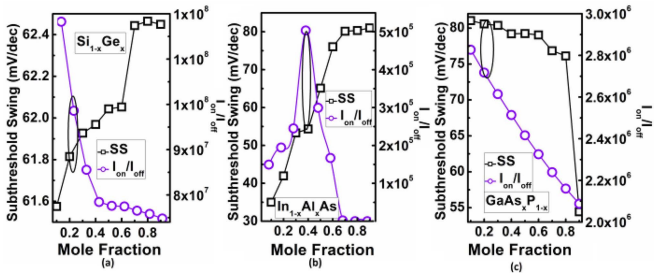

FIGURE 2. Optimization of mole fraction: mole fraction versus *SS* and I_{on}/I_{off} ratio for different source materials (a) $Si_{1-x}Ge_x$, (b) $In_{1-x}Al_xAs$, and (c) $GaAs_xP_{1-x}$.

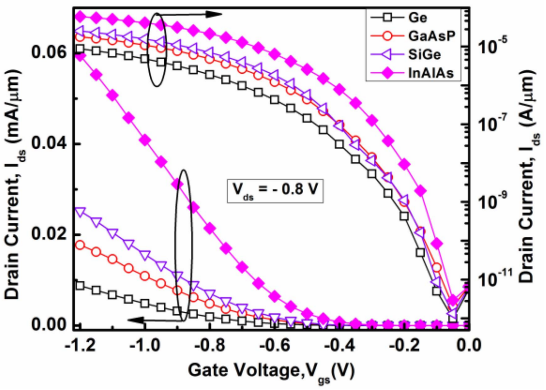

FIGURE 3. Variation of I_{ds} in logarithmic scale (right y-axis) and in linear scale (left y-axis) as a function of gate voltage V_{gs} for 50 nm Ge-body *p*TFET with Ge, GaAsP, SiGe, and InAlAs as source material at $V_{ds} = -0.8$ V.

study, $x = 0.2$ is set to achieve the highest possible value of I_{on}/I_{off} ratio for devices with $GaAs_xP_{1-x}$ source material.

V. RESULTS AND DISCUSSIONS

A. ANALOG PERFORMANCE

In order to assess the analog performance of the Ge-*p*TFETs with $Si_{1-x}Ge_x$, $In_{1-x}Al_xAs$, and $GaAs_xP_{1-x}$ source materials, the simulated $I_{ds} - V_{gs}$ data for each device and the corresponding extracted device parameters, I_{ds}, g_m, g_m/I_{ds}, R_o, and g_mR_o are compared to all Ge-*p*TFET device. Fig. 3 shows the simulated $I_{ds} - V_{gs}$ characteristics of Ge-pTFETs with different source materials. It is observed from Fig. 3 that the heterostructure devices outperform all Ge-*p*TFETs with improved I_{on}. This is because at the same biasing condition, the tunneling barrier for GaAsP, SiGe, and InAlAs source devices is lower compared to the all Ge-*p*TFETs as observed from the energy band diagrams of the corresponding devices shown in inset of Fig. 4 obtained at $V_{gs} = -1.1$ V and $V_{ds} = -0.8$ V. Due to the lower tunneling barrier of the heterostructure devices compared to all Ge devices, the electrons from the channel valence band tunnel into the available states of the source conduction band, thus, creating holes in the body and a sequential increase in I_{on} for GaAsP, SiGe, and InAlAs source devices in accordance to the tunnelling barrier compared to the Ge source devices.

Fig. 5 shows the variation of g_m and g_m/I_{ds} for different Ge-*p*TFET devices as a function of gate overdrive voltage

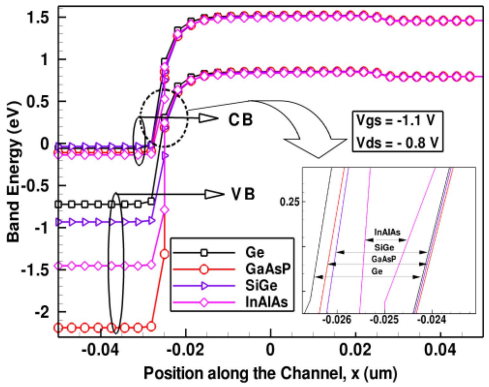

FIGURE 4. Simulated energy band diagram for Ge-*p*TFETs with Ge, GaAsP, SiGe, and InAlAs as source materials obtained at $V_{gs} = -1.1$ V and $V_{ds} = -0.8$ V. The inset shows the sequential increase in tunneling barrier for InAlAs < SiGe < GaAsP < Ge source devices.

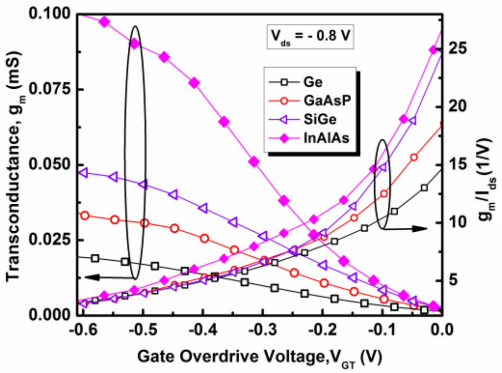

FIGURE 5. Variation of g_m and g_m/I_{ds} as a function of gate overdrive voltage V_{GT} for 50 nm Ge-body *p*TFET with Ge, GaAsP, SiGe, and InAlAs as source materials at $V_{ds} = -0.8$ V.

$V_{GT}(= V_{gs} - V_{th})$. It is observed from Fig. 5 that the values of $g_m$of the heterostructure Ge-*p*TFETs are higher than that of the all Ge-*p*TFETs. As discussed earlier (inset of Fig. 4), the heterostructure Ge devices have lower tunneling barrier than the corresponding homojunction device. As a result, more electrons tunnel through the source-body junction causing an increase in the carrier transport through the channel for the GaAsP, SiGe, and InAlAs source Ge-*p*TFETs compared to the conventional all Ge-*p*TFETs thus, affecting the current drivability. Consequently, a significant improvement in the value of g_m is observed with decreasing energy barrier of the tunnel junction of the heterostructure devices (inset of Fig. 4) over the entire range of V_{GT} as shown in Fig. 5.

It is, also, observed from Fig. 5 that the values of g_m/I_{ds} of the heterostructure Ge-*p*TFETs are higher than the all Ge-*p*TFET for low values of $|V_{gs}|$ ($|V_{GT}| < 0.3$ V). However, at the higher values of $|V_{GT}| > 0.3$ V, the heterostructure devices, do not show any significant improvement in the value of g_m/I_{ds} over all Ge-*p*TFETs. These $g_m/I_{ds} - V_{GT}$ characteristics at higher values of $|V_{GT}|$ is insignificant for analog performance since the amplification of the analog circuits is considered to show the best result in the subthreshold region operation of the devices.

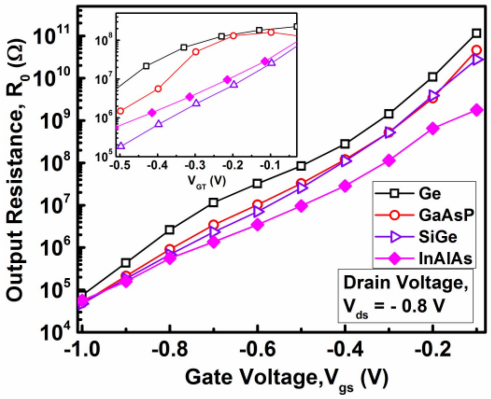

FIGURE 6. R_o versus V_{gs} plots for 50 nm Ge-body *p*TFETs with Ge, GaAsP, SiGe, and InAlAs sources at $V_{ds} = -0.8$ V. Inset shows the variation of R_o as a function of V_{GT}.

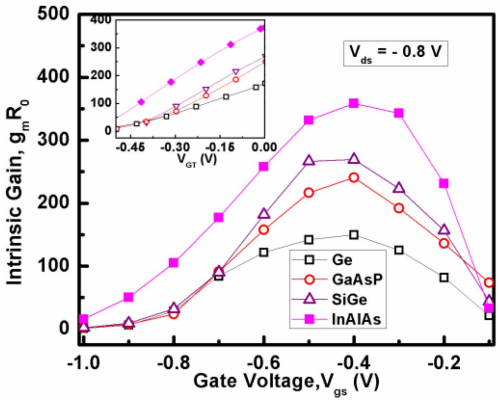

FIGURE 7. $g_m R_o$ versus V_{gs} plots for 50 nm Ge-body *p*TFETs with Ge, GaAsP, SiGe, and InAlAs sources at $V_{ds} = -0.8$ V. Inset shows the variation of $g_m R_o$ as a function of V_{GT}.

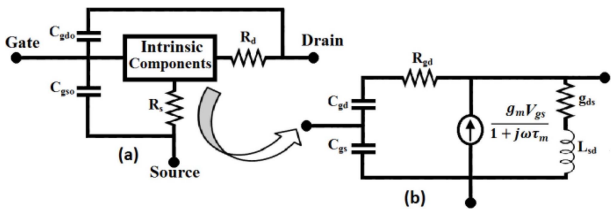

FIGURE 8. (a) Equivalent circuit of a *p*TFET device for the extraction of RF and NQS parameters: (b) Circuit schematic of intrinsic components; small-signal equivalent circuit. In the figure, C_{gso} and C_{gdo} are the bias independent extrinsic capacitances at the source and drain end of the device, respectively and R_s and R_d are the source and drain resistances respectively; C_{gs} and C_{gd} are the bias dependent intrinsic capacitances at the source and drain end of the device, R_{gd} is the bias dependent intrinsic drain resistance, τ_m is the transport delay, and L_{sd} is the inductance in order to consider the effect of the τ_m in the source-drain admittance.

Fig. 6 shows the variation in R_o as a function of both V_{gs} and V_{GT}. As observed in inset of Fig. 4, the tunneling barrier is the lowest for InAlAs and highest for Ge sources and varies in the sequence InAlAs < SiGe < GaAsP < Ge source materials for Ge-*p*TFETs. Since, the devices with lower tunneling barrier at the source/body junction correspond to higher band narrowing, therefore, the band narrowing also increases in the order of InAlAs > SiGe > GaAsP > Ge source devices. As band narrowing enhances, the lateral electric field due to the applied drain bias influences the tunneling junction more effectively. As a result, the conductivity (g_{ds}) of the channel increases and saturation behavior degrades proportionately as InAlAs > SiGe > GaAsP > Ge source devices. Therefore, R_o being the inverse of g_{ds}, increases as InAlAs < SiGe < GaAsP < Ge source devices due to the degraded output current saturation as shown in Fig. 6. In order to illustrate the variation in R_o at $V_{gs} > V_{th}$ condition with more clarity, the R_o versus V_{GT} is also given in the inset of Fig. 6.

The variation of $g_m R_o$ with respect to V_{gs} for different source materials is shown in Fig. 7. It is observed from Fig. 7 that the InAlAs source device has highest value of $g_m R_o$ in spite of having lowest value of R_o among all the devices as shown in Fig. 6. This is due to the fact that for InAlAs source device, g_m is very high compared to the other devices as shown in Fig. 5 and this high value of g_m dominates over low value of R_o resulting in highest $g_m R_o$ for InAlAs source device as shown in Fig. 7. The inset in Fig. 6 shows that the SiGe, and GaAsP source devices have lower value of R_o for the entire range of variation in V_{GT}. However, for the lower values of V_{GT}, the higher value of g_m compensates quietly over R_o thus, offering higher intrinsic gain compared to all Ge-*p*TFET. Thus, $g_m R_o$ increases gradually in the sequence of Ge < GaAsP < SiGe < InAlAs as shown in Fig. 7.

B. RF PERFORMANCE

The devices used for analog study are also used for the RF performance analysis. The RF study includes a detailed investigation of the set of NQS parameters {C_{gs}, C_{gd}, R_{gd}, τ_m} along with the set of frequency FOMs (f_T, f_{MAX}). In order to obtain the target NQS parameters and frequency FOMs, the values of Y-parameters are extracted for the small signal equivalent circuit shown in Fig. 8 using the following expressions [27]

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{3}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})}{\omega} \tag{4}$$

$$R_{gd} = -\frac{\mathrm{Re}(Y_{12})}{\omega^2 C_{gd}^2} \tag{5}$$

$$\tau_m = -\frac{1}{g_m}\left(\frac{\mathrm{Im}(Y_{21})}{\omega} + C_{gd}\right) \tag{6}$$

Before analyzing the intrinsic Y-parameters, the extrinsic gate to source/drain capacitances (C_{gdo} and C_{gso}) and extrinsic source/drain resistances (R_s and R_d) are de-embedded. The bias independent extrinsic capacitances C_{gdo} and C_{gso} at the drain and source end, respectively consist of inner fringing, outer fringing, and overlap capacitances. As RF analysis is performed in the super-threshold condition, the inner fringing capacitance becomes zero. In addition, since in this study, we have considered abrupt source/drain body junction, the overlap capacitance can be neglected. Hence,

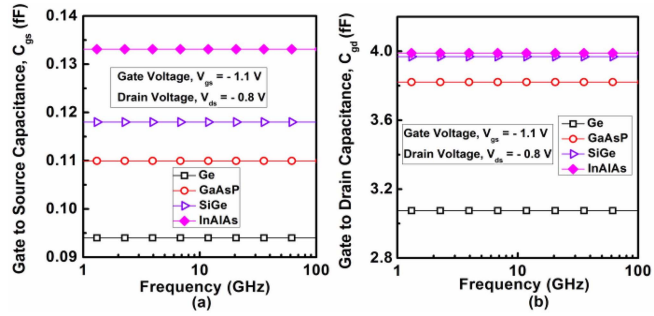

FIGURE 9. Intrinsic capacitance versus frequency plots of 50 nm Ge-*p*TFETs with Ge, GaAsP, SiGe, and InAlAs as source materials at $V_{ds} = -0.8$ V: (a) C_{gs}, (b) C_{gd}.

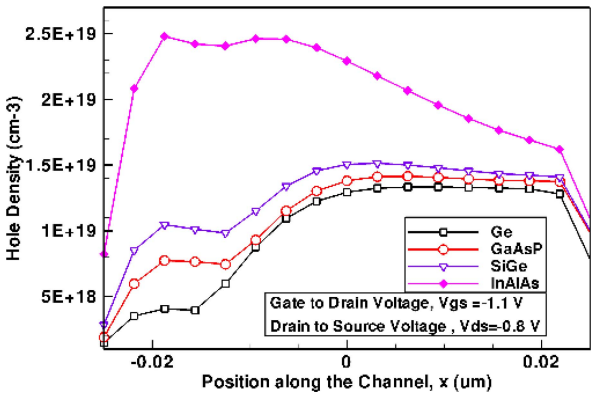

FIGURE 10. Variation in the density of holes along the channel for Ge-pTFETs with Ge, GaAsP, SiGe, and InAlAs as source materials at $V_{gs} = -1.1$ V and $V_{ds} = -0.8$ V. The middle of the channel along the *x*-axis between the source and drain is considered as '$x = 0$.' The source is on the $-x$ direction outside scale and drain is on the $+x$ direction beyond the scale.

only the outer fringing capacitance is of significance in extrinsic capacitances which is derived from the expression $C_{of} = 2\varepsilon_{ox}/\pi \ln[1 + t_g/t_{ox}]$ where ε_{ox} is the permittivity of oxide layer, t_g is the gate thicknesses and t_{ox} is the gate oxide layer thicknesses [5]. The parameters R_s and R_d of each device are extracted at $V_{gs} = 0$ V using the following expressions [28]

$$R_S = \frac{\mathrm{Re}(Y_{11}) + \mathrm{Re}(Y_{21})}{[\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{21})]^2} \tag{7}$$

$$R_d = -\frac{\mathrm{Re}(Y_{21})}{(\mathrm{Im}(Y_{21}))^2} \tag{8}$$

Using the above described extrinsic parameters the Y-parameters are de-embedded following the reported procedure of [29].

Fig. 9 shows the intrinsic capacitances, C_{gs} and C_{gd} versus frequency plots for Ge-*p*TFETs with different source materials. It is observed from Fig. 9 that the value of C_{gs} and C_{gd} are independent of frequency within the range $1 \leq f \leq 100$ GHz [29]; however, the values are different for different source materials. This is because the hole density is different for Ge-*p*TFETs with different source materials for the same biasing condition ($V_{gs} = -1.1$ V and $V_{ds} = -0.8$ V) due to different tunneling barriers (inset of Fig. 4). Since InAlAs source device has lowest tunneling barrier, therefore, has the highest tunneling at the source-channel tunnel junction and consequently, shows the highest hole density in the channel as shown in Fig. 10. Thus, InAlAs-*p*TFETs device shows highest values of C_{gs} and C_{gd} as shown in Fig. 9. Thereafter, the capacitance decreases sequentially as SiGe > GaAsP > Ge in proportion to tunneling barrier of the corresponding Ge-*p*TFET devices. The observed higher value of C_{gd} than C_{gs} in Fig. 9 is due to the pinch-off of the inversion region at the source-end; pulling the inversion region away from the source [30].

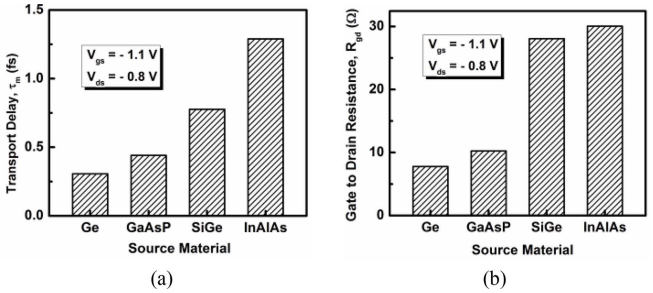

FIGURE 11. Intrinsic transport parameters for 50 nm Ge-body *p*TFETs with different source materials at $V_{ds} = -0.8$ V and frequency 11.8 GHz: (a) τ_m and (b) R_{gd}.

It is observed from Fig. 10 that the hole density increases from low to high value for the source materials Ge, GaAsP, SiGe, and InAlAs of the Ge-*p*TFET devices. This enhancement in the hole density results in enhanced scattering. Thus, due to the direct dependency of carrier mobility on scattering mechanisms, carrier mobility also degraded in heterostructure devices. This causes degradation in the transport delay given by [4]

$$\tau_m \propto L_g^2 \Big/ \mu V_{GT} \tag{9}$$

From equation (9), it is observed that τ_m increases with the decrease in the carrier mobility. Thus, τ_m increases from low to high value with the source materials as Ge, GaAsP, SiGe, and InAlAs of the Ge-*p*TFET devices as observed in Fig. 11(a) due to degradation in the carrier mobility by enhanced carrier-carrier scattering in the heterostructure devices. The value of τ_m affects gate to drain resistance, R_{gd} of TFET devices.

It is well known that τ_m determines the response time of the channel charge to the input signal and is modelled by $R_{gd}C_{gd}$. And, R_{gd} is the virtual resistance of the channel caused by the charge coupling between the gate and drain terminals [27] and is responsible for the delay in carrier response. As can be seen from Fig. 11(a) that τ_m increases from low to high values for the Ge, GaAsP, SiGe, and InAlAs source devices. Since resistance of a device increases with the increase in the carrier delay, as a result, R_{gd} increases sequentially for Ge-*p*TFETs with source materials in the order of Ge, GaAsP, SiGe, and InAlAs as shown in Fig. 11(b).The parameters τ_m and R_{gd} are found to be

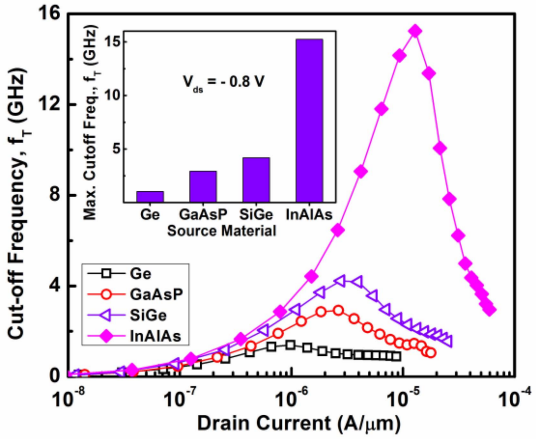

FIGURE 12. Variation of f_T with drain current for 50 nm Ge-*p*TFETs with Ge, GaAsP, SiGe, and InAlAs source materials at $V_{ds} = -0.8$ V. Inset shows the variation in maximum value of f_T for 50 nm Ge–*p*TFETs with Ge, GaAsP, SiGe, and InAlAs as source materials.

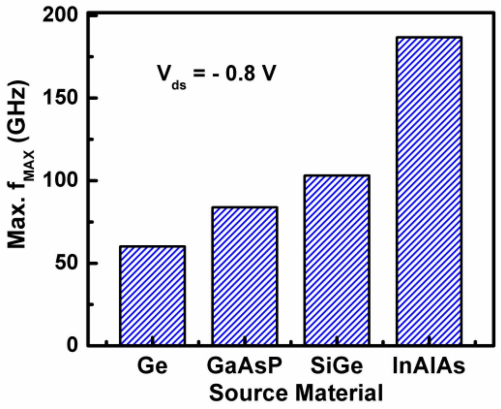

FIGURE 13. Variation in maximum value of f_{MAX} for 50 nm Ge-*p*TFETs with Ge, GaAsP, SiGe, and InAlAs as source materials.

independent of frequency [29], however, dependent on the source materials as shown in Fig. 11.

The use of different heterostructure source materials in Ge-body pTFETs prominently improves RF performances in terms of cut-off frequency (f_T) and maximum frequency of oscillation (f_{MAX}). f_T being the frequency at unity current gain, is expressed as [31], [32]

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{10}$$

The f_{MAX}, which is the frequency at unity power gain, is given by [32]

$$f_{MAX} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(R_s + R_i + R_g\right)\left(g_{ds} + g_m C_{gd}/C_{gs}\right)}} \tag{11}$$

From expression (10), we find that f_T is determined by the ratio of g_m and $C_{gg}(= C_{gs} + C_{gd})$. It is observed from Fig. 5 and Fig. 9 that the change in C_{gg} for various source materials in Ge-*p*TFET is not so significant for all values of V_{gs} whereas g_m increases rapidly from all Ge devices to GaAsP, SiGe, and InAlAs source devices. Thus, the change

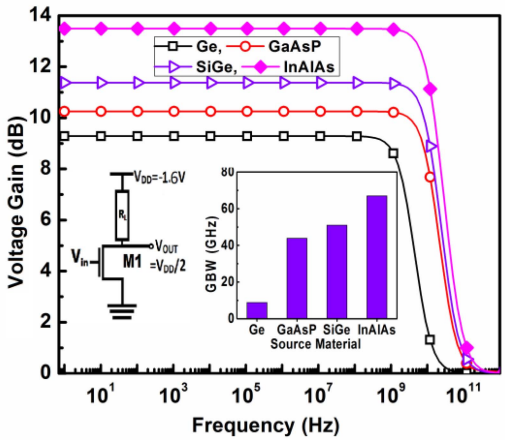

FIGURE 14. Variation in the voltage gain (in dB) with frequency for 50 nm Ge-*p*TFETs with Ge, GaAsP, SiGe, and InAlAs as source materials. Inset shows the variation in maximum value of GBW (Gain-Bandwidth Product) for 50 nm Ge-pTFETs with Ge, GaAsP, SiGe, and InAlAs source materials.

in g_m is predominant over the minor change in C_{gg}. Hence, it is obvious that, f_T will increase from all Ge devices to GaAsP, SiGe, and InAlAs source devices being dominated by g_m as shown in Fig. 12.The f_{MAX} is directly dependent on f_T and thus follows the nature of improvement in f_T as shown in Fig. 13.

C. CIRCUIT PERFORMANCE

The circuit performances of Ge-*p*TFET devices with Ge, GaAsP, SiGe, and InAlAs sources are analyzed using common source (CS) amplifier. The voltage gain of an amplifier is defined by [33]

$$A_V = \frac{V_{out}}{V_{in}} = \frac{(sC_{GD} - g_m)R_D}{R_S R_D C_{GD} C_{GS} s^2 + \left[R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D C_{GD}\right]s + 1} \tag{12}$$

Fig. 14 shows the frequency response of the common source amplifier with 50 nm channel length for all Ge-*p*TFET and GaAsP, SiGe, and InAlAs source Ge-body *p*TFETs of the same dimension. According to equation (12), in the low frequency range when ω is negligible, the voltage gain is given by $-g_m R_D$ where R_D is the parallel combination of load resistance R_L and device output resistance R_o. As the changes in both g_m and R_o with different source materials are significant enough, they both affect the gain performance. So it can be derived that the changes in gain with various source materials will follow the sequence of changes in the product term of g_m and R_o that is, $g_m R_o$. In consequence, it is clear from Fig. 14 that at constant value of R_L for each circuit, the gain is minimum for all Ge-*p*TFETs and maximum for that of InAlAs source Ge-*p*TFETs similar to $g_m R_o$ as shown in Fig. 7.

VI. CONCLUSION

This article presents a comparative analysis of analog and RF FOMs of the Ge-body *p*TFETs with different compound

semiconductors as source materials and the conventional all Ge-*p*TFETs. For the presented device structures, the heterostructure *p*TFET devices with InAlAs, SiGe, and GaAsP as source materials are found to offer remarkable analog and RF performances in terms of I_{ds}, g_m, g_mR_o, intrinsic capacitances, f_T, f_{MAX}, and GBW product compared to all Ge-*p*TFETs. However, the device parameters R_o, intrinsic resistance, and transport delay due to NQS effect tend to degrade for heterostructure Ge-*p*TFETs compared to all Ge-*p*TFETs. Thus, a proper optimization technique is required to achieve the best performance of the heterostructure Ge-*p*TFETs. This study clearly shows that the performance of Ge-body *p*TFETs with different compound semiconductor as source materials, are comparatively superior to all Ge-*p*TFET devices. Thus, the staggered heterostructure Ge-*p*TFET devices can be optimized as suitable alternatives for application specific analog/RF domain.

REFERENCES

[1] S. Ghosh, K. Koley, S. K. Saha, and C. K. Sarkar, "Non-quasi-static effect on Ge-body pTFET for different source materials," in *Proc. IEEE Electron Devices Technol. Manuf. Conf.*, Penang, Malaysia, Apr. 2020, pp. 509–512. [Online]. Available: https://doi.org/10.1109/EDTM47692.2020.9117888

[2] S. K. Saha, *FinFET Devices for VLSI Circuits and Systems*, 1st ed. Boca Rotan, FL, USA: CRC Press, 2020. [Online]. Available: https://doi.org/10.1201/9780429504839

[3] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010. [Online]. Available: https://doi.org/10.1109/JPROC.2010.2070470

[4] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York, NY, USA: McGraw-Hill, 1999. [Online]. Available: https://dl.acm.org/doi/book/10.5555/27167

[5] S. K. Saha, *Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond*. Boca Rotan, FL, USA: CRC Press, 2015. [Online]. Available: https://doi.org/10.1201/b19117

[6] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-*k* gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007. [Online]. Available: https://doi.org/10.1109/TED.2007.899389

[7] D. Leonelli *et al.*, "Silicide engineering to boost Si tunnel transistor drive current," *Jpn. J. Appl. Phys.*, vol. 50, no. 7, pp. 1725–1733, Jul. 2011. [Online]. Available: https://doi.org/10.7567/JJAP.50.04DC05

[8] Y. Yang *et al.*, "Germanium–tin P-channel tunneling field-effect transistor: Device design and technology demonstration," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4048–4056, Dec. 2013. [Online]. Available: https://doi.org/10.1109/TED.2013.2287031

[9] M. Heyns *et al.*, "Advancing CMOS beyond the Si roadmap with Ge and III/V devices," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Washington, DC, USA, Dec. 2011, pp. 1–4. [Online]. Available: https://doi.org/10.1109/IEDM.2011.6131543

[10] K. C. Saraswat, C. O. Chui, D. Kim, T. Krishnamohan, and A. Pethe, "High mobility materials and novel device structures for high performance nanoscale MOSFETs," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, San Francisco, CA, USA, Dec. 2006, pp. 1–4. [Online]. Available: https://doi.org/10.1109/IEDM.2006.346871

[11] P. Zimmerman *et al.*, "High performance Ge pMOS devices using a Si-compatible process flow," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, San Francisco, CA, USA, Dec. 2006, pp. 1–4. [Online]. Available: https://doi.org/10.1109/IEDM.2006.346870

[12] E. H. Toh, G. H. Wang, G. Samudra, and Y. C. Yeoa, "Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications," *J. Appl. Phys.*, vol. 103, no. 10, 2008, Art. no. 104504. [Online]. Available: https://doi.org/10.1063/1.2924413

[13] Y. Yang *et al.*, "Germanium-tin n-channel tunneling field-effect transistor: Device physics and simulation study," *J. Appl. Phys.*, vol. 113, no. 19, 2013, Art. no. 194507. [Online]. Available: https://doi.org/10.1063/1.4805051

[14] K. E. Moselund, H. Schmid, C. Bessire, M. T. Björk, H. Ghoneim, and H. Riel, "InAs–Si nanowire heterojunction tunnel FETs," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1453–1455, Oct. 2012. [Online]. Available: https://doi.org/10.1109/LED.2012.2206789

[15] D. Mohata *et al.*, "Barrier-engineered arsenide–antimonide heterojunction tunnel FETs with enhanced drive current," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1568–1570, Nov. 2012. [Online]. Available: https://doi.org/10.1109/LED.2012.2213333

[16] S. K. Gupta, J. P. Kulkarni, S. Datta, and K. Roy, "Heterojunction intra-band tunnel FETs for low-voltage SRAMs," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3533–3542, Dec. 2012. [Online]. Available: https://doi.org/10.1109/TED.2012.2221127

[17] P. Guo *et al.*, "Tunneling field-effect transistor with Ge/$In_{0.53}Ga_{0.47}As$ heterostructure as tunneling junction," *J. Appl. Phys.*, vol. 113, no. 9, Mar. 2013, Art. no. 094502. [Online]. Available: https://doi.org/10.1063/1.4794010

[18] R. Li *et al.*, "InAs/AlGaSb heterojunction tunnel field-effect transistor with tunnelling in-line with the gate field," *Phys. Status Solidi C*, vol. 9, no. 2, pp. 389–392, Feb. 2012. [Online]. Available: https://doi.org/10.1002/pssc.201100241

[19] A. Mallik and A. Chattopadhyay, "Tunnel field-effect transistors for analog/mixed-signal system-on-chip applications," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 888–894, Apr. 2012. [Online]. Available: https://doi.org/10.1109/TED.2011.2181178

[20] N. N. Mojumder and K. Roy, "Band-to-band tunneling ballistic nanowire FET: Circuit-compatible device modeling and design of ultra-low-power digital circuits and memories," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2193–2201, Oct. 2009. [Online]. Available: https://doi.org/10.1109/TED.2009.2028394

[21] *Sentaurus TCAD Manuals*, Synopsys Inc., Mountain View, CA, USA, 2009.

[22] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, pp. 83–91, Jun. 2004. [Online]. Available: https://doi.org/10.1063/1.1735965

[23] M. G. Bardon, H. P. Neves, R. Puers, and C. V. Hoof, "Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827–834, Apr. 2010. [Online]. Available: https://doi.org/10.1109/TED.2010.2040661

[24] S. Saha, "MOSFET test structures for two-dimensional device simulation," *Solid-State Electron.*, vol. 38, no. 1, pp. 69–73, Jan. 1995. [Online]. Available: https://doi.org/10.1016/0038-1101(94)E0050-O

[25] G. Hellings *et al.*, "Electrical TCAD simulations of a germanium pMOSFET technology," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2539–2546, Oct. 2010, doi: 10.1109/TED.2010.2060726.

[26] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Sorée, G. Groeseneken, and K. D. Meyer, "Direct and indirect band-to-band tunneling in germanium-based TFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 292–301, Feb. 2012. [Online]. Available: https://doi.org/10.1109/TED.2011.2175228

[27] S. Cho, K. R. Kim, B.G. Park, and I. M. Kang, "Analyses on small-signal parameters and radio-frequency modeling of gate-all-around tunneling field-effect transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4164–4171, Dec. 2011. [Online]. Available: https://doi.org/10.1109/TED.2011.2167335

[28] S. Cho, J. S. Lee, K. R. Kim, B.G. Park, J. S. Harris, and I. M. Kang, "RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1388–1396, May 2011. [Online]. Available: https://doi.org/10.1109/TED.2011.2109724

[29] I. M. Kang and H. Shin, "Non-quasi-static small-signal modeling and analytical parameter extraction of SOI FinFETs," *IEEE Trans. Nanotechnology*, vol. 5, no. 3, pp. 205–210, May 2006. [Online]. Available: https://doi.org/10.1109/TNANO.2006.869946

[30] Y. Yang, X. Tong, L.-T. Yang, P.-F. Guo, L. Fan, and Y.-C. Yeo, "Tunneling field-effect transistor: Capacitance components and modeling," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 752–754, Jul. 2010. [Online]. Available: https://doi.org/10.1109/TNANO.2006.869946

[31] V. Kilchytska *et al.*, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 577–588, Mar. 2003. [Online]. Available: https://doi.org/10.1109/TED.2003.810471

[32] S. Ghosh, K. Koley, S. K. Saha, and C. K. Sarkar, "Influence of the gate height engineering on the intrinsic parameters of UDG-MOSFETs with nonquasi static effect," *IEEE J. Electron Devices Soc.*, vol. 3, no. 5, pp. 410–417, Sep. 2015, doi: 10.1109/JEDS.2015.2438026.

[33] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2002. [Online]. Available: https://dl.acm.org/doi/book/10.5555/1594009