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Generation of STDP With Non-Volatile Tunnel-FET Memory for Large-Scale and Low-Power Spiking Neural Networks

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ABSTRACT Spiking neural networks (SNNs) have attracted considerable attention as next-generation neural networks. As SNNs consist of devices that have spike-timing-dependent plasticity (STDP) characteristics, STDP is one of the critical characteristics we need to consider to implement an SNN. In this study, we generated the STDP of a biological synapse with non-volatile tunnel-field-effect-transistor (tunnel FET) memory that has a charge-storage layer and a tunnel FET structure. Tunnel FET is a promising structure to reduce the operation voltage owing to its steep sub-threshold slope. Therefore, the non-volatile tunnel-FET memory we propose enables the implementation of low-operation-voltage SNNs. This article reports the $I - V$, programming, and both symmetric and asymmetric STDP characteristics of a non-volatile tunnel-FET memory with p-channel-MOS-like operation.

INDEX TERMS Spiking neural network, tunnel FET, MONOS, spike-timing-dependent plasticity, synaptic device.

I. INTRODUCTION

Neuromorphic computing is expected to be a suitable architecture to process flexible tasks such as image recognition. In particular, neural networks (NNs) are promising candidates to perform cognitive tasks that cannot be readily executed via conventional von Neumann computing [1], [2]. Deep neural networks (DNNs) are a type of NN that have been widely used; they have achieved remarkable results in various fields. Spiking neural networks (SNNs) have also received considerable attention. Compared to DNNs, SNNs have the potential to realize low-power NN systems. This is because in DNNs, processing is performed using analog signals, whereas in SNNs, processing is performed using binary or ternary digital signals.

It is generally agreed that the weight coefficient changes of biological synapses are based on Hebbian learning. Fig. 1 shows the synaptic weight change based on Hebbian learning. In Hebbian learning, the weight coefficients of the synapse change according to the timing difference between the signals arriving from the presynaptic and postsynaptic neurons. As the timing difference between the pre- and post-signals is reduced, the updated weight coefficients increase. However, when the difference is near

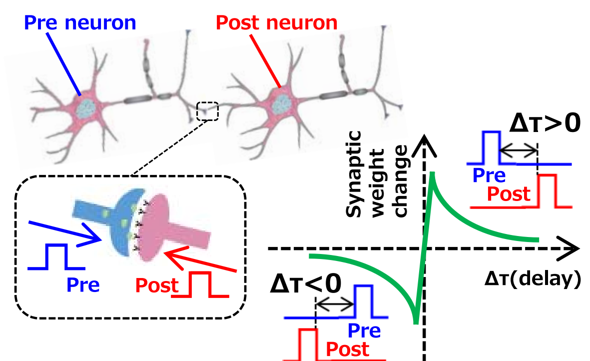

FIGURE 1. Schematic illustration of the effect of the delay between the post and pre spike on synaptic weight changes.

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zero, the coefficient rapidly approaches zero. To implement neuromorphic computing with Hebbian learning, a synaptic device constitutes a critical component [3], [4]. Many types of synaptic devices that consist of semiconductor memory have been developed. However, there are some issues to be resolved while implementing these devices. For example, a two-terminal device such as a resistive-change device needs additional switching devices. In the case of a volatile memory, such as static random-access memory (SRAM), high standby power consumption will be an issue. Therefore, some researchers have studied floating-gate-based synaptic devices with the spike-timing-dependent plasticity (STDP) of biological synapses [5], [6], as shown in Fig. 1 Floating-gate memory can reproduce the STDP of a biological synapse by exploiting the amount of injected charges. The injected charges induce a shift in the threshold voltage of the memory cell. Therefore, we can regard the threshold voltage shift as the synaptic weight change. Many prior studies have developed synaptic devices with floating-gate or charge-trapping memories, e.g., a metal-oxide-nitride-oxide-semiconductor (MONOS) structure, to implement SNN circuits [7], [8]. Both floating-gate and charge-trapping memories are suitable for large-scale SNNs owing to their simple one-transistor structure compared with other non-volatile memories, such as phase-change random-access memory, resistive random-access memory, and spin-orbit torque switching [9]–[12].

Tunnel field-effect transistors (tunnel-FETs) have also attracted considerable attention as ultra-low-operation-voltage devices. As a tunnel FET has steep subthreshold slope characteristics owing to an operation based on band-to-band tunneling (BTBT), its operating voltage can be reduced. Thus, tunnel-FETs can reduce the power consumption of circuits.

A non-volatile tunnel-FET memory consists of the MONOS and tunnel-FET structures [13]. This memory device has many advantages, such as low-voltage operation and small cell size. Therefore, a non-volatile tunnel-FET is a memory device with potential for large-scale integration and low-power operation. In this study, we propose the use of a non-volatile tunnel-FET memory as a synaptic device to achieve large-scale low-power SNN circuits, as shown in Fig. 2. The figure also shows the schematic images of how to reproduce the biological synapse STDP with non-volatile tunnel-FET memory. The proposed memory device can reproduce the synaptic weight coefficient using a number of trapped charges. In a previous study of ours, we demonstrated the symmetric and asymmetric STDP characteristics of a non-volatile tunnel FET with an operation similar to that of an n-channel metal-oxide-semiconductor (nMOS) [14]–[16]. Specifically, tunnel FETs can operate like an nMOSFET because of BTBT between the P-type source and the body under positive-biased gate. However, the tunnel current between different polar semiconductors results in a lower voltage operation compared with the tunnel current between a P-type drain and a P-type source, as shown in Fig. 3(b). In

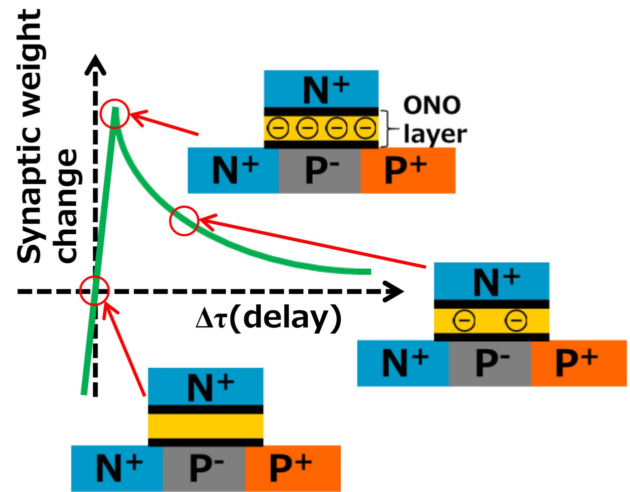

FIGURE 2. Biological synapse STDP reproduced with threshold voltage shift induced by charge trapping.

this study, to induce tunnel current between the P-type body and the N-type source, we used p-channel MOS (pMOS) like operation with negative-biased gate.

This study concludes that a tunnel-FET-based charge trapping memory can reproduce the symmetric and asymmetric STDP characteristics of biological synapses. The STDP characteristics were obtained under pMOS-like operation with negative-biased gate.

II. NON-VOLATILE TUNNEL FET MEMORY

Charge-trapping memories have been typically used as synaptic devices to compose SNN circuits owing to their small cell area [17]. However, conventional charge-trapping memories require a high operation voltage, which leads to high power consumption. In addition, the power consumption will increase with the improvement of the integration degree of neural network circuits. Therefore, low-voltage synaptic devices are required to implement low-power large-scale SNNs. To reduce the operation voltage, we propose a non-volatile tunnel-FET memory [13], [18]. The proposed memory device consists of the MONOS and tunnel-FET structures. The MONOS-structure memory is a suitable memory for implementing large-scale SNN circuits owing to the simple cell structure. Tunnel FETs achieve a steep sub-threshold slope through BTBT. Therefore, a tunnel-FET-based structure can provide the SNN circuit with a lower operation voltage. The proposed memory device structure is a promising candidate for implementing large-scale low-power SNN circuits owing to the simple cell structure of the charge trapping memory and the steep sub-threshold slope of the tunnel FET.

Fig. 3 shows the energy band diagram during OFF and ON state of the pMOS-like tunnel FET induced by BTBT effect between the N-type source and the P-type body. The threshold voltage of the proposed memory device is modulated by the quantity change of charge trapped in the SiN layer. We can use this threshold voltage as a synaptic weight. The

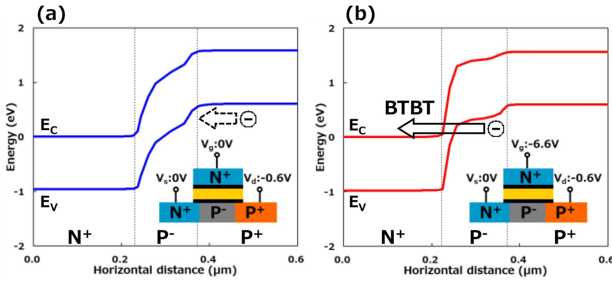

FIGURE 3. Energy band diagram of (a) OFF-state and (b) ON-state non-volatile tunnel-FET memory with pMOS like operation.

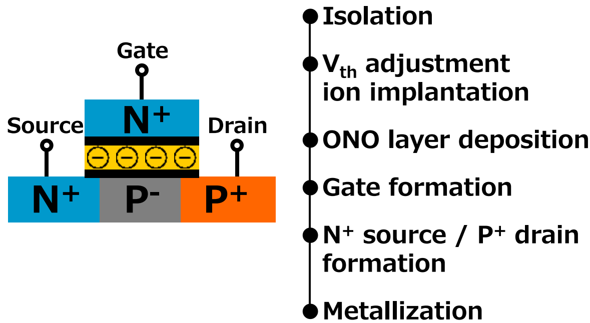

FIGURE 4. Process flow of the non-volatile tunnel-FET memory cell with MONOS structure.

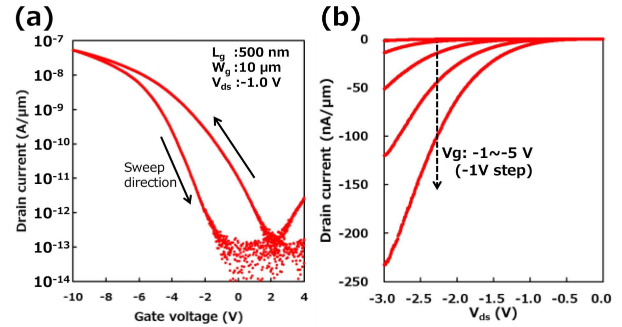

FIGURE 5. (a) $I_d - V_g$ characteristics and (b) $I_d - V_{ds}$ characteristics of the fabricated pMOS-like non-volatile tunnel-FET memory cell. $I_d - V_d$ characteristics were measured under negative-biased gate.

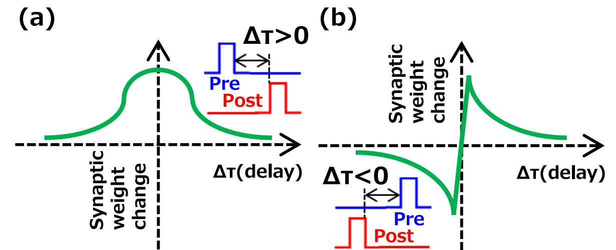

FIGURE 6. (a) Symmetric and (b) asymmetric STDP characteristics.

proposed memory device is a one-transistor structure and has the possibility of low-voltage operation. Therefore, to implement large-scale and low-power SNN circuits, the proposed memory device structure is promising. In this study, we fabricated the proposed non-volatile tunnel-FET memory and evaluated the STDP characteristics.

III. FABRICATION AND I–V CHARACTERISTICS

Fig. 4 illustrates the process flow of the non-volatile tunnel-FET memory. In this study, we used the ONO (SiO_2/SiN/SiO_2) layer for charge retention. First, we performed the isolation process on bulk Si wafers. Then, we formed SiO_2 layer with thermal oxidation. Subsequently, the SiN and SiO_2 layers were deposited by low-pressure chemical vapor deposition (LP-CVD). The thickness of the ONO layer was 8/15/3 nm. After ONO layer deposition, we also deposited the Poly-Si through LP-CVD as the gate electrode material. Then, we formed the gate electrode through inductively coupled plasma reactive-ion etching. The N-type source and the P-type drain regions were subsequently formed through ion implantation. Each doped region was defined using an electron beam lithography system (JEOL: JBX-6300FS) with high alignment accuracy. The source and the drain regions were activated with rapid thermal annealing. The activation temperature and time were 1050 °C and 10 s, respectively. Finally, the metallization process was performed.

Fig. 5(a) and (b) shows the drain current and gate voltage ($I_d - V_g$) and the drain current and voltage between the drain and source ($I_d - V_{ds}$) characteristics, respectively of the fabricated memory device. Here, the physical gate length and width were 0.5 μm and 10 μm, respectively. We measured the $I_d - V_g$ characteristics with gate voltages ranging from −10 to 10 V and from 10 to −10 V. We observed the ON current under both positive and negative gate voltages. The ON current under positive gate voltage was induced by BTBT between the P-type drain and the body region. The ON current under negative gate voltage was induced by BTBT between the N-type source region and the P-type body regions. We also obtained a typical hysteresis of the conventional MONOS memory. The ON current was approximately 240 nA/μm at 3.0 V source–drain voltage and 5.0 V gate voltage in Fig. 5(b). The value of ON current was lower than that for a conventional MONOS memory. We need to consider a method that improves the ON current. We confirmed that the fabricated non-volatile tunnel-FET memory has the typical characteristics of memory devices. Next, we measured and evaluated the symmetric and asymmetric STDP characteristics, which are key characteristics to form SNNs.

IV. STDP CHARACTERISTICS

Both symmetric and asymmetric STDP characteristics, as shown in Fig. 6, are essential to implement SNNs. To decide the programming pulse for the STDP measurements, we evaluated the effect of the voltage of the programming pulse on the threshold voltage shift of the fabricated non-volatile tunnel-FET memory. Fig. 7 shows the measurement results. Both the source voltage and the drain voltages were set to 0 V during the programming and erasing operations. The threshold voltage (V_{th}) shift was defined as the difference between the V_{th} of the programmed state and the original

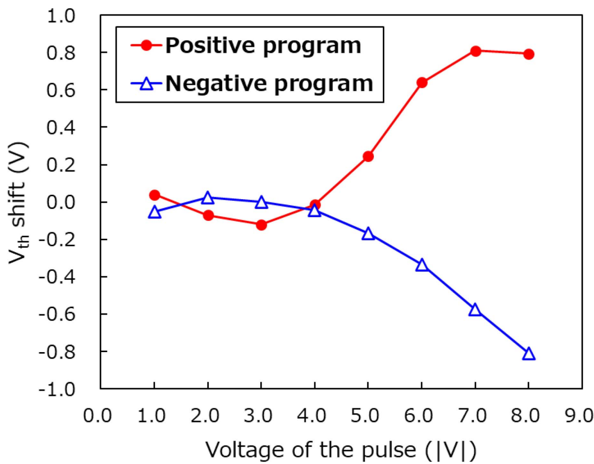

FIGURE 7. Effect of positive and the negative voltages of the pulse for positive and negative programming operation on the V_{th} shift.

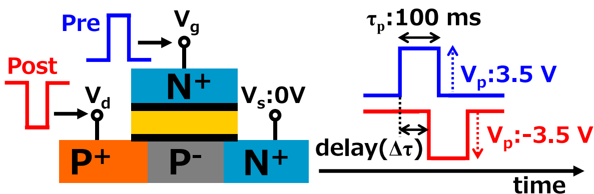

FIGURE 8. Pulse setup for symmetric STDP measurement.

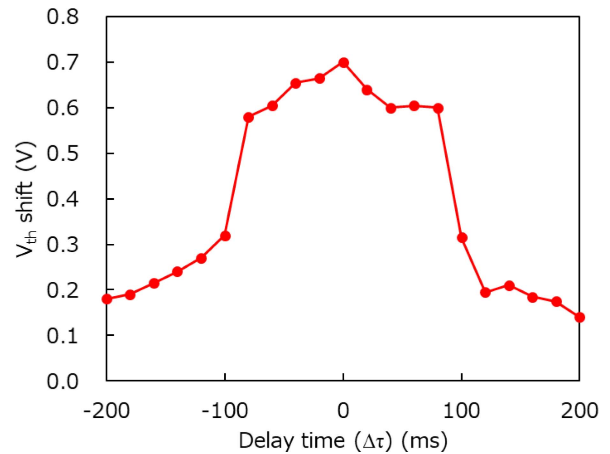

FIGURE 9. Effect of delay time on the V_{th} shift with the pulse setup shown in Fig. 8.

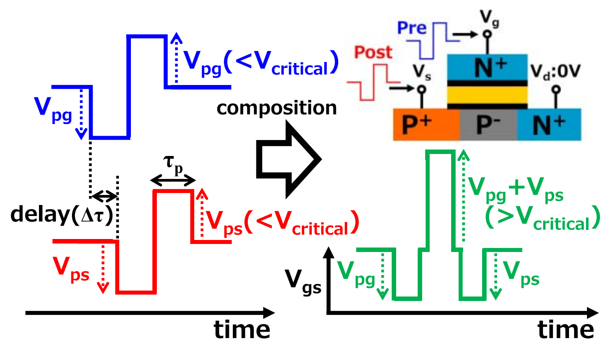

FIGURE 10. Pulse setup for asymmetric STDP measurement.

state obtained by the erasing operation. The pulse width (τ_p) for the programming and erasing operations was 100 ms. Positive and negative voltages were applied to the gate electrode for the positive and negative programming operations, respectively. Here, the positive and the negative program signify the V_{th} shifts induced by the positive and the negative gate voltage, respectively. We can assume that the positive and the negative program were induced by the electron and hole injections, respectively. The V_{th} shift increased drastically at 4 V. These results indicate that a voltage below 4 V leads to little effect on the memory window of the fabricated non-volatile tunnel-FET memory cell. We used these results to decide the waveform to measure the STDP characteristics.

First, we measured the symmetric STDP characteristics of the non-volatile tunnel-FET memory cell using the measurement setup shown in Fig. 8. To evaluate the synaptic weight update, we measured the V_{th} shift produced by a pair of rectangular pulses. One pulse was applied to the gate electrode, whereas the other was applied to the drain. Here, $\Delta\tau$ indicates the delay time between the two rectangular pulses. The width (τp) and the absolution value of the amplitude ($|V_p|$) were 100 ms and 3.5 V, respectively. The source voltage was 0 V during the programming operation. From the programming characteristic measurements presented in Fig. 7, we can conclude that only the pre-pulse cannot produce the critical effects on V_{th} of the fabricated non-volatile tunnel-FET memory cell. Therefore, it is inferred that we can obtain similar programming characteristics that are presented in Fig. 7 when the programming pulses are applied to the P-type drain; this is because a similar field is induced between the gate and the body. Therefore, we could also conclude that only post-pulse cannot produce critical effects on the V_{th}. Fig. 9 shows the measurement results of the STDP characteristics for the fabricated non-volatile tunnel-FET memory cell using the pulse setup shown in Fig. 8. We observed that the fabricated device could reproduce symmetric STDP characteristics. A high voltage of 7.0 V was applied between the gate electrode and the P-type body when two pulses overlapped. Therefore, the time interval during which high voltage was applied decreased with an increase in the delay between two pulses. Thus, V_{th}, which depends on the trapping charge, is reduced by an increase in the delay time. This result indicates that we can use the proposed device as a synaptic device using V_{th} instead of the weight coefficient.

To reproduce asymmetric STDP characteristics of a biological synapse in the floating gate memory or the charge trapping memory, previous studies used triangular waveforms [19], [20]. However, triangular waveforms lead to an increase of the circuit scale and power consumption. In this study, we implemented asymmetric STDP characteristics of biological synapses using a bipolar pulse, which can be achieved with a low-scale circuit and low power consumption. Fig. 10 illustrates the bipolar pulses, which were

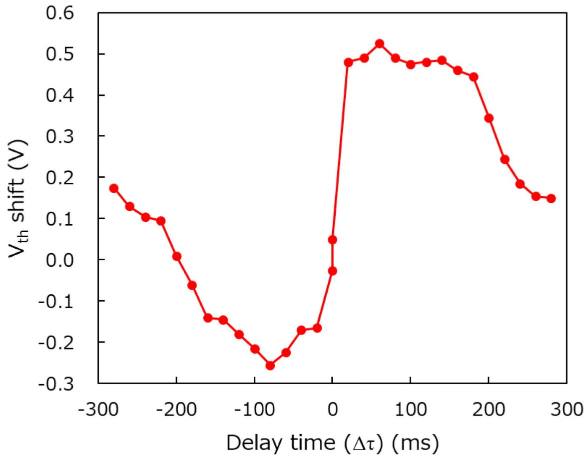

FIGURE 11. Effect of delay time on the V_{th} shift with the pulse setup shown in Fig. 10.

used for the measurement of STDP characteristics. A significantly positive voltage ($>V_{critical}$), which could affect V_{th}, was applied to the SiN layer by the composite pulse when the delay was positive. By contrast, a significantly negative voltage ($< -V_{critical}$) was applied to the SiN layer by the composite pulse when the delay was negative. The polarity of the voltage applied to the SiN layer depended on the direction of the delay. In addition, the time applied to the significant positive and negative voltages also depends on the delay. Therefore, we can implement asymmetric STDP characteristics of biological synapses with bipolar pulses. In the fabricated memory device, $V_{critical}$ was 4 V according to the programming characteristics presented in Fig. 7. Therefore, we determined that both V_{pg} and V_{ps} were 3.5 V. V_{pg} and V_{ps} denote the amplifier of the bipolar pulse applied to the gate and the drain, respectively. V_{pg} and V_{ps} cannot significantly affect V_{th} by themselves. However, when the delay is not zero, the composite pulse can sufficiently affect the V_{th} of the fabricated device owing to the high voltage of 7.0 V.

Fig. 11 shows the measurement results of the asymmetric STDP characteristics with both bipolar pulses. The source voltage was 0 V while applying the pre- and post-pulse signal. The pre- and post-pulse signals were applied to the gate and drain, respectively. These signals consisted of a bipolar pulse with 100 ms pulse width (τ_p). We achieved the asymmetric STDP characteristics, as shown in Fig. 6 (b), owing to the combination of the two simple bipolar pulses. These results indicate that the proposed non-volatile tunnel FET memory enables the implementation of SNN circuits. The realization of asymmetric STDP characteristics has been attempted with various memories. However, in many memories, the weights diverge near zero delay, [3], [21]–[23]. In actual biological synapses, the weight near zero delay is zero according to the Heb rule. The memory device developed in this study can imitate biological synapses well. Therefore, they can help create an SNN that is closer to actual biological systems.

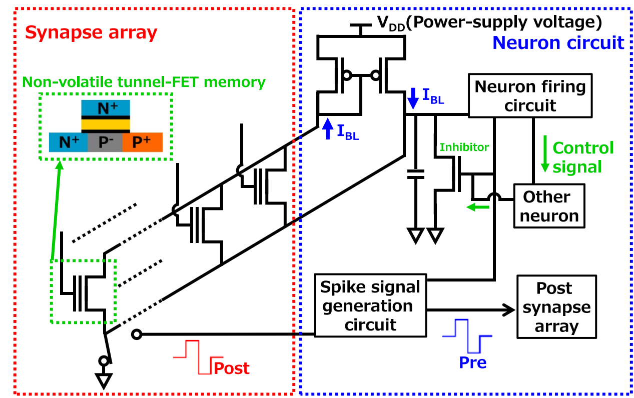

FIGURE 12. Target SNNs system with non-volatile tunnel-FET memories.

Furthermore, we are planning to develop an actual SNN, as shown in Fig. 12. This SNN consists of a synapse array and neuron circuits. In the synapse array, non-volatile tunnel-FET memories are arranged in an array. The result of the product sum operation using the weight factor saved in the memories is output to the neuron circuit. Then, the neuron firing circuit determines if the neurons will fire. Finally, to update the weight information, the spike generator sends post- and pre-signals to the previous and post synaptic arrays, respectively.

V. CONCLUSION

We fabricated and evaluated a non-volatile tunnel-FET memory with MONOS and tunnel-FET structure to enable the implementation of low-power NN circuits. The fabricated devices exhibited typical $I_d - V_g$ characteristics of a tunnel FET. Then, we demonstrated that the fabricated devices have the symmetric and asymmetric STDP characteristics of biological synapses. These results imply that the proposed memory device has the potential for implementing large-scale low-power SNN circuits. To enhance the performance of SNN circuits with non-volatile tunnel-FET memory, we consider that novel technologies such as heterojunctions [23], [24], two-dimensional materials [25], metal-nanodots flash memory [26], and three-dimensional integration [24], [27], are promising candidates. In the future, we plan to fabricate this SNN system with the non-volatile tunnel-FET memory developed in this study and other novel technologies.

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