Received 16 July 2020; revised 30 August 2020; accepted 6 September 2020. Date of publication 15 September 2020; date of current version 6 October 2020.
The review of this article was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2020.3023953

Low Ge Content Ultra-Thin Fin Width (5nm) Monocrystalline SiGe n-Type FinFET With Low Off State Leakage and High I_{ON}/I_{OFF} Ratio

CHONG-JHE SUN[1], MENG-JU TSAI[1] (Student Member, IEEE), SIAO-CHENG YAN[1], TZU-MING CHU[1], CHIENG-CHUNG HSU[1], CHUN-LIN CHU[2], GUANG-LI LUO[2], AND YUNG-CHUN WU[1] (Member, IEEE)

1 Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300, Taiwan
2 National Applied Research Laboratories, Taiwan Semiconductor Research Institute, Hsinchu 300, Taiwan

CORRESPONDING AUTHOR: Y.-C. WU (e-mail: ycwu@ess.nthu.edu.tw)

This work was supported in part by Ministry of Science and Technology, Taiwan, under Contract MOST 109-2221-E-007-031-MY3, and in part by Taiwan Semiconductor Research Institute, Taiwan.

ABSTRACT We successfully fabricate the $Si_{0.8}Ge_{0.2}$ channel fin field-effect-transistor (FinFET) with 5 nm ultra-thin fin width and high aspect ratio ($\sim 10\times$) on silicon-on-insulator (SOI) substrate by simple two-step dry etching. In comparison of the conventional Si FinFET, our proposed SiGe ultra-thin FinFETs ($Si_{0.8}Ge_{0.2}$ UT-FinFET) at $V_D = 0.75$ V & $V_G = 1.5$ V shows higher ON-state current (1 mA/fin), even achieve lower OFF-state current (0.2 nA/fin) and steep subthreshold slope (SS) of 76 mV/decade, which is owing to the better gate control given by the ultra-thin fin channel. In addition, this work also exhibits the suppression of short channel effect (SCE) with very small drain induced barrier-lowering (DIBL) of 4 mV/V.

INDEX TERMS FinFET, SiGe, high mobility, ultra-thin fin, short channel effect.

I. INTRODUCTION

Recently, high mobility group IV materials such SiGe and Ge have been most promising candidates for improving complementary metal-oxide-semiconductor (CMOS) performance and compatible sub-5-nm Si fin field-effect transistor (FinFET) technology platform [1]–[4]. Although Ge is a promising channel material for integrating a Si CMOS because of its high electron, hole mobility and compatible process on current Si platforms, the intrinsic properties of Ge, such as lower bandgap (Eg = 0.66 eV) and larger relative permittivity ($\varepsilon r = 16.0$) than those of Si cause it suffering from high off-state current and inevitable short channel effects (SCEs) [5]–[8]. On the other hand, SiGe channel can provide better electrical advantages than Si in high carrier transport for both n-type and p-type field-effect transistor, high driving current [9], feasible V_{TH} adjustment, and superior negative-bias temperature instability [10]. Ge content in the $Si_{1-x}Ge_x$ channel plays a critical role in device performances. Low Ge mole fraction SiGe fin grown on a Si substrate can prevent additional SiGe alloy scattering [11] and still provide higher electron and hole mobility than can a Si fin [12]. Therefore, this study used an optimized Ge mole fraction 20% for $Si_{0.8}Ge_{0.2}$ fin [13]–[16] to achieve high FinFET performance.

Although the $Si_{0.8}Ge_{0.2}$ channel has advantages over the Si channel, its band gap, which is lower than that of Si, may degrade the FinFET performance. To resolve the SCE, FinFETs with Si ultra-thin fin (UT-fin) have superior electrostatics gate control have been studied [17]–[19]. Recently, a high selective etching process of SiGe by using dry etching is reported [20]. In this article, we fabricated an $Si_{0.8}Ge_{0.2}$ UT-FinFET by using high selective dry etching to trim the Fin down to UT (5 nm) with a high aspect ratio FinFET, and study the high-performance electrical properties of $Si_{0.8}Ge_{0.2}$ UT-FinFET. In addition, the standard Si FinFET is fabricated for comparison.

II. DEVICE FABRICATION

The n-type SiGe and Si FinFETs were fabricated on p-type 8-inch Si on insulator (SOI) wafers. For SiGe FinFET, the

monocrystalline Si layer of SOI wafer was first thinned down to 20 nm, and then a 40 nm SiGe with 20% Ge content ($Si_{0.8}Ge_{0.2}$) was epitaxially grown by using ultra-high-vacuum chemical molecular epitaxy (UHVCME) system. Next, the active region was defined by e-beam lithography (EBL) and photoresist trimming for all the devices. By using reactive ion etching (RIE) the fin shape channel was then formed. Fig. 1 (b) and (c) show the sketches of different etching scheme between $Si_{0.8}Ge_{0.2}$ and Si devices. The $Si_{0.8}Ge_{0.2}$ devices etching process was achieved through two steps, (i) the anisotropic etching etches the fin vertically into a thick fin shape, and (ii) side fin trimming thin the SiGe part of active region down to UT-Fin. During the second step, the high etching rate difference between Si, SiGe and the hard mask protection result in the side etching that trimmed the SiGe into UT and remain the height at the same time [20]. In fact, the two different etched fin shapes are achieved with same RIE recipe and intentional over-etching. The only difference that result in the two different fin shape is the different etching rate. Self-Align Double Patterning (SADP) is needless in this experiment to fabricate such a thin fin channel.

After RCA cleaning, the gate stacks of SiO_2/HZO/TiN were formed. First, an 1-nm-thick chemical oxide interfacial layer (IL) was formed by H_2O_2 solution dipping at 75°C. Then a 5-nm-thick HZO was deposited by atomic layer deposition (ALD) as the high-k dielectric layer. Afterwards, a 80-nm-thick TiN film was deposited on the HZO dielectric layer as the gate metal. Consequently, the gate region was defined by using EBL, and the gate length was patterned from 80 nm to 500 nm by RIE. Following the gate defining, self-aligned ion implantation with 1×10^{15} cm^{-2} dosage, 10 keV phosphorous was implemented for source/drain doping. Since the Fins of SiGe devices are constructed with SiGe top and the underlying Si, for avoiding the Si bottom to contribute the electron pathway, the designed implantation energy of 10 keV ensures the phosphorous ions located on $Si_{0.8}Ge_{0.2}$ active layer. In the final step, the dopant is activated by using rapid thermal annealing (RTA) at 500°C for 30 secs in N_2 ambient. A low Dit SiGe device can be produced by using common IL/HK/WFM gate stack [21]. Interface may be degraded as the Ge content increases; and Dit is related to the temperature during the following process. Thus we choose a low Ge content SiGe (20% Ge) to be the active material and lower the RTA temperature (500°C) for decreasing the interface sate density.

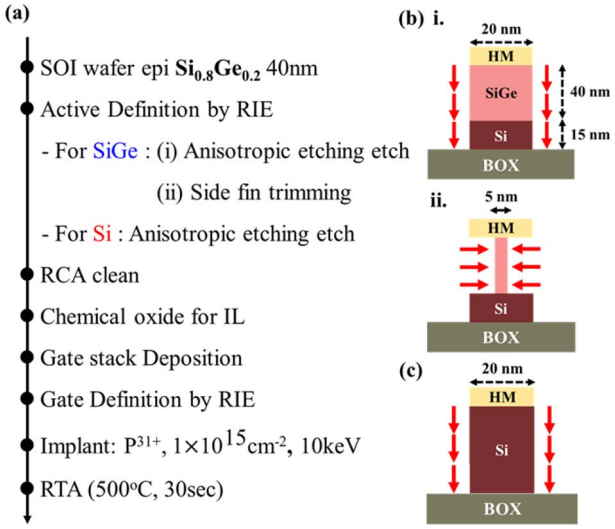

FIGURE 1. **(a) Devices process flow and the schematic flow of fin formation etching. (b) (i) anisotropic etching trim the SiGe active region down to a thick fin shape. (ii) the side etching thin the SiGe into UT-Fin (c) etching scheme of Si Fin.**

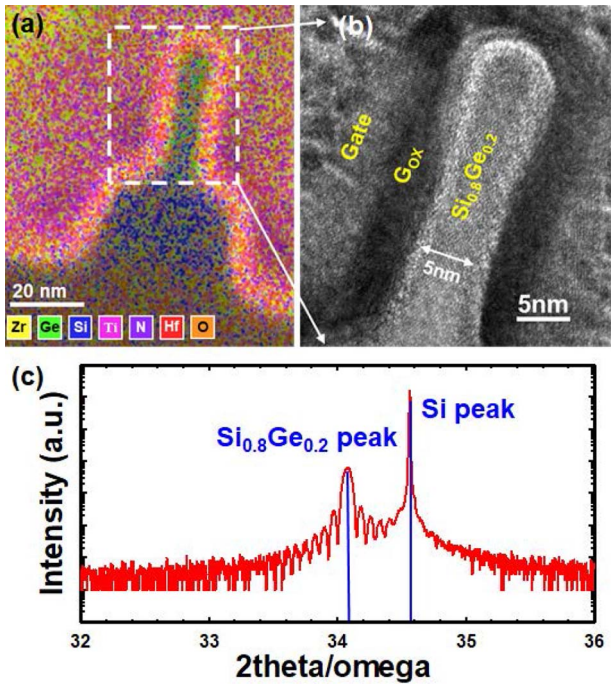

FIGURE 2. **(a) EDS-mapping of SiGe fin. (b) High resolution cross sectional TEM of SiGe fin with W_{fin} = 5 nm shows monocrystalline $Si_{0.8}Ge_{0.2}$. (c) XRD of active layer show 20% Ge content.**

III. RESULTS AND DISCUSSION

As evident in Fig. 2 (a), the cross-sectional transmission electron microscopy (TEM) image energy dispersive spectroscopy (EDS) mapping of element distribution revealed the structural materials of the $Si_{0.8}Ge_{0.2}$ UT-fin FinFET. The materials of the thin fin part are a compound of Si and Ge, and Si is used as the thick bottom base. The TEM image in Fig. 2(b) illustrates a close-up enlargement of monocrystalline $Si_{0.8}Ge_{0.2}$ UT-fin. It shows the $Si_{0.8}Ge_{0.2}$ region is well crystallized and the thin fin channel is indeed trimmed down to have channel width only 5 nm thick. Fig. 2(c) shows the XRD of the active region. The two peaks in the plot indicate that the active region is formed by two monocrystalline materials one is Si beneath and the other one is the epitaxial SiGeactive layer. Moreover, the peak position tells the Ge content of SiGe layer is about 20%.

Fig. 3 shows the $I_D - V_G$ characteristics of two FinFET devices: (i) a conventional Si FinFET with 20 nm fin width and (ii) $Si_{0.8}Ge_{0.2}$ UT-FinFET with 5 nm fin width. I_D is normalized by TEM image fin width (W_{fin}) over gate length, and the V_{TH} is extracted at $I_D = 1 \times 10^{-7}$(A) as $V_D =$ 50 mV. Both of the two FinFETs achieve good subthreshold swing: 74 mV/dec for the Si FinFET and 76 mV/dec for the $Si_{0.8}Ge_{0.2}$ UT-FinFET, which implies that the interface trap density of $Si_{0.8}Ge_{0.2}$ UT-FinFET is well suppressed. Note that, there is an obvious V_{TH} right shift (~0.3 V) for the $Si_{0.8}Ge_{0.2}$ UT-FinFET compares to Si FinFET. Because the flat band voltage (V_{FB}) can be expressed as:

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{1}$$

$$\phi_{ms} = \phi_m' - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right) \tag{2}$$

where ϕ_{ms} is the work function difference between metal and semiconductor, ϕ_m' and χ' are the modified metal work function and electron affinity which are modified to the oxide conduction band, and the potential ϕ_{fp} is the difference between E_{Fi} and E_F. Since the identical TiN gate metal and the high-k oxide layer HZO are used for the two different devices, the energy band gap difference between Si and $Si_{0.8}Ge_{0.2}$ is about 0.14eV, and the electron affinity difference is negligible, from the equation (1) and (2), it is only 0.07V V_{FB} difference which attribute to different materials used for two devices. As a result, the 0.3V V_{TH} shift for the $Si_{0.8}Ge_{0.2}$ UT-FinFET is mostly due to the Quantum confinement effect (QCE) which is invoked as the fin channel has only 5 nm width [22]. Since the dimension is smaller than electron matter wavelength in the channel (~7 nm), the conduction band acts as a quantum well, splits into several sub-bands, and decreases the electron density of state in the conduction band. Thus, it makes the Fermi-energy go upward which results in the increase of V_{FB} and the V_{TH} right shift. Furthermore, the scaled Fin width (5 nm) which is smaller than the electron matter wave length in the channel would invoke quantum confinement effect.

The experimental results also indicate that $Si_{0.8}Ge_{0.2}$ UT-FinFET has higher I_{ON} and lower I_{OFF} than that of the Si FinFET. Thus, $Si_{0.8}Ge_{0.2}$ UT-FinFET has a high on–off current ratio (I_{ON}/I_{OFF}) of approximately 2×10^7, which is more than one order of magnitude larger than the conventional Si FinFET. As shown in Fig. 4, the effective mobility comparison between $Si_{0.8}Ge_{0.2}$ UT-FinFET and Si FinFET reveals that the high I_{ON} of the $Si_{0.8}Ge_{0.2}$ FinFET is owing to the higher carrier mobility of $Si_{0.8}Ge_{0.2}$ than that of Si. As the channel fin is ultra-thin, a better gate control is expected to suppress off-state current. In addition, due to the QCE the energy band gap of the $Si_{0.8}Ge_{0.2}$ channel would be widened. Due to the improved gate control and band gap widening by QCE, the I_{OFF} of the $Si_{0.8}Ge_{0.2}$ UT-FinFET was effectively decreased.

Fig. 4 shows the electron effective mobility as a function of inversion carrier density (N_{inv}) which is extracted from

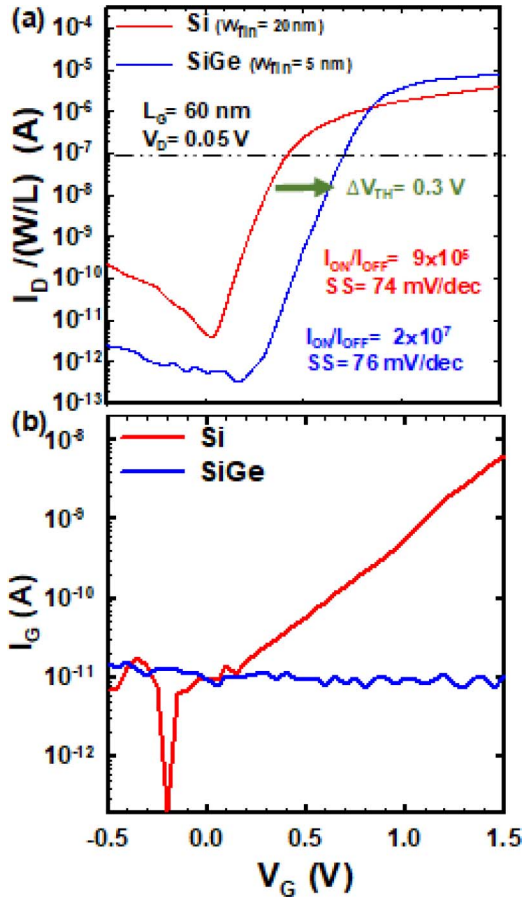

FIGURE 3. (a) $I_D - V_G$ plot of Si FinFET (V_{TH} = 0.4V) and high Ion/Ioff ratio $Si_{0.8}Ge_{0.2}$ (V_{TH} = 0.7V) UT-FinFET with L_G = 60 nm at V_D = 0.05 V. $Si_{0.8}Ge_{0.2}$ UT-FinFET has higher Vth due to QCE. (b) $I_G - V_G$ plot for the devices on Fig. 3(a).

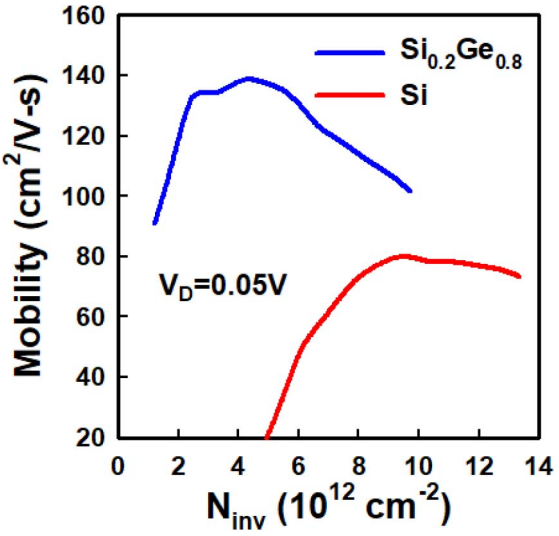

FIGURE 4. Effective mobility to inversion carrier density of Si FinFET and $Si_{0.8}Ge_{0.2}$ UT-FinFET extracted with data in Fig. 3.

equation (3) to (6). The peak mobility values of $Si_{0.8}Ge_{0.2}$ UT-FinFET and Si FinFET are 138 and 80 (cm^2/V-s) respectively. It suggests that the higher I_{ON} of $Si_{0.8}Ge_{0.2}$

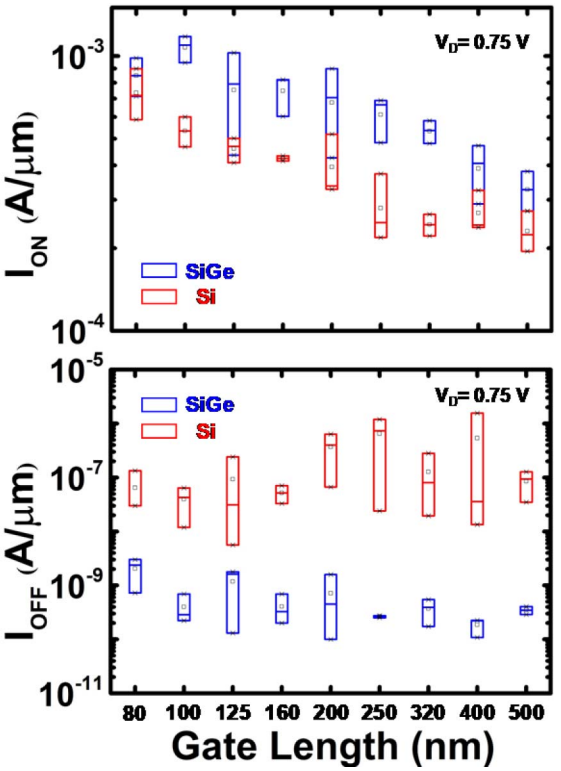

FIGURE 5. (a) I_{ON} comparison and (b) I_{OFF} comparison between Si FinFET and SiGe UT-FinFET with log scale gate length vary from 80 nm to 500 nm at $V_D = 0.75V$.

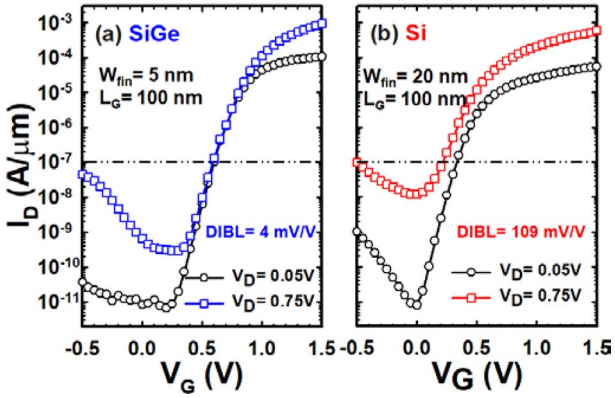

FIGURE 6. $I_D - V_G$ plots of (a) $Si_{0.8}Ge_{0.2}$ UT-FinFET and (b) Si FinFET with $L_G = 100$ nm at $V_D = 0.05$ V and 0.75 V. DIBL with Vth were extracted at $I_D = 1 \times 10^{-7}$ (A/μm).

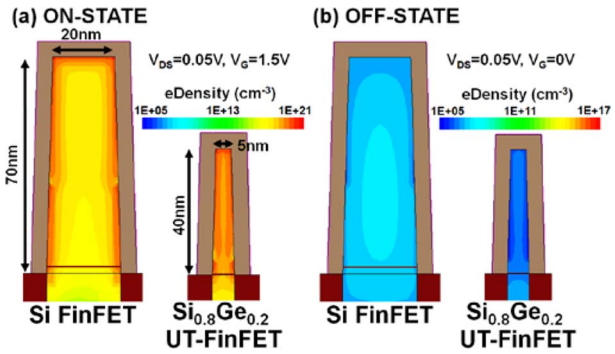

FIGURE 7. 3D TCAD simulation of electron density in fin channel at (a) OFF-state., and (b) ON-state.

UT-FinFET in Fig. 3(a) is attributed to the about 1.7 times higher electron peak mobility. The mobility peak value of $Si_{0.8}Ge_{0.2}$ UT-FinFET shows left shift of N_{inv}, comparing to Si FinFET, where $N_{inv} = C_{HK}(V_{GS} - V_{TH})/e$ at very low V_{DS}. This effect can also be explained by V_{TH} shift in Fig. 3a.

$$I_D = \frac{W\mu C_{OX}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad (3)$$

$$\mu = \left(\frac{2L}{W}\right)\frac{I_D}{C_{OX}}\left[\frac{1}{2(V_{GS} - V_T)V_{DS} - V_{DS}^2}\right] \quad (4)$$

$$Q_{inv} = C_{ox} \times (V_G - V_T) \quad (5)$$

$$N_{inv} = \frac{Q_{inv}}{e} = \frac{C_{ox}}{e} \times (V_G - V_T) \quad (6)$$

For a more complete comparison of I_{ON} and I_{OFF} between the devices. The statistical data of I_{ON} and I_{OFF} regarding L_G at $V_D = 0.75$ V were studied. Fig. 5 (a) introduces that an approximately 1.5× improvement of I_{ON} for the $Si_{0.8}Ge_{0.2}$ UT-FinFET compared with that of the Si FinFET. This higher driving current is attributed to the higher carrier mobility of $Si_{0.8}Ge_{0.2}$. Nevertheless, the I_{OFF} comparison in Fig. 5 (b) indicates that I_{OFF} was suppressed by approximately 2 orders by using the $Si_{0.8}Ge_{0.2}$ UT-FinFET because of the excellent gate control ability and QCE. The statistics clarified that these conclusions apply to the full range of L_G in this experiment. Consequently, $I_D - V_G$ characteristics with different V_D (0.05 and 0.75 V) of the $Si_{0.8}Ge_{0.2}$ UT-FinFET and Si FinFET were plotted in Fig. 6 (a) and (b), respectively. Both devices are with $L_G = 100$ nm. A nearly drain induced barrier-lowering (DIBL)-free (4 mV/V) result was observed for the $Si_{0.8}Ge_{0.2}$ UT-FinFET because the UT fin caused the gate to suppress the SCE efficiently. In addition, since the UT fin make the dopant in the S/D harder to diffuse into the channel region, the effective channel length of $Si_{0.8}Ge_{0.2}$ UT-FinFET is thus longer than that of Si FinFET. Notably, because the UT fin reduced the electric field gradient in a direction perpendicular to the channel and thus lessened energy band bending, the $I_D - V_{=G}$ curves of the $Si_{0.8}Ge_{0.2}$ UT-FinFET in Figs. 3(a) and 6 both revealed a smaller gate-induced drain leakage (GIDL) than did the Si FinFET. The $I_G - V_G$ plot in Fig. 3(b) also implies the low off current for $Si_{0.8}Ge_{0.2}$ UT-FinFET is not attributed to higher leakage current to the gate but due to the small GIDL.

To understand devices physical characteristics, the Synopsys Sentaurus 3D technology computer-aided design (TCAD) simulation [23] is used. The simulation structure was defined to fit the experimental data. Fig. 7 (a) and (b) presents the electron density distribution in the fin channel of the two FinFETs during operation ($V_{DS} = 0.05$ V, $V_G = 1.5$ V) and in the off state ($V_{DS} = 0.05$ V, $V_G = 0$ V),

respectively. The $Si_{0.8}Ge_{0.2}$ UT-FinFET shows higher electron density distributed in the fin channel in the on state. In the off state, the $Si_{0.8}Ge_{0.2}$ UT-FinFET exhibited low electron density in its channel, which resulted in a lower leakage than the Si FinFET.

IV. CONCLUSION

In this study, the $Si_{0.8}Ge_{0.2}$ UT-FinFET with only 5 nm W_{fin} was well fabricated by using simple two-step dry etching. The electrical properties of $Si_{0.8}Ge_{0.2}$ UT-FinFET has been demonstrated. An enhancement on I_{ON} and suppression on I_{OFF} are effectively achieved simultaneously by using high mobility material and ultra-thin fin structure. A high I_{ON}/I_{OFF} ratio of $\sim 2 \times 10^7$ and SS $= 76$ mV/dec are proposed. Meanwhile, the SCE can be highly reduced as the nearly DIBL-free characteristic shown in $I_D - V_G$ measurement. Furthermore, the 3D TCAD simulation also confirms the electron density in channel during on state and off state.

REFERENCES

[1] H. Arimura *et al.*, "Ge nFET with high electron mobility and superior PBTI reliability enabled by monolayer-Si surface passivation and La-induced interface dipole formation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2015, pp. 21.6.1–21.6.4, doi: 10.1109/IEDM.2015.7409752.

[2] H. Mertens *et al.*, "Si-cap-free SiGe p-channel FinFETs and gate-all-around transistors in a replacement metal gate process: Interface trap density reduction and performance improvement by high-pressure deuterium anneal," in *Proc. Symp. VLSI Technol. (VLSI Technol.)*, Jun. 2015, pp. T142–T143, doi: 10.1109/VLSIT.2015.7223654.

[3] Apoorva, N. Kumar, S. I. Amin, and S. Anand, "Design and performance optimization of novel Core–Shell dopingless GAA-nanotube TFET with Si0.5Ge0.5-based source," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 789–795, Mar. 2020, doi: 10.1109/TED.2020.2965244.

[4] Q. Zhao *et al.*, "Strained Si and SiGe nanowire tunnel FETs for logic and analog applications," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 103–114, May 2015, doi: 10.1109/JEDS.2015.2400371.

[5] W. Chang, H. Ota, and T. Maeda, "Gate-first high-performance germanium nMOSFET and pMOSFET using low thermal budget ion implantation after germanidation technique," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 253–256, Mar. 2016, doi: 10.1109/LED.2016.2523518.

[6] M. J. H. van Dal *et al.*, "Ge CMOS gate stack and contact development for vertically stacked lateral nanowire FETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2018, pp. 21.1.1–21.1.4, doi: 10.1109/IEDM.2018.8614577.

[7] A. Ritenour, J. Hennessy, and D. A. Antoniadis, "Investigation of carrier transport in germanium MOSFETs with WN/Al_2O_3/AlN gate stacks," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 746–749, Aug. 2007, doi: 10.1109/LED.2007.901272.

[8] C. Chu *et al.*, "Stacked Ge-nanosheet GAAFETs fabricated by Ge/Si multilayer epitaxy," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1133–1136, Aug. 2018, doi: 10.1109/LED.2018.2850366.

[9] K. Seo *et al.*, "A 10nm platform technology for low power and high performance application featuring FINFET devices with multi work-function gate stack on bulk and SOI," in *Proc. Symp. VLSI Technol.*, Jun. 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894342.

[10] D. Guo *et al.*, "FINFET technology featuring high mobility SiGe channel for 10nm and beyond," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573360.

[11] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2252, 1996, doi: 10.1063/1.363052.

[12] C. Jeong *et al.*, "Physical understanding of alloy scattering in SiGe channel for high-performance strained pFETs," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2013, pp. 12.2.1–12.2.4, doi: 10.1109/IEDM.2013.6724614.

[13] T. Lee, K. Kato, M. Ke, M. Takenaka, and S. Takagi, "Improvement of SiGe MOS interface properties with a wide range of Ge contents by using TiN/Y2O3 gate stacks with TMA nassivation," in *Proc. Symp. VLSI Technol.*, Jun. 2019, pp. T100–T101, doi: 10.23919/VLSIT.2019.8776523.

[14] C. H. Lee *et al.*, "A comparative study of strain and Ge content in Si1-xGex channel using planar FETs, FinFETs, and strained relaxed buffer layer FinFETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 37.2.1–37.2.4, doi: 10.1109/IEDM.2017.8268509.

[15] C. H. Lee *et al.*, "Toward high performance SiGe channel CMOS: Design of high electron mobility in SiGe nFinFETs outperforming Si," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2018, pp. 35.1.1–35.1.4, doi: 10.1109/IEDM.2018.8614581.

[16] G. Tsutsui *et al.*, "Leakage aware Si/SiGe CMOS FinFET for low power applications," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 87–88, doi: 10.1109/VLSIT.2018.8510639.

[17] M. J. H. van Dal *et al.*, "Highly manufacturable FinFETs with sub-10nm fin width and high aspect ratio fabricated with immersion lithography," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2007, pp. 110–111, doi: 10.1109/VLSIT.2007.4339747.

[18] J. Kavalieros *et al.*, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," in *Proc. Symp. VLSI Technol.*, Jun. 2006, pp. 50–51, doi: 10.1109/VLSIT.2006.1705211.

[19] T. Liow *et al.*, "Strained N-channel FinFETs with 25 nm gate length and silicon-carbon source/drain regions for performance enhancement," in *Proc. Symp. VLSI Technol.*, Jun. 2006, pp. 56–57, doi: 10.1109/VLSIT.2006.1705214.

[20] Y. Ishii, Y. Lee, W. Wu, K. Maeda, H. Ishimura, and M. Miura, "Etch control and SiGe surface composition modulation by low temperature plasma process for Si/SiGe dual channel fin application," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1277–1283, 2019, doi: 10.1109/JEDS.2019.2951360.

[21] D. Bae *et al.*, "A novel tensile Si (n) and compressive SiGe (p) dual-channel CMOS FinFET co-integration scheme for 5nm logic applications and beyond," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2016, pp. 28.1.1–28.1.4, doi: 10.1109/IEDM.2016.7838496.

[22] H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental evidence for quantum mechanical narrow channel effect in ultra-narrow MOSFET's," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 396–398, Aug. 2000, doi: 10.1109/55.852962.

[23] *Sentaurus TCAD Version 2016*, Synopsys, Mountain View, CA, USA, 2016.