Received 26 March 2020; revised 26 May 2020 and 6 August 2020; accepted 6 September 2020. Date of publication 15 September 2020; date of current version 6 October 2020. The review of this article was arranged by Editor M. Liu.

Digital Object Identifier 10.1109/JEDS.2020.3024235

Hydrogen Source and Diffusion Path for Poly-Si Channel Passivation in Xtacking 3D NAND Flash Memory

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This work was supported in part by the National Key Research and Development Program of China under Grant 2018YFB1107700, and in part by the National Science and Technology Major Project of China under Grant 2017ZX02301002.

ABSTRACT Poly-Si channels need well passivated by using hydrogen passivation process in 3D NAND flash memories for better poly-Si quality with low trap density. It is believed that Xtacking 3D NAND flash memory has the advantage of flexible arranging the passivation process. In this article, two different passivation locations were compared in Xtacking structure to achieve better trap passivation. An optimized passivation process conducted at wafer backside with passivation SiN as hydrogen diffusion source was found to have an improved trap passivation result. This benefit was attributed to the sufficient H diffusion paths in Xtacking. These results also indicated the advantage of trap passivation for future higher stacked Xtacking 3D NAND flash memory.

INDEX TERMS Xtacking 3D NAND flash memory, polycrystalline silicon, hydrogen passivation process, hydrogen source, trap passivation.

I. INTRODUCTION

In 3D NAND flash memory, vertical channel relying on poly silicon is the most commonly accepted solution for high density storage [1]–[4]. However, poly-Si contains high density of dangling bonds (DBs) at both grain boundaries and tunnel oxide/poly-Si interface. These DBs act as carrier traps and lead to the degradation on both cell performance [5]–[7] and reliability [8]. For this reason, in 3D NAND fabrication, a passivation process is necessary to remove these traps by using hydrogen species (H) [9]–[10].

However, CMOS devices require much less H than cell devices due to the reliability concerns, such as TDDB and HCI degradation [11]–[12]. In Xtacking, the variety of practicable passivation positions can be considered, such as the BEOL side of array and/or CMOS, and their backside as well. Therefore, it is believed the Xtacking structure has the benefit of flexible supply of H that can help reconcile array poly-Si trap passivation and providing less H for CMOS devices.

Hydrogenated SiN deposited by plasma enhanced chemical vapor deposition (PECVD) is regarded as one of the most efficient hydrogen source because of its high H content [13]–[14]. When SiN is annealed at a temperature higher than 400°C, H can be released from Si-H and N-H bonds and diffuse to DBs. Our previous research has successfully shown the advantage of PECVD SiN on poly-Si trap passivation in the conventional 3D NAND [15]. In this article, schemes by arranging the passivation process at different locations with PECVD SiN were investigated in the Xtacking 3D NAND structure. The optimized condition for the improvement of SS characteristics was proposed. H diffusion paths in both structures were further demonstrated, especially in Xtacking.

II. EXPERIMENTS

Xtacking samples with the structure shown in Fig. 1 (b) were prepared by bonding array to CMOS. Array was fabricated following a 3D NAND array process with array BEOL on each array wafer. Top metal was formed on the backside of

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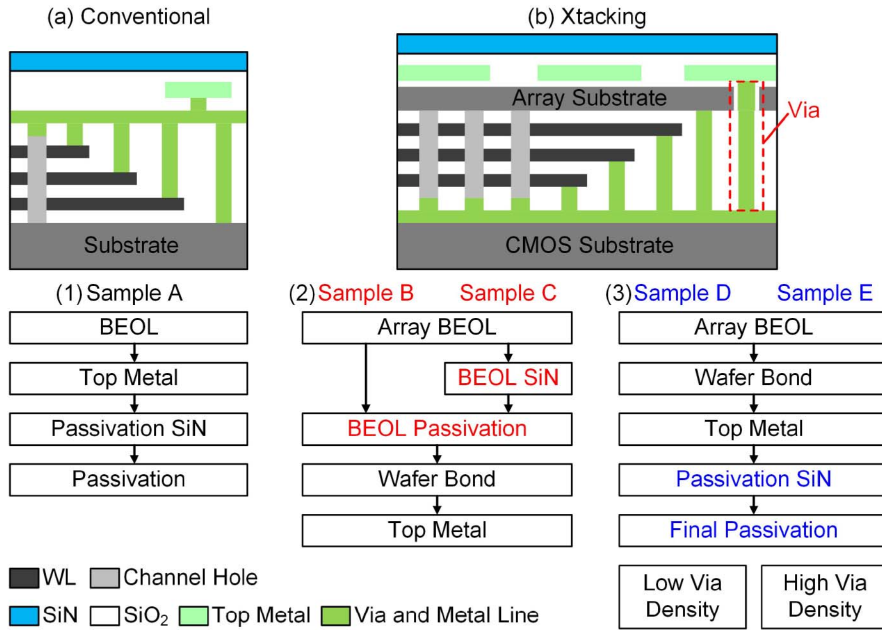

FIGURE 1. Schematic diagrams of (a) conventional and (b) Xtacking 3D NAND structures where CMOS is not shown, and corresponding samples: (1) Sample A following conventional flow, (2) Sample B and C following Xtacking flow with only BEOL passivation, and (3) Sample D and E following Xtacking flow with only final passivation.

array wafer after wafer bonding, and was connected to the circuit through metal via. Different locations of passivation process were investigated. Xtacking sample B and sample C were passivated only at the BEOL side before wafer bonding, shown in Fig. 1 (2). Sample C had a BEOL SiN as the H diffusion source. Xtacking sample D and sample E with different via density were passivated at wafer backside after wafer bonding, shown in Fig. 1 (3).

Conventional sample A as the control group was also prepared based on only array wafer which is the same as that of Xtacking samples, shown in Fig. 1 (a). Passivation SiN was deposited after the formation of interconnections and top metal. The passivation process was then conducted, shown in Fig. 1 (1).

Cell performance was identified by subthreshold slope (SS) extracted from the Id-Vg curve for both structures, because SS is strongly associated with DBs and can reflect the passivation efficiency.

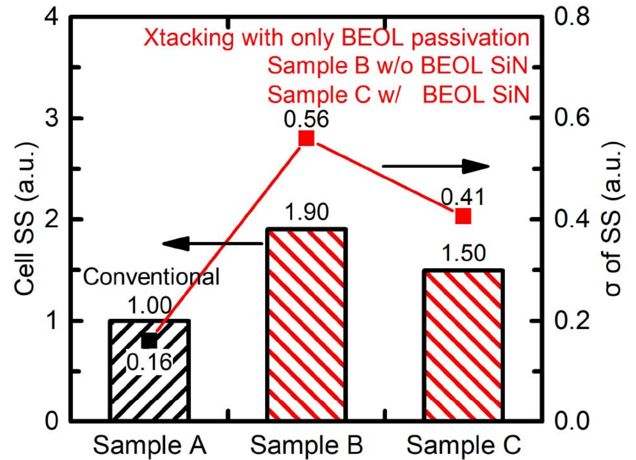

FIGURE 2. Comparison of cell SS (columns) and standard deviation s (dots) in samples with only BEOL passivation. Sample A was conventional as the control group. Sample B was only passivated in anneal ambience without an BEOL SiN as H source. Sample C was passivated with an BEOL SiN as H source.

III. RESULTS AND DISCUSSION

The conventional passivation process was originally conducted at the BEOL side in Xtacking sample B and sample C. However, sample B showed poor cell SS characteristic in Fig. 2 as compared to the conventional control group A under the same passivation condition. Even though a BEOL SiN was added as the efficient H source (sample C), cell SS was improved limitedly. This poor trap passivation indicated insufficient H was supplied to the poly-Si channels. The possible reason we consider is that the traps passivated by H can de-passivate during afterward processes containing thermal and plasma. In the first place, the Si-H bond is such a kind of weak bond that can be easily dissociated during subsequent high-temperature processes such as CVD [10]. Secondly, charging induced by plasma processes, such as plasma etch and PECVD, can also break Si-H bonds and induce defects. Therefore, it is difficult to passivate traps when supplying H at the BEOL side in Xtacking structure.

To avoid these extra thermal and plasma, the passivation process must be re-arranged to the end of the whole process flow. Array wafer backside is the most ideal position to conduct passivation process. For one reason, the effect caused

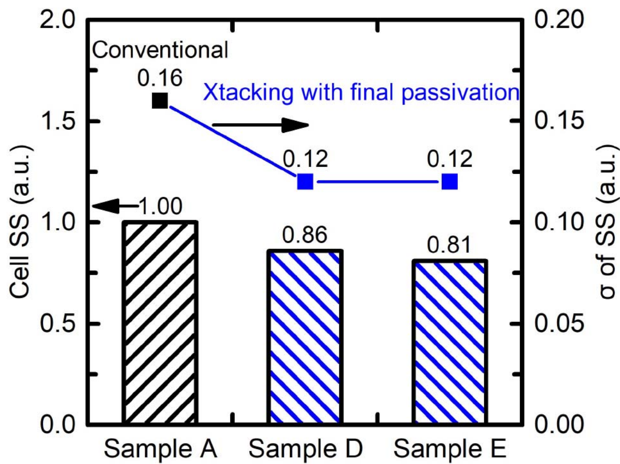

FIGURE 3. Comparison of cell SS (columns) and standard deviation σ (dots) in different structures. Sample A is the conventional sample with BEOL passivation as the control group. Sample D and sample E are Xtacking samples with final passivation but with different metal via densities.

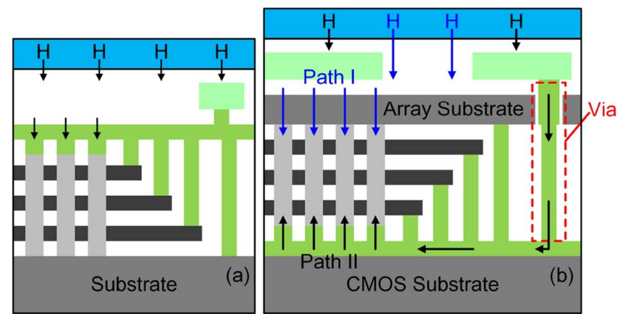

FIGURE 4. Schematic diagrams of H diffusion paths during final passivation in (a) conventional sample and (b) Xtacking samples. Path I represents for the H direct diffusion through the array Si substrate. Path II describes H diffusing along metal via and metal lines to channel holes.

by thermal and plasma processes on trap passivation can be diminished. For another, H source is much close to the cell array because the Si substrate is ground to only several microns. Furthermore, CMOS reliability should be better than that of conventional 3D NAND because the H source is far away from CMOS devices and is consumed by array poly-Si before arriving at CMOS.

Cell SS characteristics of the Xtacking samples and the conventional sample after respective passivation processes are compared in Fig. 3. A significant improvement on cell SS was observed in the Xtacking sample D compared with the conventional one (sample A), as well as an improved standard deviation σ. That the much improved amount of H was delivered to ploy-Si channels in the Xtacking structure should be reasonable. Moreover, no reliability degradation on CMOS devices was either observed through reliability test on sample D, not given in this article. Therefore, the passivation scheme of Xtacking has the benefit of providing better trap passivation efficiency than that of the conventional structure.

The reasonable explanation for this result is attributed to the H path. For the conventional sample, H can be only supplied at the BEOL side from passivation SiN, shown in Fig. 4 (a). Supplying H from the ambience at wafer backside is difficult in conventional structure. It is due to the limit on H_2 dissociation rate on Si surface. And the immobility of H_2 in Si also leads to the thick Si substrate impermeable [16].

But for Xtacking samples, H diffuses from both the substrate side and the BEOL side of the array wafer, shown in Fig. 4 (b). Firstly, H can directly diffuse through the Si substrate into ploy-Si channels, shown as Path I. For one reason, the Si substrate of the array wafer was ground to several microns. It makes H diffusion source much close to the array. Moreover, H has a good diffusion capability in crystalline Si [16]. The diffusion length in Si during final passivation was calculated to be much larger than the ground substrate thickness using the diffusion constant in the above reference. It infers that H can easily permeate through the array Si substrate. Furthermore, Si occupies the major area allowing abundant H to diffuse therein. Therefore, it is proposed that path I is the main H diffusion path.

Secondly, metal via and metal lines also allow H faster diffusion than in SiO_2, concluded from previous H diffusion studies [17]–[19], shown as Path II in Fig. 4 (b). H from the passivation SiN is prone to be adsorbed onto top metal, then diffuses along metal via to interconnections, and finally reaches ploy-Si channels. The interface of metal via and surrounding SiO_2 is regarded as a diffusion pipe allowing H faster transport than in bulk metals due to the lower activation energies [20]. Therefore, it is believed that there are sufficient diffusion paths in Xtacking structure to help H diffuse to ploy-Si channels. And the paths further lead to the improved passivation result and more uniform distribution throughout the wafer.

By-tier cell SS difference with varied passivation time was considered to characterize the H path. These samples were all Xtacking samples with final passivation processed in different passivation time. As is shown in Fig. 5, H accumulated in the beginning at the bottom of channels rather than at the top, because the lower WLs were passivated with a decreased cell SS earlier than the upper WLs. It infers that H accumulated at the bottom of channels comes from Path I. Afterwards, the upper WLs were passivated because H diffused to these cells from the channel bottom or from Path II.

To further improve trap passivation, the density of metal via was also investigated. The influence of via density on cell SS characteristic is also shown in Fig. 3 by comparing sample D with sample E. A slightly improved SS was observed in sample E with higher via density compared to sample D with low via density. It means that the metal via indeed helps supplement H and thus improves trap passivation meaning the diffusion along Path II. This supplementary effect may become important as array is stacked higher.

Since H can easily diffuse to poly-Si channels through Path I and Path II, it is reasonable to believe that our

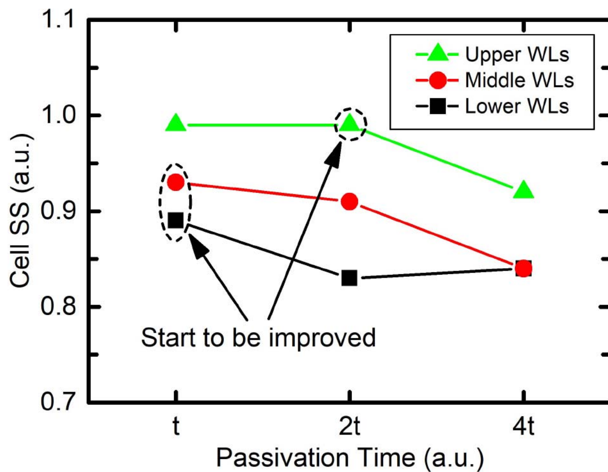

FIGURE 5. By-tier cell SS difference as a function of passivation time. The lower and upper WLs corresponds to the cells close to the Si substrate and interconnections, respectively.

passivation scheme can well passivate traps even in future higher stacked Xtacking 3D NAND as long as sufficient hydrogen atoms are delivered to the poly-Si channels. Also, for future applications of the passivation process in higher stacked Xtacking, the density of metal via may need fine tuning to improve poly-Si trap passivation.

IV. CONCLUSION

In this work, a limitation on trap passivation of conventional passivation scheme conducted at the BEOL side of array was observed in Xtacking 3D NAND flash memory. The afterward processes containing thermal and plasma were suspected. To achieve efficient trap passivation, the passivation scheme using passivation SiN deposited at wafer backside as the H diffusion source was investigated in the Xtacking structure. It achieved a better trap passivation result than that in the conventional sample. This benefit was attributed to the enhanced hydrogen diffusion by the sufficient diffusion paths existing in Xtacking structure. The direct H diffusion through the Si substrate (Path I) is theoretically calculated and experimented to be the main path. The metal via also works as a path (Path II) helping supplement H for passivation, which may become important in future generation Xtacking 3D NAND. Therefore, through our passivation scheme, it is believed that traps can be well passivated even if higher stacked array is used in future Xtacking 3D NAND as long as H delivery and via density are fine tuned.

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