Received 24 July 2020; revised 5 September 2020 and 7 September 2020; accepted 7 September 2020. Date of publication 14 September 2020; date of current version 4 November 2020. The review of this article was arranged by Editor J. Rajendran.

Digital Object Identifier 10.1109/JEDS.2020.3023803

Modeling of DC - AC NBTI Stress - Recovery Time Kinetics in P-Channel Planar Bulk and FDSOI MOSFETs and FinFETs

NILOTPAL CHOUDHURY (Graduate Student Member, IEEE), NARENDRA PARIHAR (Member, IEEE), NILESH GOEL (Member IEEE), A. THIRUNAVUKKARASU, AND SOUVIK MAHAPATRA (Fellow, IEEE)

Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India

CORRESPONDING AUTHOR: S. MAHAPATRA (e-mail: souvik@ee.iitb.ac.in)

ABSTRACT The physics-based BTI Analysis Tool (BAT) is used to model the time kinetics of threshold voltage shift (ΔV_T) during and after NBTI in p-channel planar bulk and FDSOI MOSFETs and SOI FinFETs. BAT uses uncorrelated contributions from the trap generation at the channel/gate insulator interface (ΔV_{IT}) and gate insulator bulk (ΔV_{OT}), and hole trapping in pre-existing gate insulator bulk traps (ΔV_{HT}). The ΔV_{IT} kinetics is simulated by the Reaction-Diffusion (RD) model. The empirical ΔV_{HT} model used earlier is now substituted by the Activated Barrier Double Well Thermionic (ABDWT) model. The ABDWT model is also used to verify the time constant of the electron capture induced fast ΔV_{IT} recovery. Empirical equations are used for ΔV_{OT}. The enhanced BAT modeling framework is validated using measured data from a wide range of experimental conditions and across different device architectures and gate insulator processes.

INDEX TERMS NBTI, BAT, RD model, ABDWT, TTOM.

I. INTRODUCTION

Negative Bias Temperature Instability (NBTI) remains as an important reliability issue in modern High-K Metal Gate (HKMG) technology based devices, such as planar bulk and Fully Depleted Silicon on Insulator (FDSOI) MOSFETs, bulk and SOI based FinFETs and Gate All Around Nanosheet (GAA NS) FETs [1]–[5]. NBTI impacts the PMOS device and results in a gradual accumulation of positive charges in gate insulator, when the gate is biased more negative compared to the other three terminals of the FET. The accumulated charges, in turn, lead to a gradual shift in various transistor parameters over time, and hence the performance of devices, circuits, and systems get degraded [6]. Interestingly, NBTI defects and the related device parametric shift partially recover if the stress is removed, and therefore, AC stress results in a lower parametric shift when compared to DC stress. Technology qualification depends on keeping the End-of-Life (EOL) degradation under acceptable limits. Hence, it is important to develop physics-based NBTI models, for accurate projection of EOL (e.g., at 10 years) parametric shift under use conditions, by using data from shorter-time accelerated stress experiments.

The physical mechanism responsible for NBTI has been a subject of many debates [7]–[11]. At present, there are mainly two competing viewpoints, the BTI Analysis Tool (BAT) [12] and the Compact Physical (Comphy) [13] model frameworks. Comphy models the measured ΔV_T stress-recovery kinetics by uncorrelated contributions from a recoverable (∼hole trapping-detrapping) and a semi-permanent (∼trap generation) parts that are modeled respectively by the Non-radiative Multi-Phonon and Two Well Thermionic models. The reader may refer to [13] and related papers for details of the Comphy framework and its capabilities.

BAT uses uncorrelated contributions from generated traps at the channel/gate insulator interface (ΔV_{IT}) and inside the gate insulator bulk (ΔV_{OT}), and hole trapping in pre-existing gate insulator traps (ΔV_{HT}), to model the kinetics of threshold voltage shift (ΔV_T) during NBTI stress [12]. The recovery of ΔV_T after NBTI stress is modeled using the recovery of ΔV_{IT} and ΔV_{HT}, since ΔV_{OT} shows negligible

recovery. The double interface Reaction-Diffusion (RD) model is used for the time kinetics of interface trap generation and passivation (density is DN_{IT}), and their contribution (ΔV_{IT}) due to charge occupancy is modeled by the Transient Trap Occupancy Model (TTOM). Empirical stretched-exponential equations are used for TTOM and ΔV_{HT} in [12], and ΔV_{HT} equations are replaced using the Activated Barrier Double Well Thermionic (ABDWT) model, first proposed in [14], in recent reports [15], [16]. The empirical model is used for ΔV_{OT} [12]. Therefore, ΔV_{IT} and ΔV_{HT} constitute the recoverable part and ΔV_{OT} determines the semi-permanent part of the BAT framework. The difference between BAT and Comphy is whether ΔV_{IT} constitutes the recoverable or semi-permanent part (ΔV_{IT} recovery is discussed later for BAT).

BAT has been used to model the ΔV_T time kinetics during and after both DC and AC stress at various stress bias (V_{GSTR}), recovery bias (V_{GREC}), temperature (T), duty cycle (PDC) and frequency (f), in Gate First (GF) HKMG planar p-MOSFETs having different Nitrogen (N%) content in the gate stack [12], in Replacement Metal Gate (RMG) HKMG SOI FinFET [17] and bulk Si, SiGe (Silicon Germanium) channel FinFETs with different Ge% in the channel and N% in the gate stack [18], [19]. BAT can model the layout dependence (distance between STI to active) in planar, and fin dimension (length and width) dependence in FinFETs [20]–[22]. Moreover, the macroscopic BAT framework can also model the mean of measured stress-recovery kinetics from multiple small area or few fin devices [23], [24]. The various capabilities of BAT are summarized in a recent review [25]. It has become evident from all the above reports that ΔV_{IT} contributes a significant fraction of ΔV_T for the range of V_{GSTR} and T used (see original references), while the other components can become important depending on the device type (more ΔV_{HT} for poor quality of the gate insulator) and stress condition (more ΔV_{OT} at high V_{GSTR} and T). Note, ΔV_{IT} dominates overall ΔV_T for the normal use condition of these devices. Further, a Technology CAD (TCAD) platform is enabled to calculate the ΔV_{IT} component during NBTI stress and validated using Si and SiGe p-FinFETs with various Ge%, N% and fin dimensions [26], [27].

In the above reports [12], [17]–[25], the ΔV_{HT} component is modeled using empirical stretched-exponential equations, with trapping and detrapping time constants (t_{HT} and t_{DT}) that vary with T for some devices, and variation in t_{DT} with stress time (τ_{STR}). Such variations can be manually done or modeled with empirical equations. However, ΔV_{HT} is modeled by ABDWT in [15], [16], and being a physical model it can automatically calculate the hole trapping and detrapping kinetics across all experimental conditions. Furthermore, the stochastic version of ABDWT can explain Random Telegraph Noise (RTN) and Time Dependent Defect Spectroscopy (TDDS) experiments as shown in [28].

This article presents a comprehensive overview of our recent conference reports [15], [16]. NBTI time kinetics is modeled using BAT with ABDWT for ΔV_{HT} and validated against a wide range of experimental data. Additionally, the electron capture time constant (τ_{EC}) associated with fast ΔV_{IT} recovery from TTOM is validated using ABDWT for various V_{GSTR} and T in this article. The device and measurement details are listed in Section II. The ABDWT enabled BAT framework is briefly explained in Section III. The model is validated with measured data in Section IV, and the paper is concluded in Section V.

II. DEVICE DETAILS AND MEASUREMENT DESCRIPTION

Experimental results are obtained from our earlier published reports. Keysight B1530 enabled with Waveform Generator/Fast Measuring Unit (WGFMU) is used for ultrafast electrical characterization. The Measure-Stress-Measure (MSM) scheme is used to measure the drain current drift in a logarithmic time interval and later translated to threshold voltage shift using the lateral shift method [29]. The measurement delay is kept close to ~10us to reduce the impact of the recovery-related artefacts. Three different types of devices are analyzed in this work: (1) GF HKMG planar devices with different gate stack processes resulting in lower (D1) and higher (D2) N%, (2) GF HKMG planar FDSOI devices, and (3) RMG SOI FinFETs, see [12], [17], [20], [21] for additional details.

III. MODEL DESCRIPTION

Fig. 1 illustrates the schematic of the BAT framework, while Fig. 2 shows the modeling of a typical ultra-fast measured ΔV_T stress-recovery kinetics using three uncorrelated components: ΔV_{IT}, ΔV_{HT}, and ΔV_{OT}. Note, the non-correlated nature of the subcomponents are verified in our earlier reports [12], [17]–[19], where they are shown to vary differently with changes in stress conditions (V_{GSTR} and T) and process changes (channel Ge% and gate oxide N%). As mentioned, the double-interface RD model is used for DN_{IT} and subsequently TTOM for ΔV_{IT}, ABDWT for ΔV_{HT} and empirical equations for ΔV_{OT}. The RD, TTOM and ΔV_{OT} model equations and parameters are listed in [12]. It is important to note that the adjustable parameters (4 for RD, 2 for TTOM and 1 for ΔV_{OT}) vary with processes, and are kept same as the original reports [12], [17]–[19], [21], [22]. This implies that the ΔV_{IT} and ΔV_{OT} subcomponents are the same between the earlier BAT and the current implementation, the empirical ΔV_{HT} equations are replaced by a physical ABDWT model in this work.[1] All process agnostic free parameters are listed in [12].

Fig. 3 illustrates the ABDWT model for ΔV_{HT} kinetics used in the enhanced BAT framework [15], [16]. It has two states E_1 (uncharged) and E_2 (charged) that are separated by a barrier (E_B). The mean (E_{B_mean}) and spread (E_{B_spread}) of the Gaussian barrier E_B are T activated, with

1. The worst-case difference in DVHT between the empirical and ABDWT models is ~5mV (typically ~2-3mV) for all cases studied in our work. The % error in modeling of overall ΔV_T is negligible between the two approaches (refer to results in the original references and this work).

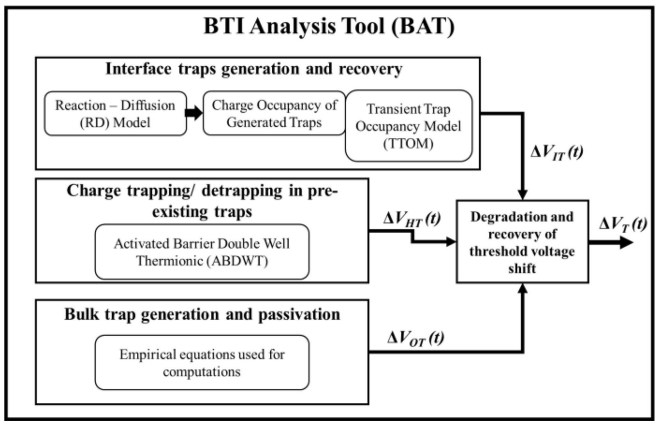

FIGURE 1. Schematic illustration of the BAT framework.

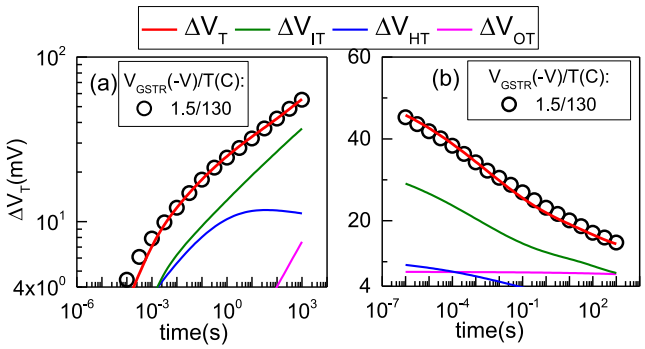

FIGURE 2. Time evolution of measured (symbols) and modeled (lines) ΔV_T at fixed V_{GSTR} and T for D1 device, along with the underlying subcomponents during (a) stress and (b) recovery.

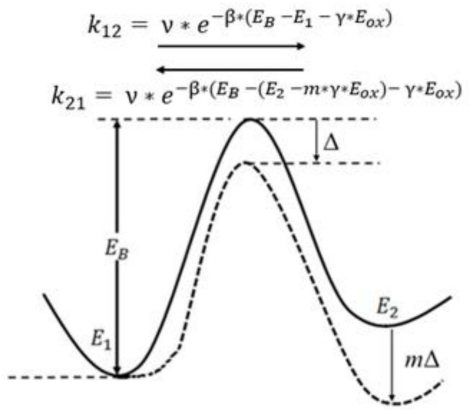

FIGURE 3. Schematic diagram of the ABDWT model with rate equations [15].

TABLE 1. List of parameters for the ABDWT model. (SOIFF is SOI FinFETs).

Parameters	ABDWT ΔV_{HT}				TTOM
	D1	*D2*	*SOIFF*	*FDSOI*	*SOIFF*
N_0 (/cm^2)	1.4E+12	4.0E+12	--	--	--
γ (C.cm)	4.6E-09	3.6E-09	5.7E-09	3.3E-09	6.0E-09
m (no unit)	3.2	3.5	2.4	3.2	4
$E_{B\ mean}$ (eV)	1.3				1.1
$E_{A\ mean}$ (eV)	0.0085				0
E_2 (eV)	0.21				0.18
$E_{B\ spread}$ (eV)	0.24				0.24
ν (/s)	1E+13				1E+13
$E_{A\ spread}$ (eV)	0.0055				0

energies E_{A_mean} and E_{A_spread} respectively. Note, the T activation is taken into consideration to account for the effects related to phonon coupling, and it is similar to the temperature-activated capture cross-section used in the conventional Shockley-Read-Hall (SRH) theory [30].

The application of V_{GSTR} (or electric field, E_{OX}) lowers the barrier E_B and state E_2 by Δ and m*Δ respectively (compared to E_1), where $\Delta = \gamma * E_{OX}$ and γ is the field acceleration factor. Thermionic emission occurs from E_1 to E_2 over the barrier E_B under the influence of the electric field during stress, which lowers the barrier E_B. The opposite happens during recovery after the end of stress. Considering the possible extraordinarily complex band bending scenarios inside the gate oxide due to spatially non-uniform trapped charges, the parameter m is kept as a fitting parameter. N_0 is the initial trap density and ν is the attempt frequency, $\beta = 1/kT$ where k is the Boltzmann constant. The ABDWT model has a total of nine parameters, only three of them are process dependent (see Table 1).

The RD model calculated trap generation (density DN_{IT} and contribution ΔV_{IT}) shows a long-time power-law slope of $n \sim 1/6$ during stress, Fig. 2. ΔV_{HT} saturates, while ΔV_{OT} shows a power-law slope of $n \sim 1/3$ at long t_{STR}. Note, the relative contribution from ΔV_{HT} is large at shorter t_{STR}, but it is not significant for longer t_{STR}. ΔV_{IT} recovery is due to fast electron capture that is handled by TTOM, and slower trap passivation by RD model. As before, empirical equations are used for TTOM, however, the time constant (τ_{EC}) is verified with ABDWT (see later). Moreover, ΔV_{HT} recovers fast while ΔV_{OT} is semi-permanent (negligible recovery). Note that the measurement delay plays an important role in measured ΔV_T. In samples with higher ΔV_{HT} contribution and very fast ΔV_{HT} recovery, the measured ΔV_T can be substantially lower than the "actual" ΔV_T from a hypothetical "no-delay" method. However, this is not an issue in production quality devices used in this work, as they feature good quality gate insulators and the contribution from ΔV_{HT} is indeed small.

IV. RESULTS AND DISCUSSIONS

A. DC STRESS KINETICS

Fig. 4 plots the measured and modeled ΔV_T time kinetics at various V_{GSTR} and T for (a) D1 and (b) D2 devices. Note that D2 has a higher N% in the gate stack compared to D1 devices. Therefore, the relative contribution of the ΔV_{HT} component on overall ΔV_T is higher in D2 devices due to the higher number of pre-existing defects, although ΔV_{IT} still dominates overall ΔV_T for both devices. The subcomponents are not explicitly shown here for brevity, refer to [12], [15] for additional details. This shows the ability of the ABDWT

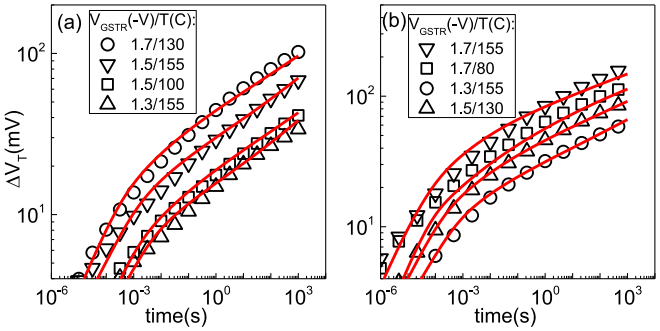

FIGURE 4. Time evolution of measured (symbols) and modeled (lines) ΔV_T during stress at various V_{GSTR} and T for (a) D1 and (b) D2 devices, from [15].

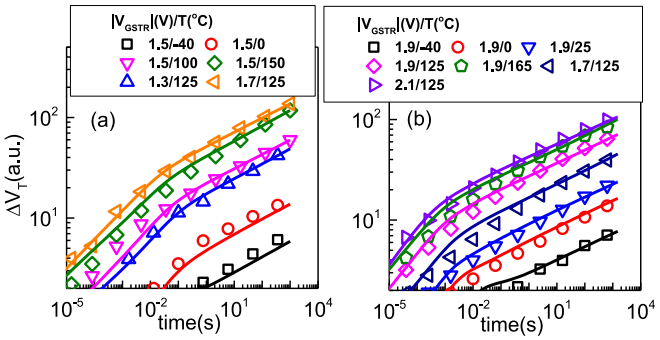

FIGURE 5. Time evolution of measured (symbols) and modeled (lines) ΔV_T during stress at various V_{GSTR} and T for (a) SOI FinFETs and (b) FDSOI devices, from [16].

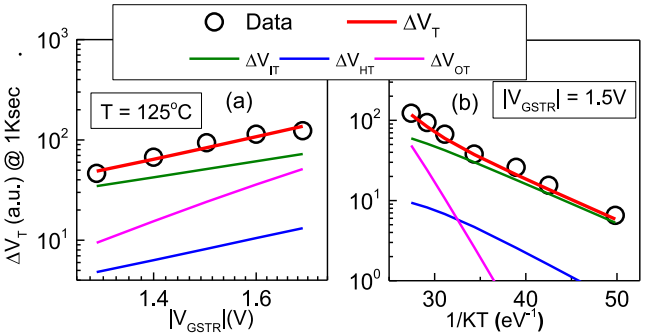

FIGURE 6. Fixed time measured (symbols) and modeled (lines) ΔV_T as a function of (a) V_{GSTR} at a fixed T, and as a function of (b) T at a fixed V_{GSTR} for SOI FinFETs, from [16]. The underlying subcomponents are also shown.

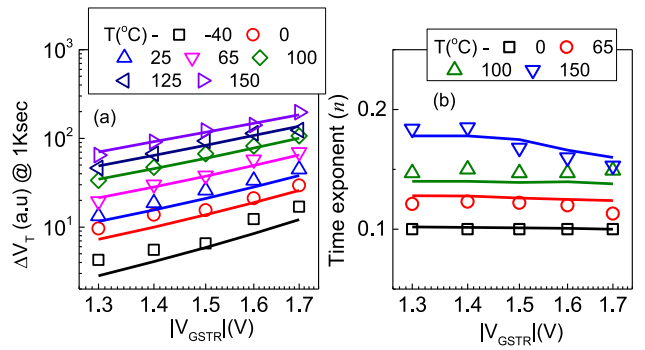

FIGURE 7. Measured (symbols) and modeled (lines) of (a) fixed time ΔV_T and (b) longer time slope *n* (1s-1Ks) as a function of V_{GSTR} over a range of T for SOI FinFETs, from [16].

enabled BAT framework to explain NBTI in devices with different N% in the gate stack.

Fig. 5 plots the measured and modeled ΔV_T time kinetics at various V_{GSTR} in (a) SOI FinFETs and (b) FDSOI MOSFETs over a wide range of T from −40°C to 150°C for SOI FinFETs and from −40°C to 165°C for FDSOI devices. As explained in [17], [21], although ΔV_{IT} dominates the overall ΔV_T across T, the relative contribution from ΔV_{HT} is higher at lower T, while ΔV_{OT} plays an important role at higher T, especially for higher V_{GSTR}. It is indeed possible that for very large V_{GSTR} at high T, the contribution from ΔV_{OT} can become more than ΔV_{IT}. This is further discussed hereinafter.

Fig. 6 plots the measured and modeled ΔV_T at fixed time as a function of (a) V_{GSTR} (at fixed T) and (b) T (at fixed V_{GSTR}) for SOI FinFETs. The underlying model components are also plotted. The V_{GSTR} and T dependencies of ΔV_{OT} is larger than the other components. This is expected as a generation of bulk oxide traps is also responsible for TDDB, which has high V_G acceleration and T activation. ΔV_{IT} dominates overall ΔV_T for the range of V_{GSTR} and T used in this study. As also mentioned above, ΔV_{OT} would indeed dominate ΔV_T at very high V_{GSTR} and/or T, however, ΔV_{IT} completely dominates overall ΔV_T at V_{GSTR} closer to the operating conditions. As explained in [19], the use of simpler empirical models can severely misestimate the extrapolated EOL ΔV_T at use condition, owing to different relative contributions of different components at different V_G.

Fig. 7 plots the measured and modeled (a) ΔV_T at fixed time and (b) longer time power-law slope *n* as a function of V_{GSTR} at different T for SOI FinFETs. BAT can model the measured time kinetics (see [17]) across V_{GSTR} x T, which is evidenced by the ability to model the ΔV_T magnitude and time slope, and also the variation in Voltage Acceleration Factor (VAF) across T. Note, VAF reduces at higher T in spite of having relatively larger contribution from ΔV_{OT}. This is attributed to the bond polarization effect [12], [17], which becomes even larger for the SiGe channel devices [18], [19]. The ability to model data across V_{GSTR} x T matrix is needed to reliably estimate longer time measurements closer to use condition [17].

B. DC RECOVERY KINETICS

Fig. 8 plots the measured and modeled time kinetics of ΔV_T after DC stress using (a, b) varying V_{GSTR} (but fixed T) and (c, d) varying T (but fixed V_{GSTR}), for V_{GREC} of (a, c) 0V and (b, d) –0.6V in device D1, the related stress kinetics are shown in Fig. 4. It is important to note that no parameters have been re-adjusted between stress and recovery to model such a wide range of recovery data, refer to [12], [15] for details.

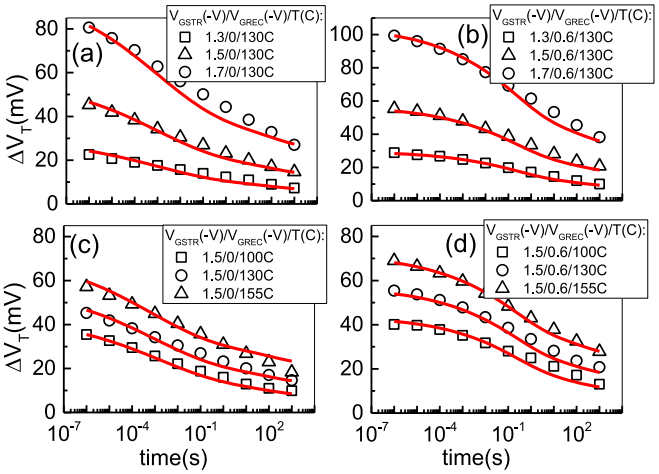

FIGURE 8. Time evolution of measured (symbols) and modeled (lines) recovery of ΔV_T after stress for 0V recovery bias (left panels) and for non-zero recovery bias (right panels), for (a, b) different V_{GSTR} and (c, d) different T. D1 devices are used, from [15].

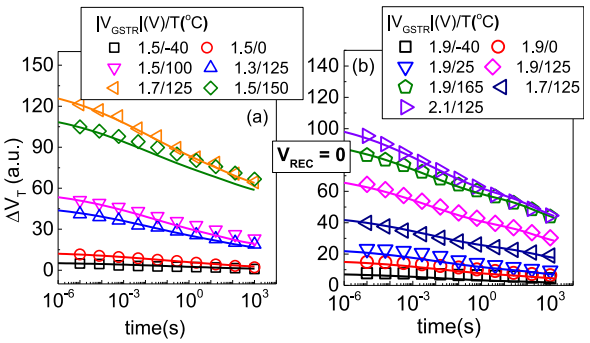

FIGURE 9. Time evolution of measured (symbols) and modeled (lines) recovery of ΔV_T after stress for 0V recovery bias at different V_{GSTR} over an extended range of T for (a) SOI FinFETs and (b) FDSOI devices, from [16].

Fig. 9 plots the measured and modeled time kinetics of ΔV_T after DC stress for a wide range of V_{GSTR} and T conditions for (a) SOI FinFETs and (b) FDSOI MOSFETs, the related stress data are shown in Fig. 5. Once again, no parameters have been re-adjusted between stress and recovery to model such a wide range of recovery data, see [16], [17], [20], [21] for details.

Fig. 10 (a) models the t_{STR} dependence of recovery kinetics in SOI FinFET. Note that the earlier report [17] used empirical ΔV_{HT} model with different (manually) adjusted τ_{DT} at different t_{STR}. However, such dependency is automatically observed in the current BAT implementation owing to the physical nature of the ABDWT model framework. Fig. 10 also plots the V_{GREC} dependence of recovery kinetics after (b) long and (c) short t_{STR} in the same device. The enhanced, ABDWT enabled BAT framework can model such a wide range of recovery data across variations in t_{STR} and V_{GREC} without any manual parameter adjustment or re-adjustment (between stress and recovery).

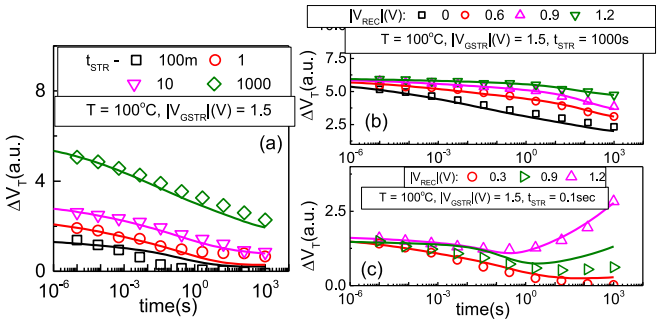

FIGURE 10. Time evolution of measured (symbols) and modeled (lines) recovery of ΔV_T after stress for (a) different t_{STR} at 0 recovery bias and with different V_{GREC} for (b) t_{STR} = 1000s and (c) t_{STR} = 100ms for SOI FinFETs, from [16].

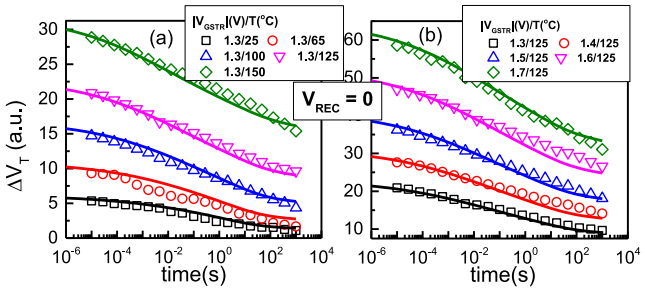

FIGURE 11. Time evolution of measured (symbols) and modeled (lines) recovery of ΔV_T after stress for (a) varying T at fixed V_{GSTR} and (b) varying V_{GSTR} at fixed T. The empirical TTOM equations to calculate the ΔV_{IT} subcomponent is substituted with the ABDWT model. SOI FinFETs are used.

C. VERIFICATION OF TTOM BY ABDWT MODEL

The recovery modeling shown earlier in this work and in all our previous reports are done with empirical equations for the electron capture component (TTOM enabled ΔV_{IT} recovery). Fig. 11 plots the measured and modeled time kinetics of ΔV_T after DC stress using (a) varying V_{GSTR} (but fixed T) and (b) varying T (but fixed V_{GSTR}), where the empirical TTOM for the ΔV_{IT} component is replaced by ABDWT model. Although not shown here for brevity, the ΔV_{IT} recovery time kinetics from RD with empirical TTOM and RD with ABDWT-TTOM are verified with each other. The ABDWT-TTOM parameters are also listed in Table 1. This verifies that the electron capture time constant used in empirical TTOM is physically justified. Due to ease of implementation, the empirical TTOM model is used in all our analysis.

D. TIME CONSTANTS FOR HOLE TRAPPING-DETRAPPING

Fig. 12 plots the simulated ΔV_{HT} (a) stress and (b) recovery time kinetics from ABDWT and empirical models at various V_{GSTR} and T for SOI FinFETs. A similar exercise is done for FDSOI devices, not explicitly shown for brevity. Note that the ABDWT model parameters (see Table 1) are same as used to model measured ΔV_T kinetics using the BAT framework.

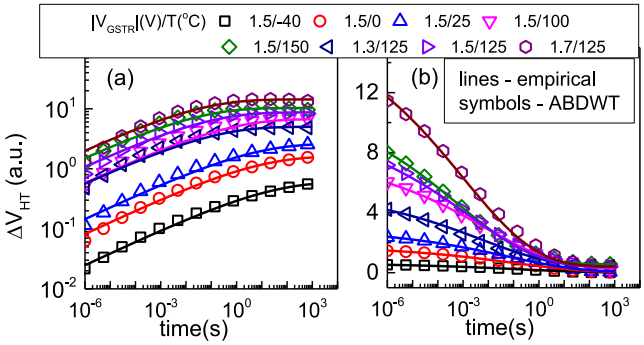

FIGURE 12. Comparison of ABDWT and empirical models for hole (a) trapping and (b) detrapping at various V_{GSTR} and T for SOI FinFETs, from [16].

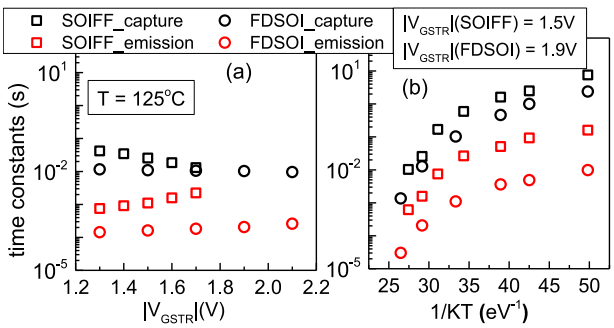

FIGURE 13. Extracted hole capture and emission time constants for SOI FinFETs and FDSOI devices as a function of (a) V_{GSTR} at fixed T and (b) T at fixed bias, from [16].

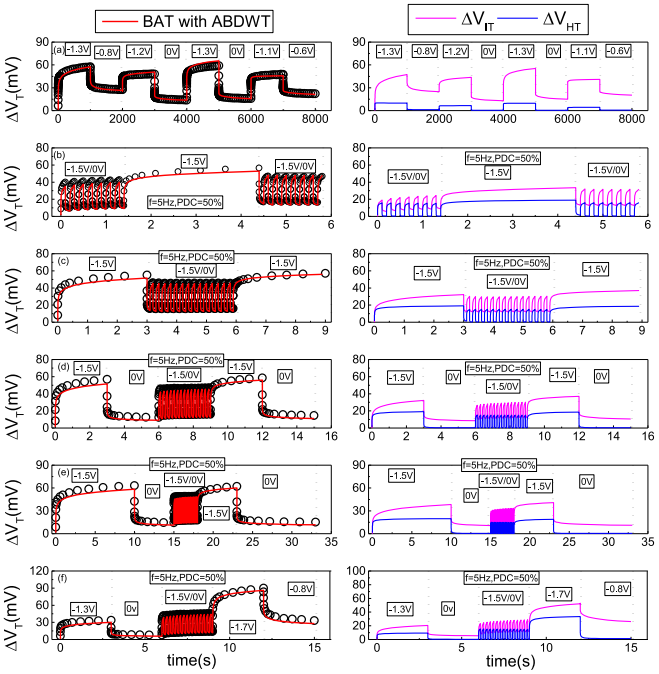

FIGURE 14. Time evolution of measured (symbols) and modeled (lines) ΔV_T for various mixed DC-AC stress (left panels) and the underlying subcomponents (right panels), for (a) DC stress-recovery cycle with varying V_{GSTR} and V_{REC}, (b) AC stress / DC stress / AC stress, (c) DC stress / AC stress / DC stress, (d) DC stress-recovery / AC stress / DC stress-recovery, and DC stress-recovery / AC stress / DC stress-recovery with different (e) time and (f) V_{GSTR} (and/or V_{GREC}) for DC and AC segments. D2 devices are used, from [15].

Fig. 13 plots the empirical model extracted hole capture and emission time constants τ_{HT} and τ_{DT} at different (a) V_{GSTR} (but fixed T) and (b) T (but fixed V_{GSTR}) for both SOI FinFETs and FDSOI MOSFETs. Larger values of τ_{HT} than τ_{DT} implies that the hole capture (∼trapping) is a slower process than emission (∼detrapping) in these devices. Moreover, τ_{HT} reduces and τ_{DT} increases at higher V_G (V_{GSTR} or V_{GREC}) as expected, although the variation is not significant in these devices. However, both τ_{HT} and τ_{DT} reduce at higher T, possibly due to the increased interaction with phonons at elevated T. Importantly, both hole capture and emission processes are fast (compared to the other subcomponents) in the BAT framework. This is in contrast to Comphy, which relies on widely distributed (several orders of magnitude) time constants for the hole capture and emission processes, see [13] and related reports.

E. MULTI-CYCLE STRESS-RECOVERY ANALYSIS

Fig. 14 left panels plot the measured and modeled ΔV_T time kinetics for various (a) DC stress and recovery bias cycles, (b, c) mixed DC stress and AC stress, and (d-f) mixed DC stress-recovery and AC stress for the D2 device. The corresponding right panels show the respective contributions from ΔV_{IT} and ΔV_{HT} subcomponents. The ΔV_{OT} component is not shown as it is negligible in high N% D2 devices [12]. Fig. 15 left panels plot the measured and modeled ΔV_T time kinetics during AC stress under varying V_{GSTR}, f and PDC for the D2 devices. The right panels, once again, plot the respective contributions from ΔV_{IT} and ΔV_{HT} subcomponents. Both Fig. 14 and Fig. 15 model a wide combination of measurements by the ABDWT enabled BAT framework, without making any parameter re-adjustment than that used for modeling simple stress-recovery kinetics. It is noteworthy that for only DC stress data modeling, the ΔV_{HT} subcomponent saturates fast and does not have any significant contribution on overall ΔV_T at a longer time. However, in the subcomponent plots (right panels) of both Fig. 14 and Fig. 15, the ΔV_{HT} component shows a significant contribution on overall ΔV_T as the pulse ON (∼stress) times are short. Nevertheless, the ABDWT model intrinsically handles all cases without any parameter re-adjustments.

F. MODELING OF AC DEGRADATION

The above experiments (Fig. 14 and Fig. 15) use low f AC pulse to show the cycle-by-cycle modeling capability. Higher f AC stress kinetics (up to 1MHz) has been modeled cycle-by-cycle using the BAT framework in [12], [17], [19], the ΔV_{HT} component has been found to be negligible at longer t_{STR}. The reader may refer to the original reports for further details.

Fig. 16 plots the measured and modeled fixed time ΔV_T as a function of PDC for (a) Mode-A and (b) Mode-B AC

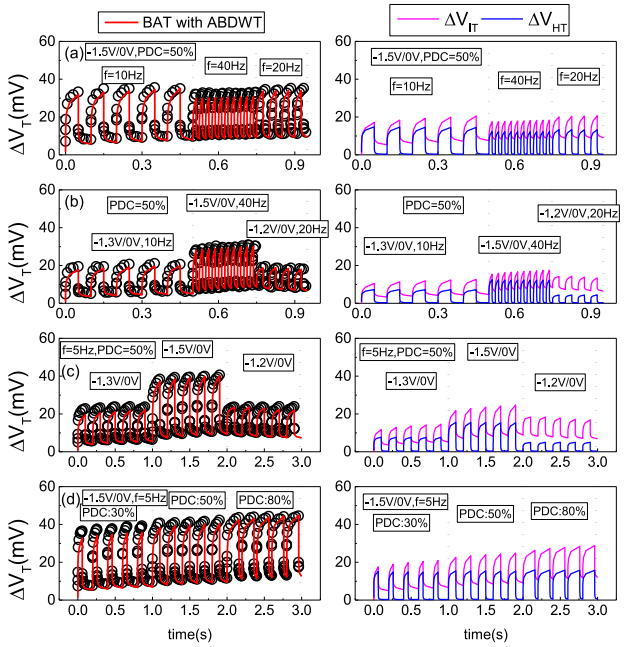

FIGURE 15. Time evolution of measured (symbols) and modeled (lines) ΔV_T for AC stress (left panels) and the underlying subcomponents (right panels), for variation in (a) f, (b) f and V_{GSTR}, (c) V_{GSTR}, and (d) PDC. D2 devices are used, from [15].

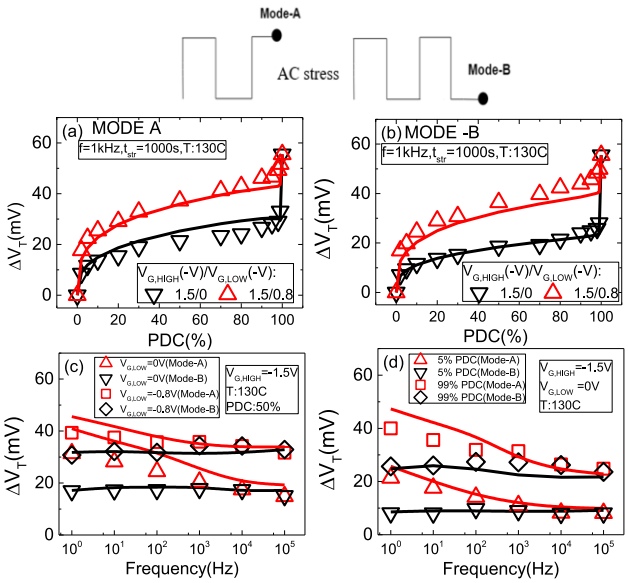

FIGURE 16. Fixed time measured (symbols) and modeled (lines) ΔV_T for AC stress under (a) Mode-A and (b) Mode-B as a function of PDC at fixed f but with different V_{GLOW}, and under both Mode-A and Mode-B as a function of f for different (c) V_{GLOW} at 50% PDC and (d) PDC at 0V V_{GLOW}. The gate pulse for Mode-A and Mode-B stresses are illustrated. D1 devices are used, from [15].

stress, with different V_{GLOW} but with fixed f, and Mode-A and Mode-B AC stress as a function of f with (c) fixed PDC but different V_{GLOW} and (d) fixed V_{GLOW} but different PDC. The AC stress modes are illustrated, and V_{GLOW} is the pulse low bias, which is equivalent to V_{GREC} for DC stress-recovery experiments. D1 devices are used, a similar exercise is reported in [15] for D2 devices, and all simulations are done using the ABDWT-BAT framework. The model can explain S-shaped PDC dependence together with the kink near DC that depends on experimental conditions (stress mode and V_{GLOW}). It can also explain the f dependence (for Mode-A) or f independence (for Mode-B) of AC stress, at different experimental conditions (PDC, V_{GLOW}). No parameters are re-adjusted between DC and AC stress with the exception of empirical ΔV_{OT} model prefactor, see [12], [17], [19] for additional details, and also see [31] for further details on the f dependence of bulk trap generation.

V. CONCLUSION

The BAT framework used earlier to model the NBTI stress-recovery kinetics is now enhanced using ABDWT for the hole trapping-detrapping component. The ABDWT enabled BAT is able to explain a wide range of experimental data under DC and AC stress with just three process-dependent parameters for the ABDWT model, all the other BAT parameters remain the same as before. The time constants associated with the fast recovery of interface trap generation, due to electron capture in TTOM, is also verified using ABDWT. The enhanced BAT framework is validated against different types of devices.

REFERENCES

[1] S. Pae *et al.*, "BTI reliability of 45 nm high-K + metal-gate process technology," in *Proc. IEEE Int. Rel. Phys. Symp.*, Phoenix, AZ, USA, 2008, pp. 352–357, doi: 10.1109/RELPHY.2008.4558911.

[2] C. Ndiaye, V. Huard, R. Bertholon, M. Rafik, X. Federspiel, and A. Bravaix, "Layout dependent effect: Impact on device performance and reliability in recent CMOS nodes," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, South Lake Tahoe, CA, USA, 2016, pp. 24–28, doi: 10.1109/IIRW.2016.7904894.

[3] S. Ramey *et al.*, "Intrinsic transistor reliability improvements from 22nm tri-gate technology," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Anaheim, CA, USA, 2013, pp. 1–5, doi: 10.1109/IRPS.2013.6532017.

[4] H. Lee, C.-H. Lee, D. Park, and Y.-K. Choi, "A study of negative-bias temperature instability of SOI and body-tied FinFETs," *IEEE Electron Device Lett.*, vol. 26, no. 5, pp. 326–328, May 2005, doi: 10.1109/LED.2005.846587.

[5] M. Wang *et al.*, "Bias temperature instability reliability in stacked gate-all-around nanosheet transistor," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2019, pp. 1–6, doi: 10.1109/IRPS.2019.8720573.

[6] S. Mahapatra, V. Huard, A. Kerber, V. Reddy, S. Kalpat, and A. Haggag, "Universality of NBTI—From devices to circuits and products," in *Proc. IEEE Int. Rel. Phys. Symp.*, Waikoloa, HI, USA, 2014, pp. 1–8, doi: 10.1109/IRPS.2014.6860615.

[7] V. Huard, "Two independent components modeling for negative bias temperature instability," in *Proc. IEEE Int. Rel. Phys. Symp.*, Anaheim, CA, USA, 2010, pp. 33–42, doi: 10.1109/IRPS.2010.5488857.

[8] T. Grasser *et al.*, "The paradigm shift in understanding the bias temperature instability: From reaction–diffusion to switching oxide traps," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3652–3666, Nov. 2011, doi: 10.1109/TED.2011.2164543.

[9] S. Mahapatra *et al.*, "A comparative study of different physics-based NBTI models," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 901–916, Mar. 2013, doi: 10.1109/TED.2013.2238237.

[10] J. H. Stathis, S. Mahapatra, and T. Grasser, "Controversial issues in negative bias temperature instability," *Microelectron. Rel.*, vol. 81, pp. 244–251, Feb. 2018. [Online]. Available: https://doi.org/10.1016/j.microrel.2017.12.035

[11] S. Mahapatra and N. Parihar, "A review of NBTI mechanisms and models," *Microelectron. Rel.*, vol. 81, pp. 127–135, Feb. 2018. [Online]. Available: https://doi.org/10.1016/j.microrel.2017.12.027
[12] N. Parihar, N. Goel, S. Mukhopadhyay, and S. Mahapatra, "BTI analysis tool—Modeling of NBTI DC, AC stress and recovery time kinetics, nitrogen impact, and EOL estimation," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 392–403, Feb. 2018, doi: 10.1109/TED.2017.2780083.
[13] G. Rzepa *et al.*, "Comphy—A compact-physics framework for unified modeling of BTI," *Microelectron. Rel.*, vol. 85, pp. 49–65, Jun. 2018, doi: 10.1016/j.microrel.2018.04.002.
[14] S. Desai *et al.*, "A comprehensive AC/DC NBTI model: Stress, recovery, frequency, duty cycle and process dependence," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Anaheim, CA, USA, 2013, pp. 1–11, doi: 10.1109/IRPS.2013.6532117.
[15] N. Choudhury, N. Parihar, N. Goel, A. Thirunavukkarasu, and S. Mahapatra, "A model for hole trapping-detrapping kinetics during NBTI in p-Channel FETs: (Invited paper)," in *Proc. 4th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Penang, Malaysia, 2020, pp. 1–4, doi: 10.1109/EDTM47692.2020.9117913.
[16] N. Choudhury, N. Parihar, and S. Mahapatra, "Analysis of the hole trapping detrapping component of NBTI over extended temperature range," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Dallas, TX, USA, 2020, pp. 1–5, doi: 10.1109/IRPS45951.2020.9129245.
[17] N. Parihar, U. Sharma, R. G. Southwick, M. Wang, J. H. Stathis, and S. Mahapatra, "Ultrafast measurements and physical modeling of NBTI stress and recovery in RMG FinFETs under diverse DC–AC experimental conditions," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 23–30, Jan. 2018, doi: 10.1109/TED.2017.2773122.
[18] N. Parihar, R. G. Southwick, M. Wang, J. H. Stathis, and S. Mahapatra, "Modeling of NBTI kinetics in RMG Si and SiGe FinFETs, part-I: DC stress and recovery," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1699–1706, May 2018, doi: 10.1109/TED.2018.2819023.
[19] N. Parihar, R. G. Southwick, M. Wang, J. H. Stathis, and S. Mahapatra, "Modeling of NBTI kinetics in replacement metal gate Si and SiGe FinFETs—Part-II: AC stress and recovery," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1707–1713, May 2018, doi: 10.1109/TED.2018.2819020.
[20] V. Huard *et al.*, "Key parameters driving transistor degradation in advanced strained SiGe channels," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Burlingame, CA, USA, 2018, pp. 1–6, doi: 10.1109/IRPS.2018.8353699.
[21] N. Parihar *et al.*, "Modeling of process (Ge, N) dependence and mechanical strain impact on NBTI in HKMG SiGe GF FDSOI p-MOSFETs and RMG p-FinFETs," in *Proc. Int. Conf. Simulat. Semicond. Processes Devices (SISPAD)*, Austin, TX, USA, 2018, pp. 167–171, doi: 10.1109/SISPAD.2018.8551724.
[22] N. Parihar, R. Tiwari, and S. Mahapatra, "Modeling channel length scaling impact on NBTI in RMG Si p-FinFETs," in *Proc. Int. Conf. Simulat. Semicond. Process. Devices (SISPAD)*, Austin, TX, USA, 2018, pp. 176–180, doi: 10.1109/SISPAD.2018.8551740.
[23] A. Chaudhary, B. Fernandez, N. Parihar, and S. Mahapatra, "Consistency of the two component composite modeling framework for NBTI in large and small area p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 256–263, Jan. 2017, doi: 10.1109/TED.2016.2630311.
[24] N. Parihar, R. Anandkrishnan, A. Chaudhary, and S. Mahapatra, "A comparative analysis of NBTI variability and TDDS in GF HKMG planar p-MOSFETs and RMG HKMG p-FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3273–3278, Aug. 2019, doi: 10.1109/TED.2019.2920666.
[25] S. Mahapatra and N. Parihar, "Modeling of NBTI using BAT framework: DC–AC stress-recovery kinetics, material, and process dependence," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 1, pp. 4–23, Mar. 2020, doi: 10.1109/TDMR.2020.2967696.
[26] R. Tiwari *et al.*, "A 3-D TCAD framework for NBTI—Part-I: Implementation details and FinFET channel material impact," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2086–2092, May 2019.
[27] R. Tiwari *et al.*, "A 3-D TCAD framework for NBTI, part-II: Impact of mechanical strain, quantum effects, and FinFET dimension scaling," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2093–2099, May 2019.
[28] S. Bhagdikar and S. Mahapatra, "A stochastic hole trapping-detrapping framework for NBTI, TDDS and RTN," in *Proc. Int. Conf. Simulat. Semicond. Process. Devices (SISPAD)*, Udine, Italy, 2019, pp. 1–4, doi: 10.1109/SISPAD.2019.8870524.
[29] S. Mahapatra, N. Goel, A. Chaudhary, K. Joshi, and S. Mukhopadhyay, "Characterization methods for BTI degradation and associated gate insulator defects," in *Fundamentals of Bias Temperature Instability in MOS Transistors* (Springer Series in Advanced Microelectronics), 1st ed., S. Mahapatra, Ed. New Delhi, India: Springer, 2015, pp. 43–92.
[30] D. V. Lang and R. A. Logan, "A study of deep levels in GaAs by capacitance spectroscopy," *J. Electron. Mater.*, vol. 4, p. 1053, Oct. 1975. [Online]. Available: https://doi.org/10.1007/BF02660189
[31] N. Parihar, U. Sharma, R. G. Southwick, M. Wang, J. H. Stathis, and S. Mahapatra, "On the frequency dependence of bulk trap generation during AC stress in Si and SiGe RMG P-FinFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2019, pp. 1–8, doi: 10.1109/IRPS.2019.8720577.