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Understanding and Improving Reliability for Wafer Level Chip Scale Package: A Study Based on 45nm RFSOI Technology for 5G Applications

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ABSTRACT Wafer level chip scale package (WLCSP) is true chip scale package with low cost by eliminating package substrate. The direct chip-to-board attach through solder joints provides low interconnect inductance and resistance, as well as improved thermal performance. These properties make WLCSP a packaging format well suited for 5G radio frequency (RF) applications where minimized package size and parasitics as well as thermal performance are critical. Due to the dissimilar properties between chip and board, the reliability of WLCSP can be challenging. This article reports a reliability study of WLCSP using 45nm RFSOI technology for 5G RF applications. Dedicated test chips and boards were designed and used for board level reliability tests. The test vehicles passed bHAST and drop test, whereas it is found that temperature cycling on board (TCoB) is challenging for solder joint reliability in some cases. Thorough tests were carried out based on Kelvin test on specially designed individual bump and bump pair structures and developed fail criterion. Finite element modeling was adopted to simulate the reliability performance in different configurations. The impact on reliability performance from bump depopulation, die thickness, bump size, UBM to board pad alignment, and board wiring trace were thoroughly investigated. Based on comprehensive testing and deep understanding of the failure mechanisms, design optimizations for chip, board and interconnect were implemented. WLCSP reliability was significantly improved.

INDEX TERMS WLCSP, 5G, mm-wave, board level reliability, temperature cycling on board, solder joint fatigue, finite element modeling.

I. INTRODUCTION

It is estimated that the coming 5G network will connect more than 100 billion devices and deliver fast radio frequency (RF) data communication with high bandwidth and low latency among these devices. This will have profound impact on a variety of fields, including computing, communication, consumer, industrial, medical and automotive. A high performance, low cost yet reliable packaging solution is a key enablement for the wide adoption of 5G.

Wafer level chip scale package (WLCSP) is a workhorse in advanced packaging in recent years [1]–[2]. Fig. 1 shows a schematic of the WLCSP chip/bump build-up cross-section, where a solder ball directly landed on a chip pad via a UBM (under bump metallization) layer. The chip pad is typically an Al pad fabricated during wafer back end of line (BEOL) process. A passivation layer, which is typically polyimide-based material, is also deposited on top of the chip BEOL. Such configuration with bump landing on chip pad is referred as BOP (bump on pad). Alternatively, the connection between solder bump and chip can be through a redistribution layer (RDL) or multiple RDLs. The bumped chip is then directly attached to a printed circuit board (PCB) without using a substrate in between.

WLCSP is suited for the RF applications that 5G is targeting at. The 5G rollout starts with sub-6GHz and is to be followed by millimeter wave (mm-Wave) band. In these frequency ranges, especially in mm-Wave, one great challenge is the free space loss of the radiated signal power. The direct chip-to-board attach through solder joints in WLCSP provides low interconnect inductance and resistance.

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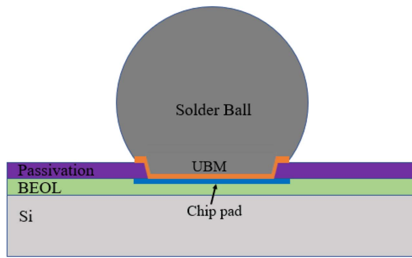

FIGURE 1. Schematic of the chip/bump build-up cross-section.

TABLE 1. Test vehicles.

	Die	*Die thickness*	*BEOL*	*Bump diameter*	*Bump pitch*
TV1	D1	280 μm	S1	150 μm	350 μm
TV2	D1	280 μm	S2	150 μm	350 μm
TV3	D1	200 μm	S1	200 μm	350 μm
TV4	D2	280 μm	S1	220 μm	400 μm

This results in greatly reduced package parasitics and signal loss. To further mitigate the RF signal loss, high gain antenna arrays with power amplifiers, which also dissipate significant amount of heat, are often employed [3]. The direct chip-to-board connection of WLCSP also improves the package thermal performance which is critical to 5G RF applications. WLCSP also offers the smallest package footprint with true chip scale package, which is beneficial to applications such as mobile, wearable and IoT. Furthermore, the elimination of package substrate in WLCSP reduces the cost, which is essential for adoption at scale.

The reliability of a WLCSP needs to be thoroughly assessed and understood before implementing this assembly technology for production. It is well known that the chip-package interaction (CPI) in flip chip can result in reliability fails such as white bump, die corner crack and delamination, and solder fatigue [4]–[7]. In WLCSP, chip is directly attached to PCB which has drastically dissimilar material properties compared to chip. This results in increased thermo-mechanical stress on the chip and solder joints, posing more challenges to CPI risks. When the silicon technology used in WLCSP evolves into more advanced nodes which typically use low k or ultra-low k (ULK) dielectrics in BEOL for electrical performance, the chip structural integrity issue under CPI becomes increasingly challenging due to the less favorable mechanical properties of low k and ULK. To mitigate the CPI risk, the size of chips used in WLCSP is typically small, which fits RF application needs.

A perhaps even more difficult challenge is solder joint reliability (SJR). The CPI thermo-mechanical stress can cause crack generation and growth in solder joints and eventually fail the interconnect. In RF applications, smaller bump size is preferred for improved performance. In many cases, a fairly large percentage of chip area is depopulated with solder bumps to further reduce the coupling noise. These two requirements can significantly impact the reliability life of the solder bumps even for small chip applications.

Researchers have spent significant effort to improve WLCSP reliability. Shih *et al.* [8] showed the thin die and thicker dielectric can improve reliability for drop test and temperature cycling on board (TCoB) performance. Chiu *et al.* [9] discussed PBO opening and board thickness impacts on fail rate of ULK layers during TCoB Stress. Wu and Malinowski [10] presented a work in achieving enhanced WLCSP reliability by optimizing die, bump and board design. Zhang *et al.* [11] developed plastic work based finite element model (FEM) to predict SJR lifetime.

This article reports a comprehensive study on WLCSP reliability based on 45nm RFSOI technology, 45RFSOI, a high performance 300mm RF platform developed by GLOBALFOUNDRIES. This RF technology is well suited to applications in 5G base stations, backhaul, satellite, radar, and front-end modules for mobile devices. Both component level reliability (CLR) test and board level reliability (BLR) test on multiple test vehicles are conducted. FEM simulation is adopted to assist comprehending the experimental observations. Effects of die thickness, bump size, bump depopulation, die to board alignment, board wiring design are thoroughly investigated. By in depth analysis and comprehension of failure mechanisms, optimization is implemented and WLCSP reliability is significantly improved.

II. TEST VEHICLE

Dedicated test chips were used for this WLCSP work. TABLE 1 lists four test vehicles based on two test chips: D1 and D2 [10]. The area of D1 and D2 are 3.4 mm by 3.4 mm, and 3.6 mm by 3.6 mm, respectively. The die used in TV3 is 80 μm thinner than other TVs. All chips use full flow FEOL and BEOL processes. Two BEOL stacks S1 and S2 are used. Stack S1 has 10 Cu metal levels with a 2 μm thick Al. Stack S2 has 7 Cu levels and with a 4 μm thick Al. Both stacks have low k dielectrics, whereas S1 also has ULK layers. The k value of S1 ULK is 2.45 which is even lower than the ones used in most advanced nodes. This low k value boosts electrical performance and reduces the power consumption, but with increased CPI risk.

The dedicated test structures on the test chips include chip perimeter lines, perimeter via stacks, under bump serp-combs, under bump via stacks, individual corner bump stitches & stitch pairs, and bump daisy chains. The test structures were used to detect structural integrity fails and moisture ingress related degradation. ESD protection circuits were also designed for the ESD sensitive test structures. The test structures have a wide test coverage and these structures had also been placed at CPI critical locations which include, the corner bumps, the die corners and the peripherals, and the under bump BEOL stacks.

The bumping process used is a ball drop BOP without RDL, shown in Fig. 1. This design results in the shortest path between PCB to circuits on chip with optimum signal

TABLE 2. Component level reliability test.

Stress	*Condition*	*Duration*	*Result*
Pre-con	125°C bake	24 hr	PASS
	85°C, 85% RH	168 hr	
	260°C reflow	3x	
TC-B	-55°C to 125°C	1000x	PASS
uHAST	110°C, 85% RH	264 hr	PASS
HTS	150°C	1000 hr	PASS

performance. The bump material used is SAC405 with a PBO passivation. The solder raw ball diameters before bumping are 150 μm, 150 μm, 200 μm and 220 μm for TV1, TV2, TV3 and TV4, respectively. The bump pitch is 350 μm and 400 μm for D1 and D2 respectively. These small size bumps are challenging for reliability. In addition, D2 has about 25% of chip area with bump depopulation for enhanced RF performance, which results in more stress to the remaining bumps, including the corner bumps, thus further increases the reliability failure risk.

III. COMPONENT LEVEL RELIABILITY

To ensure the dies have no intrinsic reliability issue, a component level reliability (CLR) test was first conducted on dies with bumps. TV1 and TV2 were used for this component level reliability test. Standard JEDEC environmental stresses, including temperature cycling (TC, condition B), unbiased HAST (uHAST), high temperature storage (HTS, 150°C), were used for this reliability evaluation. Prior to each stress tests, a MSL1 (moisture sensitivity level 1) pre-conditioning (pre-con) was also applied to all parts. The details of the stress conditions are listed in TABLE 2. Both TV1 and TV2 passed all CLR tests. These tests verify that the test chips after bumping are intrinsically robust.

IV. BOARD LEVEL RELIABILITY

A. HAST TEST

Due to the elimination of the organic laminate between chips and PCBs, the impact from PCBs to chips and solder joints are critical to the WLCSP reliability. BLR tests were used to further evaluate the robustness of chips and solder joints under CPI. Stresses include biased HAST (bHAST), drop test, and temperature cycling on board (TCoB). Low-k and particularly ULK dielectrics have much faster moisture uptake than TEOS. Patterned metal crackstop structures, also known as seal rings, are implemented in the BEOL of chip peripheral to block cracks as well as moisture from penetrating into the active chip area. bHAST is an effective test to detect moisture ingress through a defective seal ring. TV1 and TV2 were used for bHAST under 3.6V, 110°C and 85% RH. Both TVs passed 264 hours of stress, confirming there is no moisture ingress issue for both BEOL stacks S1 and S2, and the seal rings for both BEOL stacks are effective.

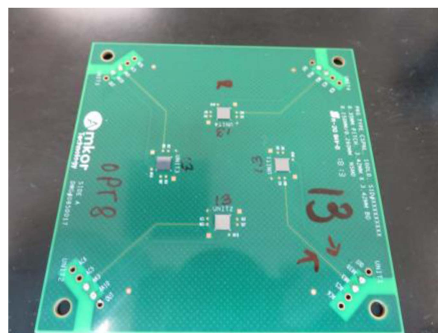

FIGURE 2. Drop test board with 4 dies mounted.

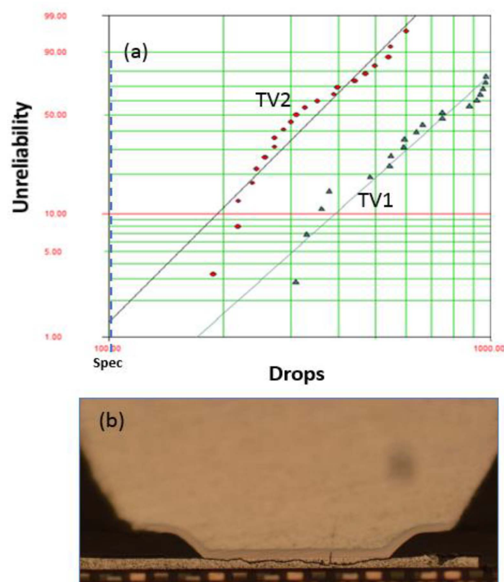

FIGURE 3. (a) Weibull plots of drop test result; (b) cross-sectional optical micrograph of a common drop test failure mode.

B. DROP TEST

The drop test was performed following the JESD22-B110B condition B with 1500G acceleration, 0.5 ms impact time, half-sine pulse. The test board used conforms to the JEDEC JESD22-b111a recommendation. The board is composed of 10 layers FR4 dielectric and Cu wiring traces, with a 1018 μm total thickness. The PCB metal pads for solder joints are non-solder mask defined (NSMD). Four chips are placed on each board symmetrically following JEDEC recommendation. Fig. 2 shows a picture of the test board used in this study. No underfills were used for all parts.

TV1 and TV2, with different BEOL stacks, were used in this study. Tests were run up to 1000 drops. The Weibull plots of drop test fail distributions are shown in Fig. 3(a). TV1 has better performance in drop test compared to TV2. Fig. 3(b) shows a failure analysis optical micrograph. The commonly observed failure mode which is under UBM cracking into Al pads. The worse drop test performance of TV2 is probably attributed to the 4 μm thick Al level in the BEOL stack, which makes it stiffer than 2 μm thick Al

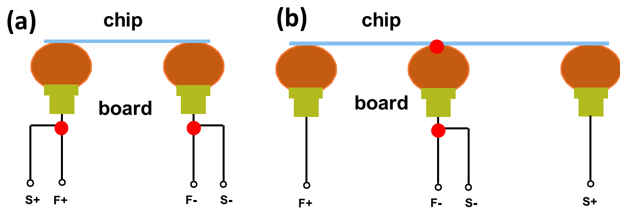

FIGURE 4. Schematics for the bump test structures and Kelvin test schemes (a) Individual bump pair structure; (b) Individual bump structure.

on TV1 and therefore more prone to a crack initiation. The relatively softer ULK in TV1 may also have helped to suppress this fail mode. Nevertheless, both TV1 and TV2 pass the 100-drop spec by wide margin. Hence, there is no concern on field drop reliability life for the targeted 5G RF applications [10].

C. TEMPERATURE CYCLING ON BOARD TEST

Temperature cycling on board (TCoB) is to assess the impact of thermo-mechanical stress from PCBs to dies and solder bumps. Due to significant CTE mismatch between PCBs and dies, TCoB is one of the most challenging stresses and critical to WLCSP reliability evaluation. All TVs were used in TCoB study. Throughout all tests, no silicon or BEOL related fails were observed, confirming the silicon technology is robust to survive TCoB stress. The failure mode observed was solder joint fatigue fail which is the focus of this section.

C.1. TEST METHOD AND FAIL CRITERION

The build-up layers of TCoB board follows JEDEC JESD22-b111a recommendation. Four dies are placed on each board similar to the drop test board fashion. Again, no underfills were used on these parts.

The differentiation is that TCoB in this study has wider test coverage and better test accuracy. It is often practiced by many others that TCoB uses the same test and criterion as the drop test which monitors resistance of daisy chains with a 1000-ohm shift in resistance as the fail criterion. In this work, multiple BEOL CPI structures and individual bump structures are tested in addition to the daisy chains. Especially, a four-point Kelvin test is used on individual bumps and bump pairs including the bumps located in the most critical area at the die corner. The ability to measure a very low resistance of the solder bump must be applied, which is beyond the resolution of typical daisy chain measurement [10].

Fig. 4 shows the schematics for the bump test structure and Kelvin test schemes with force and sense on each terminal labeled. Fig. 4(a) illustrates a bump pair test structure. Fig. 4(b) illustrates a test structure for individual bumps where the inner bump can be individually tested.

Fig. 5 shows a picture of the TCoB board. To accommodate the number of I/Os needed to enable Kelvin test on bump structures and BEOL CPI structures, four connectors

FIGURE 5. TCoB test board with 4 dies and 4 connectors mounted.

with 4x50 pins are mounted on the PCB and employed in the test.

Fig. 6(a) shows the measured bump resistance sampling data. Each data point on the graph represents a sample chip. The individual corner bump of TV3 shown in blue color is about 25 milliohms. The corner bump pair of TV4 shown in grey color is about 44 milliohms. These data are stable for many samples. Fig. 6(b) shows the resistance shift of a bump pair net monitored by the four-point Kelvin method during TCoB stress test. TC condition N (0-100°C) was used in this case. Resistance shifts were observed on many chips. Majority of these parts have only a resistance shift of a few Ohms, with some of them even below 1 ohm. They stay in that low resistance shift range for hundreds of cycles of stress, which would not be detected as fails if the typical daisy chain measurement were used with 1000-ohm resistance shift as fail criterion. Only a few of these parts went to electrical open and beyond 1000 ohms, which would be detected as fails.

However, by physical failure analysis (PFA), we find that there are already through cracks in the solder bumps of the samples with a low resistance shift. Fig. 7 shows a Scanning Electron Microscopy (SEM) image of the bump cross-section prepared by Focused Ion Beam (FIB). There is clearly a through crack in the solder bump above UBM close to the chip side. Such through cracks in bump structures with low resistance shifts after stress are repeatable on a large sample size across all TVs.

The physical explanation of why a cracked bump is not electrically open may be, due to the cross-sectional area of a solder bump is relatively large, when a crack breaks through a bump, there can still be some area where two cracked surfaces contacting each other and forming a conducting path for the electrons. The resistance is increased up to a few ohms as observed due to smaller conducting area and additional surface or interface scattering. From functionality point

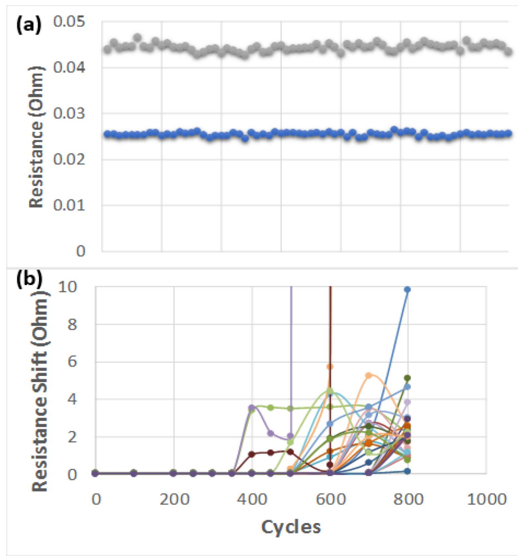

FIGURE 6. (a) Blue: resistance of a corner bump structure of TV3; Grey: resistance of a corner bump pair structure of TV4; (b) Resistance traces of a bump test structure in TCoB stress test.

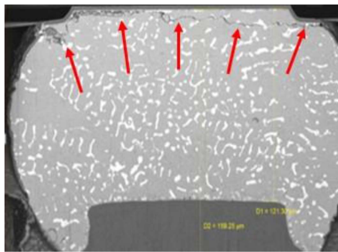

FIGURE 7. FIB cross-section of a bump with less than 10 ohms of resistance shift post stress shows a through crack in the bump.

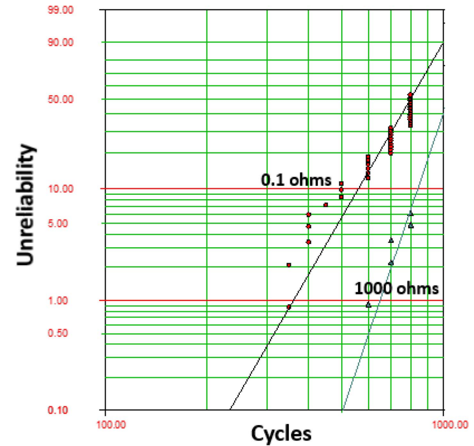

FIGURE 8. Weibull plots for TCoB fails based 1000 ohms and 0.1 ohms resistance shift as fail criteria.

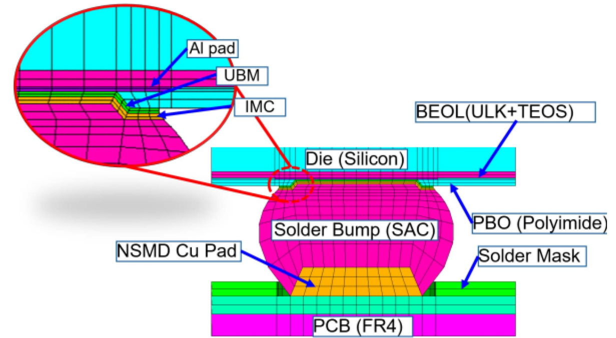

FIGURE 9. Solder bump and connection structure finite element model.

of view, small resistance shift may have limited impact to DC power bumps. For the signal bumps, it could degrade the performance or even impact functionality depending on the tolerance of design. For RF signal, the crack surfaces could also create reflection which may be detrimental to RF signal integrity. Although the true impact of a low resistance change especially for RF bumps on actual product performance requires further design dependent investigation, the 1000-ohm fail criterion can be too overoptimistic in product reliability projection.

We developed a fail criterion based on 0.1 ohms resistance shift which was verified by failure analysis as good criterion in detecting cracks. Plotted in Fig. 8 are the Weibull plots of the same set of data based on two different criteria: 1000 ohms versus 0.1 ohms. The drastic difference is apparent. The first fail based on 1000 ohms criterion starts at 600 cycles, whereas, if based on 0.1 ohms criterion, it starts at 350 cycles. Based on a 100 ppm extrapolation, the reliability life projection based on 0.1 ohms shift is about 3 times shorter than 1000 ohms shift which is overoptimistic [10]. The rest TCoB discussion of this article will be based on 0.1 ohms resistance shift as the fail criterion.

C.2. FINITE ELEMENT MODELING

To better understand WLCSP TCoB experimental results, FEM simulation was performed. A 3D quarter symmetric model was built by using commercial software ANSYS. Fig. 9 shows the detailed solder ball sub-model. This sub-model will be used to investigate critical corner bump behavior during TCoB stress test.

Solder joint goes through uniform temperature cycling during TCoB stress. Anand constitutive model [12] is used to simulate the solder's creep behavior. Anand model constitutive equations can be written as:

$$\frac{d\varepsilon_p}{dt} = A\left[\sinh\left(\varepsilon \cdot \frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \cdot \exp\left(\frac{-Q}{kT}\right)$$

and three evolution equations in,

$$\frac{ds}{dt} = \left\{h_0 \cdot (|B|)^a \cdot \frac{B}{|B|}\right\} \cdot \frac{d\varepsilon_p}{dt}$$

$$B = 1 - \frac{s}{s^*}$$

$$s^* = s^{\wedge}\left[\frac{1}{A} \cdot \frac{d\varepsilon_p}{dt} \cdot \exp\left(\frac{Q}{kT}\right)\right]n$$

where $d\varepsilon_p/dt$ is inelastic strain rate, ϵ is the multiplier of stress, σ is equivalent stress, Q is activation energy, k is

TABLE 3. Anand constants for solder ball.

Constant	Parameter	Value
C1	S_0 (MPa)	45.9
C2	Q/k (1/k)	7460
C3	A (1/sec)	5.87e6
C4	ξ	2
C5	m	0.0942
C6	H_0 (MPa)	9350
C7	S^ (MPa)	58.3
C8	n	0.015
C9	a	1.5

Boltzmann's constant, T is absolute temperature, s is deformation resistance with initial value as s_0, A is pre-exponential factor, ξ is multiplier of stress, m is strain rate sensitivity of stress, h_0 is hardening constant, $s^{\wedge}$ is coefficient for deformation resistance saturation value, n is strain rate sensitivity of saturation (deformation resistance) value, and a is strain rate sensitivity of hardening. The relative parameters used in this study are listed in TABLE 3 and were provided from the material vender.

Darveaux methodology [13] was used in this study and its solder life prediction calculate equations can be shown as:

$$N_0 = C_1(\Delta W)^{C_2}$$
$$\frac{da}{dN} = C_3(\Delta W)^{C_4}$$

where N_0 represents the initial crack life, da/dN represents the crack propagation rate, and ΔW is the increment of plastic work density of solder balls. C1∼C4 are material model constants and can be fit using a combination of experimental testing and Finite Element Analysis (FEA) simulation.

$$N_f = N_0 + \frac{a}{da/dN}$$

where N_f represents the characteristic cycles to failure and a represents the characteristic crack length [11].

In this work, a was set to UBM diameter since the crack was found propagating along with the UBM. Three thermal cycles were simulated (Fig. 10). Each cycle's plastic work increment (ΔW_x) was calculated from weight averaged plastic work increment at solder critical region [11]. The increment of plastic work density (ΔW), used in Darveaux model to determine solder joint lifetime, was calculated from $\Delta W_3 - \Delta W_2$.

The elastic material properties used in model are listed in TABLE 4.

C.3. EFFECT OF BUMP DEPOPULATION

In some RF applications, a fairly large percentage of chip area is depopulated with solder bumps for performance enhancement. The remaining interconnects are exposed to more mechanical stress, which could result in a shorter lifetime than a fully populated WLCSP package. An FEM simulation study was performed to assess the impact of the bump depopulation to reliability. Fig. 11 shows the modeling details. The die was removed in the figure to better show solder array population. Corner bump is set to the most critical bump. The impact of bump depopulation was evaluated by adding and removing adjacent bumps.

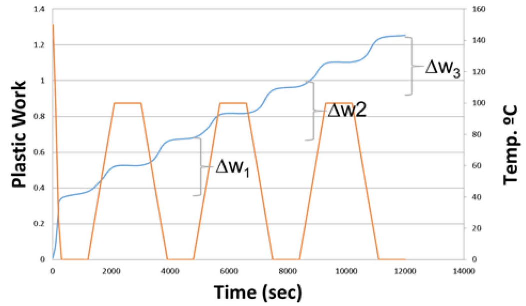

FIGURE 10. Plastic work accumulation per cycling.

TABLE 4. Elastic material properties used in model.

Material	Modulus (GPa)	Poisson ratio	CTE (ppm)
Silicon	165	0.22	2.6
Aluminum	69	0.3	22
BEOL	59	0.24	1
Copper	117	0.35	17
FR4	29.9	0.35	13.5
PBO	2.3	0.35	64
UBM	135	0.33	14.5
Solder	53	0.5	22
Solder mask	3.2	0.35	60

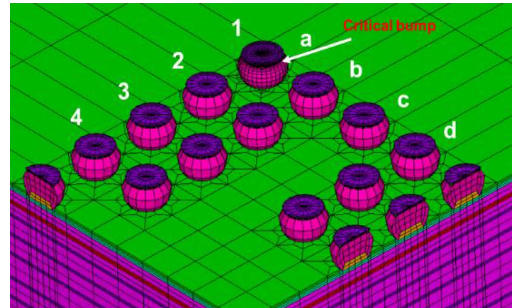

FIGURE 11. Depopulated solder bump model configuration.

Fig. 12 shows the plastic work reduced by adding adjacent bumps. Simulation result shows the bumps closer to the corner bump have bigger impact on lifetime of the corner bumps. Bump 2a, 1b and 2b (shown in Fig. 11), which are neighboring the corner bump 1a, are the most important bumps to reduce the plastic work on bump 1a. The impact on the corner bump reliability from the population of other bumps further away from the corner bump is less significant.

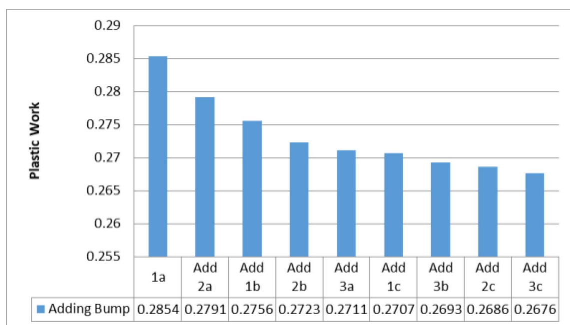

FIGURE 12. Plastic work change on corner bump by adding support bump.

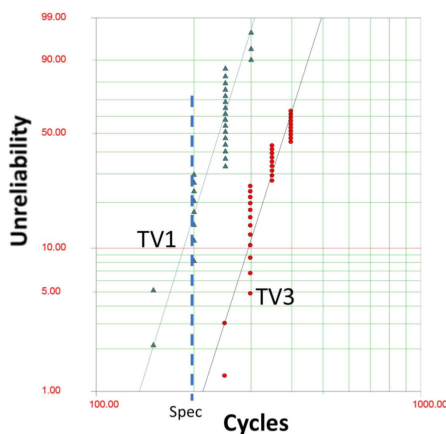

FIGURE 13. Weibull plots for TCoB fails for TV1 and TV3. Fail criterion is based on 0.1 ohms resistance shift.

C.4. EFFECTS OF BUMP SIZE AND DIE THICKNESS

Bump size and die thickness are two important factors impacting SJR during TCoB. In this section, TV1 and TV3 were used to study the effects. Both TV1 and TV3 are with BEOL stack S1 which has ULK in the stack and thinner Al. It is obvious that S1 is the risker case for CPI in terms of BEOL integrity compared to S2. For SJR, it was also observed in another assessment that BEOL stack S2 on TV2 is slightly better than that of BEOL stack S1 on TV1, perhaps due to the thicker stack of S2 keeping the Si substrate slightly further away from PCB [10]. Therefore, TV1 and TV3 were used to cover the worse cases for both Si and interconnects.

In general, thinner die is more flexible to bend upon stress from board so that the solder joints deform less. Therefore, it is beneficial to solder reliability. A larger bump ball size resulting in larger standoff height and more compliant bumps if same UBM diameter is used. In case of a larger UBM diameter, the force is spread out to a larger area and a crack needs to grow for a longer length to break through a bump. It is reasonable to expect better reliability for these two cases too.

Fig. 13 shows Weibull plots of TCoB reliability wear-out data for TV1 and TV3, with 0.1 ohms resistance shift as criterion [10]. The TCoB stress is based on condition G

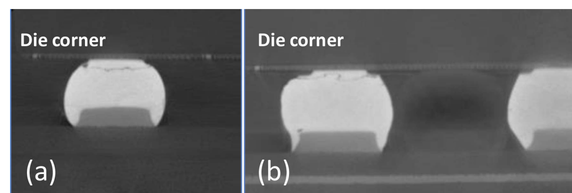

FIGURE 14. (a) X-ray image of a TV1 fail in a die corner bump; (b) X-ray image of a TV3 fail in a corner bump, and an intact adjacent bump without crack.

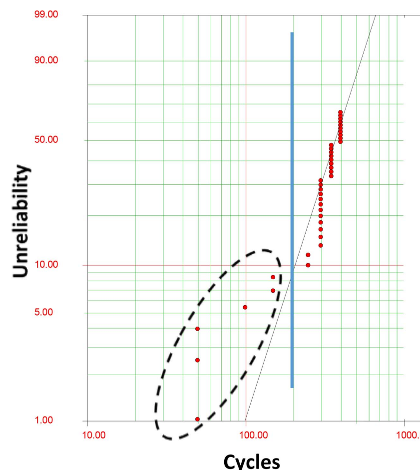

FIGURE 15. Weibull plots for TCoB fails for TV3 with the early fails highlighted.

which is −40°C to 125°. TV1 starts to fail at 150-cycle readout with a characteristic life at 250 cycles, whereas TV3 starts to fail at 250-cycle readout with a characteristic life at 400 cycles. The reliability performance trend is consistent with expectation.

Failure analysis by X-ray imaging was performed on both TV1 and TV3 fails. As shown in Fig. 14 (a) and (b), the failure mode for both TVs is solder crack in corner bumps. The crack path is in the bulk of solder above UBM. Also shown in Fig. 14(b) is an adjacent bump which is intact without any crack formation. In other words, the rest bumps are still functioning. This suggests that the product reliability could be significantly enhanced, if a redundant bump design is used for bumps placed at the corner of the die.

C.5. EFFECT OF UBM TO BOARD PAD ALIGNMENT

In the TCoB experiment (condition G) for TV3, there are a few early fails observed. Fig. 15 shows the Weibull plots of accumulated fail percentage including the early fails. The test readout cadence is 50 cycles. There appears to be 2 different distributions of the fails. The early fails start at 50 cycles and ends at 150 cycles. Then there are no fails at 200 cycle readout. The main distribution of fails start at 250 cycles. It indicates that the early fails may have a different mechanism.

The failure modes of the fails in both distributions are investigated by PFA. Fig. 16 shows the X-ray images for the early and late fails. Fig. 16(a) shows a cracked solder and

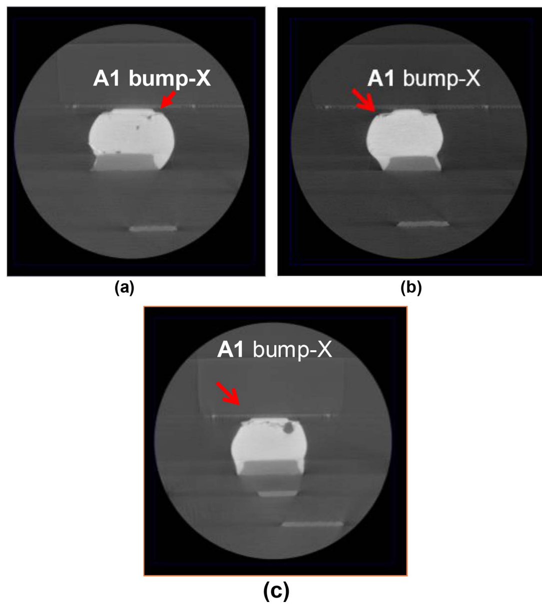

FIGURE 16. X-ray images for TCoB failed corner bumps. (a) and (b) Early fail samples; (c) normal wearout fail sample from the main distribution.

UBM misaligned with PCB pad and towards to die center. Fig. 16(b) shows a cracked solder and UBM misaligned with PCB and towards to die edge. Fig. 16(c) shows solder normal wear out cracks. From PFA, early fail samples were associated with UBM to board Cu pad misalignment bump at the corner bump.

FEM was used to analyze the misalignment impact on solder joint reliability [11]. Two types of misalignment were simulated: one is Cu pad towards die center and the other is Cu pad towards die edge. The misalignment angle used in the simulation is fixed as 9.3° which matches with the measurement by PFA. Simulation results show the numbers of cycle to failure reduced sharply for UBM/Cu pad misalignment solder bump. For Cu pad shift towards die center 25μm corresponding to 9.3° misalignment, N_f was reduced ~31% and for Cu pad shift towards to die edge, N_f was reduced ~37%. TABLE 5 lists the modeling geometry inputs and $N_f$comparison. Simulation results verified the testing results. UBM/ board Cu pad misalignment has significant impact on solder joint fatigue life and should be minimized by process or design optimization [11]. This UBM/Pad misalignment is related to the board pad dimension and solder mask opening (SMO) is close to process window edge. It is only observed on TV3. It is believed that by optimizing the board design, e.g., using a larger SMO, this misalignment issue thus the early fails can be resolved.

C.6. EFFECT OF BOARD WIRING TRACES

Board design can also have large impact on the solder bump reliability. This section studies the effect of board wiring traces connecting to the Cu bump pads. TV4 with 220 μm diameter bump sphere and 400 μm pitch is used for this study. In one design, the wiring traces connecting to NSMD pads are running in solder mask layer, as schematically

TABLE 5. UBM/PAD misalignment model input and result.

	POR	Misalignment right side	Misalignment Left side
Die Size, mm	3.42x3.42x0.2	3.42x3.42x0.2	3.42x3.42x0.2
UBM Diameter,um	180	180	180
Bump Diagemeter, um	230	230	230
Bump Height	152.8	152.8	152.8
Number of Bump	100 (10x10)	100 (10x10)	100 (10x10)
Bump Pad Type		Pad Shift Towards Die center	Pad Shift Towards Die Edge
Board Type	JES22-B111A	JES22-B111A	JES22-B111A
Solder Materials	SAC405	SAC405	SAC405
ΔPLNW/cycle	0.9014	1.3196	1.4469
Normalized No. of Cycle to fail	1.00	0.69	0.63

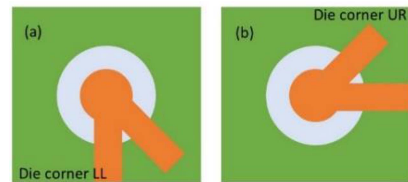

FIGURE 17. Schematics for NSMD Cu pads and wiring traces designed at LL corner (a) UR corner (b).

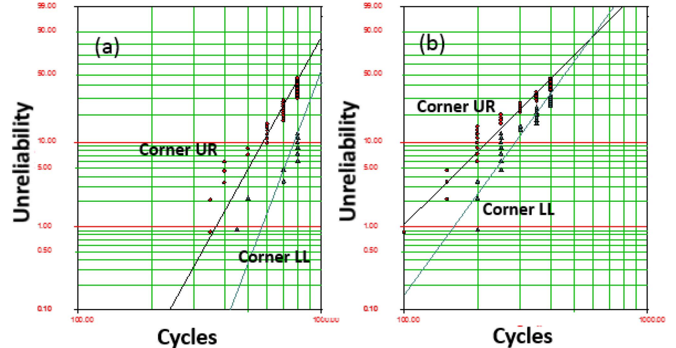

FIGURE 18. Weibull plots of TCoB fails for corner UR and corner LL. (a) TC condition N; (b) TC condition G.

shown in Fig. 17. To enable sensitive Kevin test, each corner bump has two wiring traces. The lower left (LL) corner and the upper right (UR) corner have slightly different designs, as shown in Fig. 17(a) and (b).

TCoB test data based on this TV4 board design is presented in Fig. 18, where the reliability performance of corner LL and corner UR is compared. Two TC conditions were used in the stress: condition N which is 0 to 100°C shown in Fig. 18(a), and condition G which is −40°C to 125°C shown in Fig. 18(b). Fail criterion used is still 0.1 ohms resistance shift. Interestingly, corner UR has consistently worse reliability than corner LL for both stress conditions [10].

A wiring trace in the design above essentially increases the area of a Cu pad. It is known that larger pad size drives up

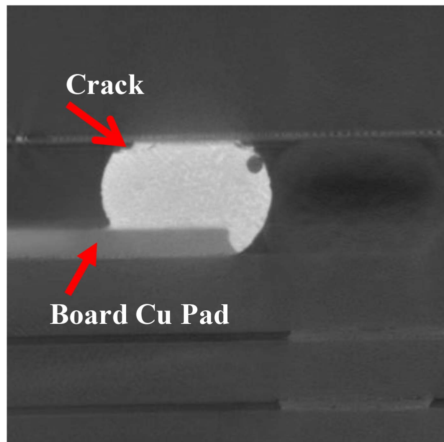

FIGURE 19. X-ray image of a failed corner bump showing a crack in solder bump above UBM and the board Cu pad and wiring trace.

the stress in the bump close to UBM. Two traces connecting to one Cu pad makes the situation worse. Therefore, the designs at both LL and UR corners are not favorable to reliability.

Fig. 19 shows an X-ray image of a failed bump where the Cu pad on the board connecting directly with the wiring trace in solder mask layer can be observed. Although the designed Cu pad to UBM area ratio is about 0.8 which is in the optimal range, the effective pad size is significantly increased due to the wiring. This results in earlier crack fails in the solder bump above UBM, which can also be observed in Fig. 19.

Due to the symmetry of the chip and bump design, the difference between corner LL and corner UR should come primarily from the diagonally orientated traces. In corner UR, the wetting of solder to the diagonal trace tends to drive more solder towards die corner. These design differences may explain the differences in the reliability results between the corner UR and corner LL.

FEM is also used to simulate the impact of Cu trace and pad on solder reliability. Three solder bump landing types on PCB were studied: 1) solder connecting to joint of two traces; 2) solder directly connecting to single trace; and 3) solder connecting to a round pad and the pad connects the 2nd level metal trace through via. Simulation results indicate two traces connecting has a decreased solder joint lifetime and solder on round pad has the best predict solder joint lifetime. The lifetime order is solder on pad (1.00) > solder on one trace (0.83) > solder on two traces (0.60). Normalized N_f comparison and model input between three cases were listed in TABLE 6. Traces connecting to solder should be avoided. Moving traces below the solder mask and connecting solder to Cu pad through via are suggested [11].

C.7. RESULTS AFTER OPTIMIZATION

The above learnings were then implemented on TV4 with optimized board design and die attach assembly processes. The board is designed with both traces moved to a layer below solder mask and connected to Cu pad through a via. Fig. 20 shows the original and modified solder bump landing configuration and wiring traces. Since we have confirmed from above study that the failure modes in TCoB condition N and condition G are the same, with an acceleration factor between 3 and 4, from Fig. 18. The TCoB condition G had been applied for the parts assembled on this board with optimal designs and processes. The TCoB stress test result is shown in TABLE 7. It passes 1000 cycles of stress. The reliability is significantly improved.

TABLE 6. Board Cu PAD configurations for modeling and lifetime comparison.

	Bump on two traces	Bump on one trace	Bump on pad
Die Size, mm	3.42x3.42x0.2	3.42x3.42x0.2	3.42x3.42x0.2
UBM Diameter,um	180	180	180
Bump Diagemeter (ARF), um	230	230	230
Bump Height	152.8	152.8	152.8
Number of Bump	100 (10x10)	100 (10x10)	100 (10x10)
Bump Pad Type			
PCB Pad Model			
Board Type	JES22-B111A	JES22-B111A	JES22-B111A
Solder Materials	SAC405	SAC405	SAC405
ΔPLNW/cycle	1.5077	1.0806	0.9014
Normailized No of cycle to fail	0.60	0.83	1.00

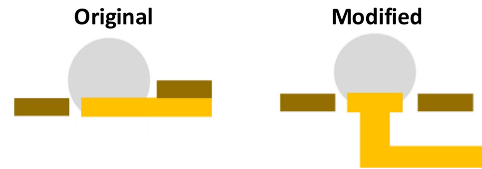

FIGURE 20. Original and modified design for board wire trace and bump landing configuration.

TABLE 7. TCoB of TV4 after optimization.

Stress	*Condition*	*Duration*	*Result*
TCoB	-40°C to 125°C	1000x	PASS

Note that all the above studies are based on vehicles without underfill. The product reliability can be further enhanced if an optimized underfill material is applied.

V. CONCLUSION

This article summarizes the results of reliability study carried out on WLCSP with different design features based on 45RFSOI technology. Reliability tests had been conducted on component and board level. The most challenging reliability is TCoB. From the testing and simulation results, it can be concluded:

1) Kelvin test on individual bump and bump pair structures with 0.1 ohm resistance shift fail criterion is a better

method in detecting solder bump fails than two-point test on a daisy chain with 1000 ohm shift fail criterion.

2) Bumps located in the die corners are the most critical bumps in TCoB stress. Reduant design for the corner bumps can significantly improve product reliability performance.

3) Bump depopulation can degrade reliability and should be practiced with care to balance reliability and performance, especially for the bumps close to the critical bumps.

4) Decreasing die thickness and increasing bump size can improve solder joint reliability performance.

5) UBM to PCB Cu pad misalignment can cause early bump fails and should be avoided by improved assembly process or proper board design.

6) Board wiring traces connecting to solder directly in solder mask layer should be avoid. Moving traces below solder mask and connecting solder to Cu pad through via can significantly improve reliability performance.

WLCSP CPI is a complex interaction among die, interconnect and board. It is critical to conduct thorough test and analysis to understand the physics of the failure mechanisms. Based on the comprehension, co-optimization of design and process for chip, interconnect and board can be implemented to meet both RF performance and reliability requirements for 5G applications.

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