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Pad-Based CDM ESD Protection Methods Are Faulty

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ABSTRACT Charged device model (CDM) electrostatic discharge (ESD) protection remains a huge challenge for integrated circuit (IC) reliability designs. The "internal-oriented" CDM model and the "external-oriented" human body model (HBM) describe fundamentally different ESD phenomena. Through the comprehensive analysis, this article concludes that the classic pad-based ESD protection methods, commonly used for "from-external-to-internal" HBM ESD protection, are theoretically not working for "from-internal-to-external" CDM ESD protection. It states that the actual internal distribution of static charges within a chip is vitally critical to CDM ESD protection. The discovery explains the potential root cause of the randomness and uncertainty of pad-based CDM ESD protection designs commonly observed today, hence calls for new CDM ESD protection solutions.

INDEX TERMS ESD, CDM, HBM, SOI, SPICE.

I. INTRODUCTION

ESD failure is regarded as the most challenging reliability problem for ICs, which requires on-chip ESD protection for all ICs [1]–[6]. ESD phenomena are classified according to the origins, leading to various industrial ESD test standards, such as HBM, CDM and IEC [7]–[9]. These industrial ESD testing standards have been constantly evolving to accommodate the new understanding of ESD phenomena, especially for advanced IC technologies. Nowadays, as IC technology continues to scale down and chip complexity rapidly increases, CDM ESD protection emerges as a major IC reliability design challenge, particularly at sub-28nm nodes and for FinFET CMOS. Recognizing that a CDM ESD event is extremely fast compared to an HBM ESD event, the main research efforts in CDM ESD protection designs have been devoted to making CDM ESD devices faster. In practical designs, the classic pad-based HBM ESD protection approaches have been commonly used for CDM ESD protection. On the other hand, CDM ESD protection remains a black magic full of uncertainties today, being a huge headache to IC designers [10]–[12]. The commonly asked questions about CDM ESD protection are: Why are CDM ESD test results often not repeatable, reproducible and unreliable? Why does an IC still fail in CDM zapping in field although the chip passed the CDM test in production? Why does CDM ESD failure seem to be so random in field? In short, the fundamental question to ask is that, does the popular pad-based on-chip CDM ESD protection approach really work? Extended from the conference report, this article provides a thorough analysis that concludes that the classic pad-based CDM ESD protection methods are fundamentally faulty [13].

II. HBM ESD PROTECTION: FROM-EXTERNAL-TO-INTERNAL

HBM ESD is an "external-oriented" ESD phenomenon where electrostatic charges accumulated inside a human body will discharge into the IC core through an IC pad when touching the IC [1]. Fig. 1 depicts the transient HBM waveform, defined by the original MIL-STD-883E Standard, which is used to zap IC pads, and the HBM pulse flowing into the IC core may cause HBM ESD failures [7]. The ANSI/ESDA/JEDEC JS-001-2017 Standard provides details to build an HBM ESD tester to faithfully model the real-world HBM ESD events [8]. The key parameters for an HBM pulse are waveform rising time (t_r ~10ns) and decay

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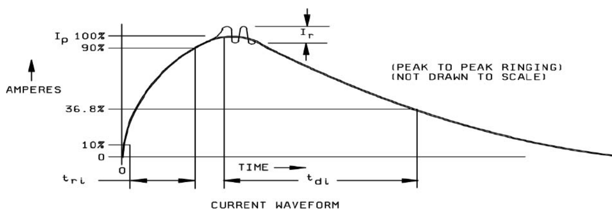


FIGURE 1. The HBM ESD waveform defined in [7].

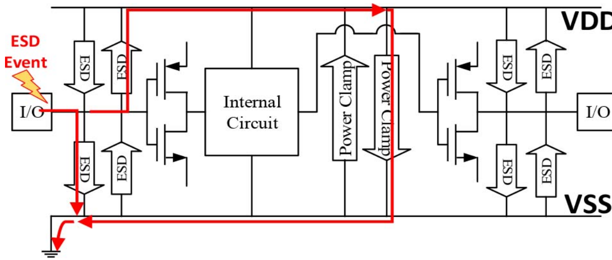
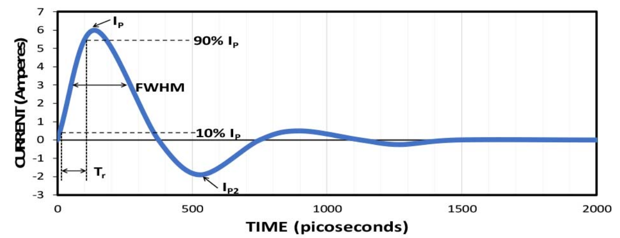
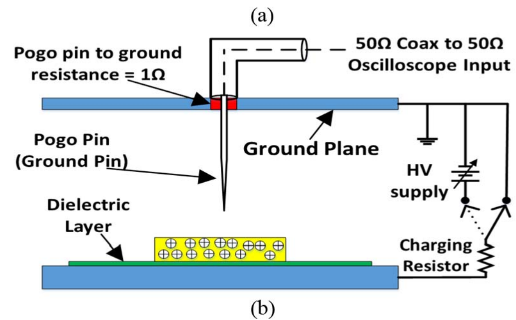


FIGURE 2. Classic pad-based full-chip ESD protection scheme relies on the ESD devices at pads to form low-R paths to discharge the incoming HBM ESD transients, i.e., blocking external alien charges from getting into the IC core. It works for any "from-external-to-internal" ESD events.



(a)



(b)

FIGURE 3. Illustration of the standard CDM ESD test model: (a) CDM ESD discharging waveform, and (b) FICDM CDM ESD test set-up.

time (t_d ~150ns). Fig. 2 depicts the classic pad-based on-chip HBM ESD protection method where ESD protection devices are placed at the IC pads (I/O, V_{DD}, V_{SS}, etc.), which will be turned on at ESD stressing to form low-R conduction paths to bypass the incoming HBM transients into ground. In principle, pad-based HBM ESD protection works in a way that the incoming alien charges from a human body are blocked by the ESD devices at the pads from getting into the IC core, hence, realizing ESD protection. HBM ESD protection requires careful design of the ESD-critical parameters including triggering voltage (V_{t1}), triggering time (t_1) and discharging resistance (R_{ON}) [1]. In theory, the pad-based ESD protection method is a "from-External-to-Internal" ESD protection method where the ESD devices at pads serve as the "guard" at the "gate" (i.e., pad) to defend against the "external-oriented" HBM ESD events, which, however, does not apply to the "internal-oriented" CDM ESD events.

III. CDM ESD PROTECTION: FROM-INTERNAL-TO-EXTERNAL

CDM ESD is an "internal-oriented" event in nature that is completely different from the "external-oriented" HBM event. CDM ESD is a self-charging/discharging ESD phenomenon where, in real world, an IC may be charged by various possible mechanisms, triboelectrically or field induction, during their lifetime. The induced electrostatic charges are stored inside the IC in a random and distributed way. When the IC is grounded, the static charges stored inside will discharge into the ground. The resulting strong and ultrafast CDM ESD transients flow from the IC core outward to the ground, resulting in CDM ESD failures [1]. Fig. 3 shows the waveform and test set-up per CDM ESD standards [9]. A CDM ESD pulse is ultra-fast and very short (t_r ~100ps, t_d ~2ns) compared to an HBM ESD pulse (t_r~10ns, t_d~150ns). The latest CDM ESD standard (ANSI/ESDA/JEDEC JS-002-2014) provides details for building a field-induction CDM (FICDM) ESD tester including two steps: 1) charge an IC part by field induction; 2) discharge the charged device, i.e., device under test (DUT), by using the pogo pin to touch the DUT to ground it. As such, the static charges stored inside the DUT will discharge into the ground, which is apparently an "internal-oriented", "from-internal-to-external" procedure, completed different from an "external-oriented", "from-external-to-internal" HBM ESD event. The sharp difference in nature for CDM and HBM ESD events suggests that their ESD protection methods shall be different too. However, the classic pad-based ESD protection methods have been commonly used for CDM ESD protection; while the main CDM ESD design effort has been devoted to making a CDM ESD device faster. We believe that the pad-based CDM ESD protection method is fundamentally faulty, which leads to the uncertainty and randomness of CDM ESD design failures that we observed today for the following reasons. First, since the problematic static charges (the "bad guys") are already staying inside an IC part, the ESD devices at pads lose their key function as the "guard" at gate, i.e., blocking the external alien charges from getting into the IC core as in an HBM ESD protection case. Second, theoretically, since the charges stored inside an IC must run through the IC core before being discharged into GND, it is highly possible that internal CDM damages may occur somewhere inside the IC core due to voltage or current build-up. Third, CDM failures depend on the internal current flow routing during CDM discharging, which is very sensitive to both the amount of static charge accumulated inside the IC and, critically, their internal distribution (i.e., location) within the IC core. Theoretically, the internal distribution of static charges can be anywhere, random and time-varying during the lifetime of

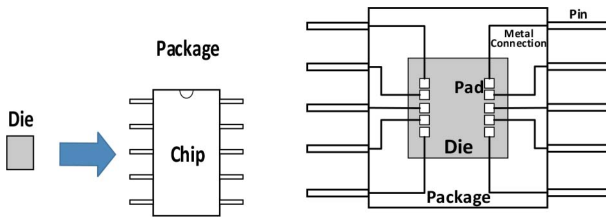


FIGURE 4. DUT's suffering from CDM ESD failures can be bare IC dies, packaged ICs or sub-system modules.

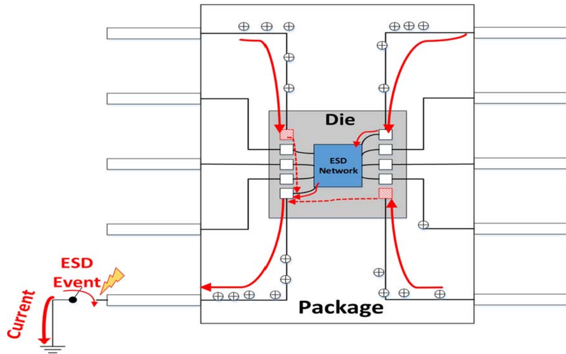


FIGURE 5. Ideally, a pad-based global ESD network for a packaged IC has ESD devices at all pads to ensure a low-R ESD discharge path between any two pads on a die. Red pads have missing ESD turn-on, forcing charges flowing into the IC die (dashed lines) and causing possible CDM failures.

an IC product. Fourth, the industrial standard FICDM is an accelerated "short" charge induction procedure, which does not faithfully represent the true CDM charging procedures in real world that is a "lifetime" problem. As such, the charges induced into the DUT device during the charging procedure using an FICDM-based CDM tester may not fully distribute throughout the IC chip as is in real world, hence, resulting in great variation in CDM ESD failures. Therefore, the FICDM CDM ESD testing method is over-simplified, which adds another major uncertainty to CDM ESD testing. In brief, the above analysis suggests that the classic pad-based CDM ESD protection method is fundamentally faulty, causing uncertainty of CDM ESD protection designs and random CDM ESD failures in field, which will be validated by case studies below.

IV. FAULTY PAD-BASED CDM ESD PROTECTION

As depicted in Fig. 4, in principle, CDM ESD failures can occur at any level: bare silicon dies, packaged ICs or system modules [2], [14]. Therefore, robust CDM ESD protection must be designed to protect ICs at any level. Classically, complete full-chip ESD protection requires a global ESD protection network consisting of ESD devices at every pad, so that there is always a low-R ESD discharging path between every two pads under ESD stressing [1]. This is the way to ensure full-chip ESD protection, which works well for "from-external-to-internal" HBM ESD protection. For a packaged IC, the global full-chip ESD protection network may exist on the chip as shown in Fig. 5 where the central ESD block depicts a pad-based ESD protection network

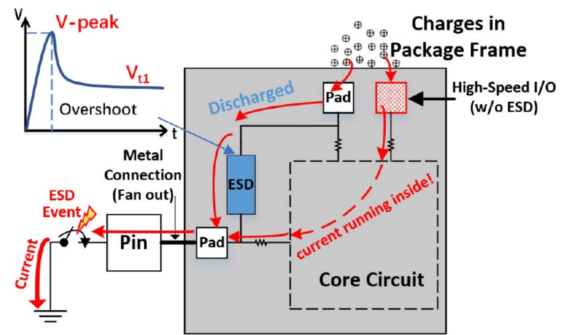


FIGURE 6. Often, data pads for high-frequency or high-speed links do not have ESD protection devices to avoid ESD-induced parasitic effects. Red pad missing ESD device, and forcing charges flowing into the core (dashed line) and causing possible CDM failures.

connected to all pads on a chip. For a CDM-charged packaged IC, the static charges are often considered to be stored on the package frame and/or on the power buses [10]. If so, under CDM ESD stressing, i.e., one package pin is suddenly grounded as depicted in Fig. 5, the stored charges on the package will, conceptually, always be able to find a way to discharge into the grounded pin, either directly through the package metal buses if located nearby, or, through the global ESD protection network connected to the pads on a chip, then discharge into the grounded pin. Either way, the charges stored on the package frame are external to the IC die. This means that, from the viewpoint of the IC die, a CDM ESD event for the packaged IC is similar to the "from-external-to-internal" HBM ESD event for the IC die inside the package. Therefore, the pad-based HBM ESD protection approach shall work, ideally, for the packaged IC in CDM ESD events. Unfortunately, real-world designs are never ideal. In one case, common in practical ESD designs, an ESD device may not be optimized in both directions for the ESD-critical parameters (t_1, V_{t1}, R_{ON}, etc.). Therefore, some ESD devices cannot be turned on in either forward or reverse direction. Since CDM ESD discharge in a packaged IC can be random, this means there are always situations where one or more ESD devices at pads in the global ESD network cannot be turned on in certain direction under the CDM ESD stressing. As a result, the charges stored randomly on a package frame will inevitably run into the internal core circuit, resulting in internal CDM ESD damage, even though the charges will eventually be discharged into the grounded package pin. This is almost unavoidable in practical designs. In a second case, for high frequency, wide bandwidth ICs or high data rate ICs, the signal pads are often not ESD-protected in order to avoid ESD-induced parasitic effects that will affect the high-speed IC performance, as shown in Fig. 6. In such cases, the global ESD protection network is incomplete. Hence, under CDM ESD stressing, there are always situations where the charges stored on the package frame will route into the internal core circuit on the way to package GND, resulting in CDM ESD damages to the core circuit. In summary, the classic pad-based CDM

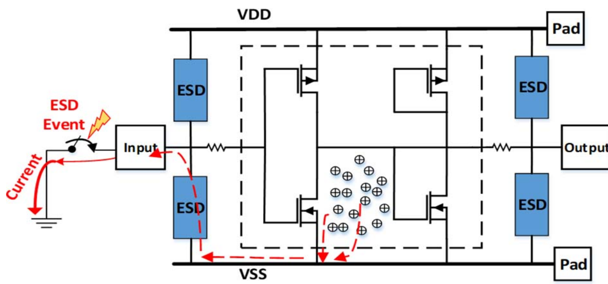


FIGURE 7. Illustration of using classic pad-based CDM ESD protection method to discharge the electrostatic charges randomly stored inside an IC die.

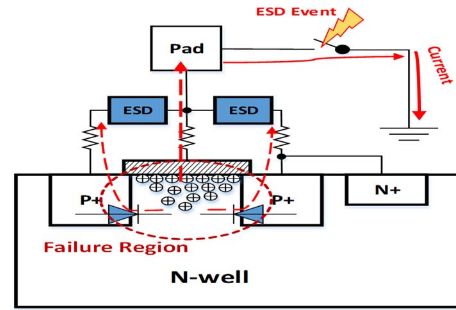


FIGURE 8. In a case when substantial static charges are stored locally to a MOSFET on a chip, under CDM ESD stressing, some charges will inevitably run through the S/D junction or the gate, resulting in CDM ESD damages regardless if pads are ESD-protected.

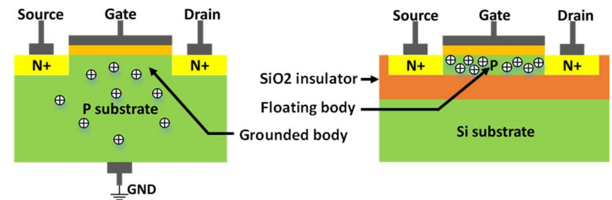


FIGURE 9. In an SOI IC die, static charges may be stored locally in a MOSFET that is completed isolated from the rest of the chip. Under CDM ESD stressing, these locally stored charges may cause gate ESD damage. (L) charges stored in a bulk MOSFET, and (R) charges stored in an SOI MOSFET.

ESD protection method, theoretically, will not work in many scenarios for packaged ICs.

Recently, CDM ESD failure to unpackaged bare IC dies becomes a major reliability concern, which is more devastating compared to packaged ICs. As depicted in Fig. 7, for a bare Si die, the charges induced by whatever procedures, are stored inside the IC die randomly, unpredictably and anywhere, e.g., in the substrate, along the metal rails or locally to transistors [2], [14]. Using the classic pad-based ESD protection method, as shown in Fig. 7, simply will not provide CDM ESD protection for the bare IC die. In the case where the charges are stored nearby the GND pad (e.g., V_{SS}), it is possible that the charges may be discharged safely into the nearby ground through the ESD device at a close-by pad. Unfortunately, such an ideal case would be in dream only. For a large and complex chip, the chance is that substantial charges are distributed everywhere randomly on a die that must find their way out to the grounded pad under CDM ESD stressing. Therefore, the charges will flow throughout the internal IC die before discharging into GND, randomly and unpredictably. This means that internal CDM ESD damages will occur even if the pad-based global ESD network would function properly. Even if the pad-based ESD devices were designed perfectly and verified individually by CDM ESD testing, it likely will not provide CDM ESD protection as expected on a chip. Fig. 8 shows a case where, during a CDM event, the locally stored charges may be capacitively coupled through the gate to a pad when discharging, inevitably causing CDM ESD damage to the gate. Similar CDM ESD failures were reported for 14nm FinFET design, which failed CDM test at low CDM stress (<100V) and the ESD failure was attributed to electrical overstress to the metal gate during CDM stress [12]. The random CDM ESD failure becomes even worse for SOI chips where each MOSFET is isolated from the rest of the circuit. Consequently, as shown in Fig. 9, the CDM induced charges are likely stored and confined locally to a MOSFET, which will most likely run through the local gate during discharging and cause gate damage even if all pads are ESD-protected by design. From the above analysis, we believe that the classic pad-based ESD protection method, while working nicely for "from-external-to-internal" HBM ESD events by blocking external charges from getting into the core circuit through pads, it, in principle, will not protect ICs against "from-internal-to-external" CDM ESD stressing. This discovery likely explains why CDM ESD design is still a black magic full of uncertainty, and the "luck" makes CDM ESD designs essentially unpredictable and unreproducible today.

V. FAULTY CDM ESD PROTECTION BY CIRCUIT ANALYSIS

The validation was conducted by circuit analysis using a 3-stage oscillator IC designed in a foundry 45nm SOI CMOS as shown in Fig. 10, which uses the classic pad-based ESD protection scheme for CDM ESD protection where the three pads, VDD, VSS and cko (Output), are protected by diode ESD devices. Per the foundry Design Rules, we chose the ESD diodes with a total finger width of 360μm for the targeted 500V CDM ESD protection (10A). SPICE circuit simulation was conducted for three CDM ESD testing scenarios for comparison.

A. NEW PSEUDO-DISTRIBUTED FICDM ESD TEST MODEL

Fig. 11 depicts the lumped equivalent circuit model for the commonly used FICDM test setup by ANSI/ESDA/JEDEC JS-002-2014 Standard [9], where C_{DUT} is the capacitance between the DUT and the induction field plate, C_{DG} is the capacitance between the DUT and the discharge ground plate and C_{FG} is the capacitance between the field plate and the ground plate. From the previous discussion, the over-simplified FICDM tester circuit model fails to accurately model the real-world CDM events because the lumped capacitance circuit simply cannot reflect the full distribution nature of the CDM charge storage inside a DUT IC, hence, leading

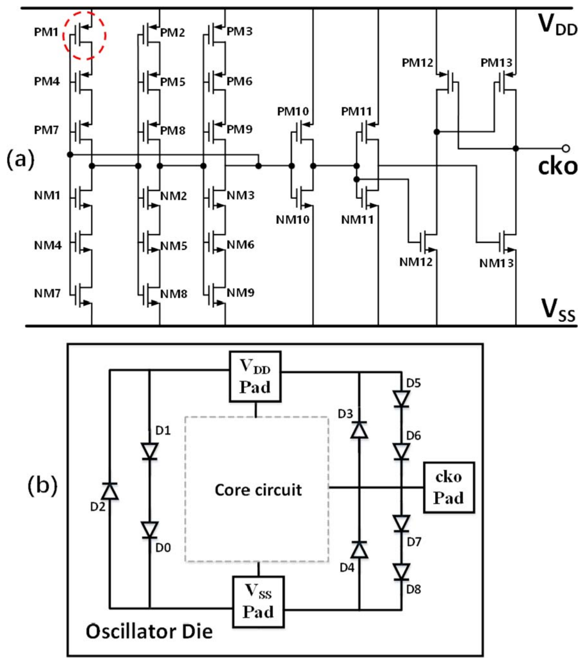


FIGURE 10. A 3-stage oscillator designed in 45nm SOI in this study is protected by traditional pad-based CDM ESD protection scheme: (a) circuit schematic, (b) IC die diagram including core schematic and ESD network.

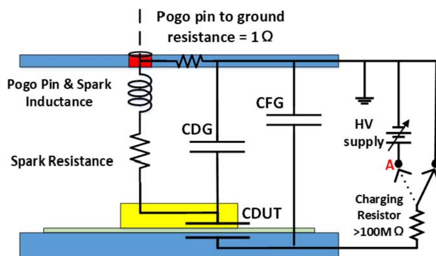


FIGURE 11. A simplified FICDM tester circuit schematic [9].

to major CDM testing uncertainties in field. To address this problem, we propose a new pseudo-distributed equivalent circuit model for an enhanced FICDM-like CDM test setup as depicted in Fig. 12. In the new model, C_{DG} is considered as a distributed capacitor net (C_{DG1}, C_{DG2}, ... C_{DGx}) across all IC pads, which, in first order approximation, may be equal for each pad assuming all pads are same. C_{DUT} is decomposed into two parts: C_{die-FP} for the capacitance from die substrate to field plate and C_{DF} for the capacitance from each pad to the field plate, which comprises a distributed capacitor net (C_{DF1}, C_{DF2}, ... C_{DFx}) across all package pads. C_{die-FP} can be estimated per the IC die area with respect to the size of the small calibration metal disc of an FICDM tester. C_{DF1}, C_{DF2}, ... C_{DGx} are considered equal for each pad. For the 3-pad oscillator IC designed within a 2mm x 2mm die in 45nm SOI CMOS in this study, the estimated values are: $C_{DG1,2,3} \approx 0.61$pF, $C_{DF1,2,3} \approx 2.114$pF, $C_{die\text{-}FP} \approx 0.437$pF and $C_{FG} \approx 17.0$pF. We call it a pseudo-distributed FICDM test model because the capacitor networks are largely depending upon how fine the grid is for the capacitor mesh

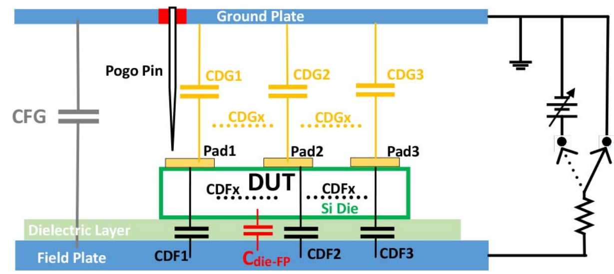


FIGURE 12. Our new pseudo-distributed circuit model for FICDM tester.

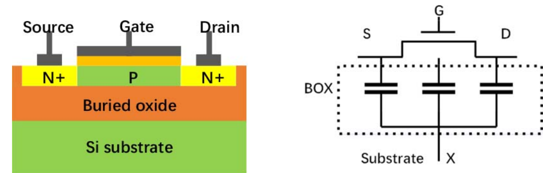


FIGURE 13. A MOSFET in 45nm SOI CMOS: cross-section and BOX/substrate model with X node being the substrate.

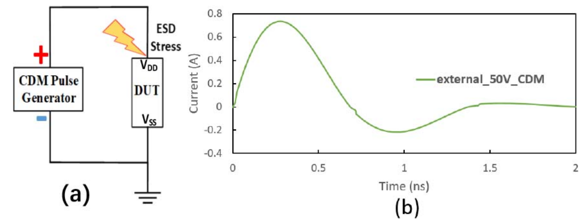


FIGURE 14. Scenario-1 HBM-like CDM ESD stressing where an external CDM pulse is applied to the DUT (oscillator IC die) by zapping the V_{DD} pad with respect to the V_{SS} pad (GND): (a) schematic, and (b) CDM zapping waveform used per CDM standard.

associated with the DUT; nevertheless, it is a much-improved model over the lumped FICDM test model commonly used. Fig. 13 depicts a MOSFET in 45nm SOI where capacitance associated with the buried oxide (BOX) layer and the substrate node “X” are included in the foundry PDK, hence avoiding extra effort needed to model it [15].

B. SCENARIO-1: EXTERNAL-ORIENTED CDM ESD ZAPPING

Three CDM ESD discharge scenarios were studied for the oscillator IC designed in 45nm SOI. Depicted in Fig. 14, Scenario-1 models HBM-like CDM ESD zapping method where a fast CDM pulse, defined by CDM ESD test model [9], is used to zap the oscillator IC die, similar to very-fast transmission-line pulsing (VFTLP) testing (i.e., from-external-to-internal stressing) to emulate CDM zapping [1]. In all scenarios, the VDD pad was zapped. CDM ESD stimuli of varying levels (voltage and current) are used to zap the DUT IC die. The simple ESD failure criterion used in this study is the gate voltage breakdown ($|V_{GS}|$ or $|V_{GD}|$) of any MOSFET, which is $BV_{OX} \sim 6.5$V, during the CDM pulse period of 2ns. Fig. 15 depicts the transient CDM discharging voltage waveforms by SPICE for an exemplar MOSFET PM1, which shows that, under both 500V and 50V CDM zapping, no CDM-induced MOSFET

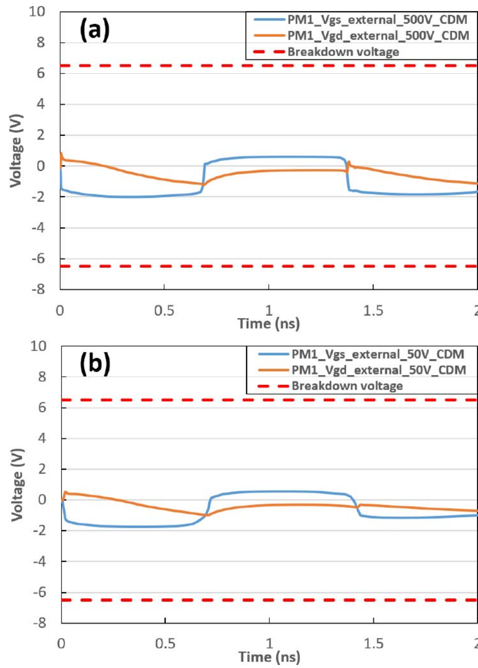


FIGURE 15. Exemplary transient voltage analysis for V_{GS} and V_{GD} of PM1 of the oscillator IC under Scenario-1 CDM zapping: (a) 500V CDM stressing, and (b) 50V CDM stressing.

TABLE 1. Summary of peak $|V_{GS}|$ and $|V_{GD}|$ of PM1 under CDM zapping.

Scenario-1 External-Oriented CDM Zapping				
	50V CDM	100V CDM	250V CDM	500V CDM
Max $|V_{GS}|$&$|V_{GD}|$ (V)	1.76	1.82	1.91	2.02
Scenario-2 Internal-Oriented Lumped FICDM Zapping				
	25V CDM	50V CDM	75V CDM	100V CDM
Max $|V_{GS}|$&$|V_{GD}|$ (V)	4.51	7.44	8.04	8.21

breakdown occurs. Table 1 summarizes the maximum V_{GS} and V_{GD} of PM1 under CDM zapping, showing that the peak transient V_{GS} and V_{GD} increased slightly as CDM increases from 50V to 500V, meaning the pad-based ESD protection works well in defending against external-oriented ESD stressing. Fig. 16 shows more details on the CDM discharging behaviours under the 50V V_{DD}-to-V_{SS} CDM zapping. It is observed that, due to CDM discharging waveform oscillation, two CDM discharge paths are turned on alternatively: D1+D0 path during the positive cycle, and D2 path during the negative cycle, each taking almost the full load of CDM discharging current during its functional cycle. CDM discharging current flowing into the IC core is negligible, hence provides CDM ESD protection.

C. SCENARIO-2: ENHANCED FICDM ESD ZAPPING

Scenario-2 models from-internal-to-external FICDM ESD zapping (Fig. 12), where the DUT IC die is charged by induction and then discharges by grounding the V_{DD} pad. Fig. 17 depicts the FICDM ESD simulation schematic deck where "GND" and "Field" represent the ground plate and

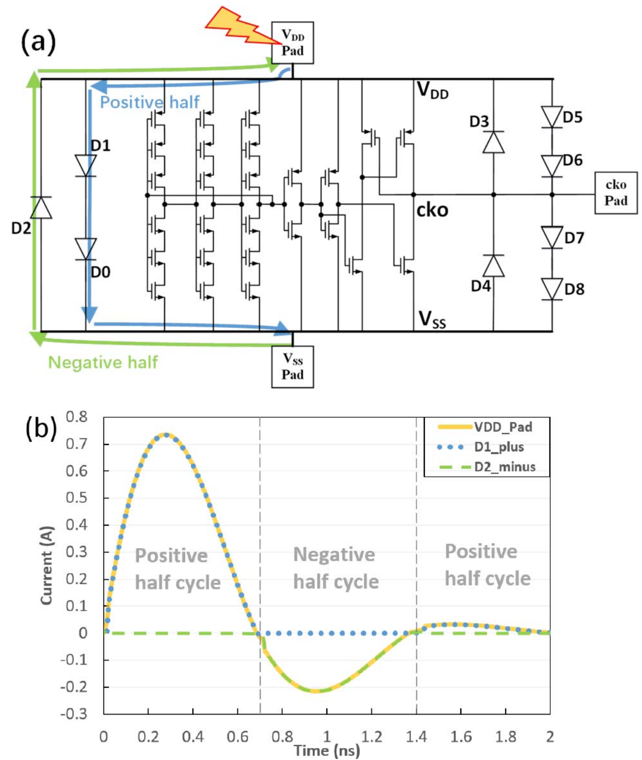


FIGURE 16. CDM ESD stressing Scenario-1 using an external 50V CDM pulse to zap V_{DD} pad w.r.t. VSS pad: (a) CDM ESD discharge paths, and (b) transient CDM current waveforms.

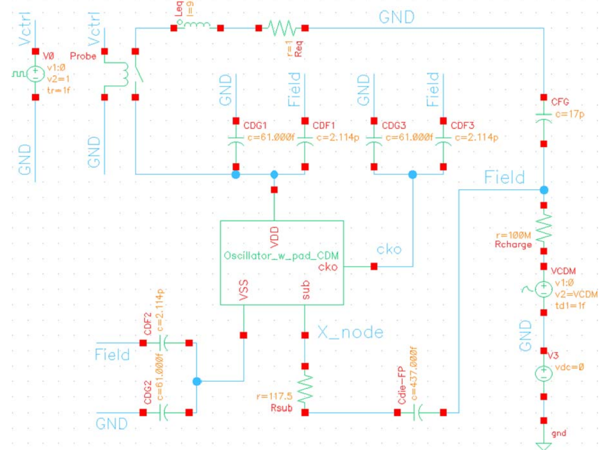


FIGURE 17. A schematic deck used in Scenarios-2/3 to simulate the oscillator under CDM ESD stressing due to internal charges where "V_{DD}" padis zapped.

field plate, respectively, and "sub" is the "X" node of MOSFET. A voltage-controlled switch models the spark as the pogo pin approaches DUT pad. Voltage source V_{CDM} is the FICDM charging voltage. Voltage source V_0 controls the switch to trigger CDM discharging. Fig. 18 depicts the transient CDM discharge voltage waveforms by SPICE for exemplar MOSFET PM1 under FICDM zapping with the extracted maximum transient V_{GS} and V_{GD} of PM1 listed in Table 1. It is observed that CDM failure occurs to some

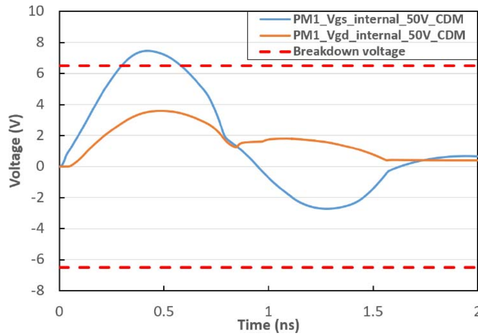


FIGURE 18. Exemplary transient voltage analysis for V_{GS} and V_{GD} of PM1 of oscillator IC under Scenario-2 CDM zapping by the 50V CDM pulse.

MOSFETs, e.g., V_{GS} breakdown at PM1. Fig. 19 shows more details on the CDM discharging behaviours under the 50V FICDM zapping at V_{DD} pad. It is observed that, due to CDM discharging waveform oscillation, four CDM discharge paths are turned on alternatively: D1 + D0 path (V_{DD} to V_{SS}) and D5+D6 path (V_{DD} to cko) during the positive cycle, and D2 path (V_{SS} to V_{DD}) and D3 path (cko to V_{DD}) during the negative cycle, respectively, together taking the full load of CDM discharging current during their functional cycles. This is sharply different from Scenario-1 where the external CDM pulse zapping the V_{DD} pad can be readily discharged via one path starting from the zapping node (V_{DD}). However, in Scenario-2, due to the distributed nature of internal charge storage, the static charges may stay anywhere inside the IC core. Specifically, the charges accumulated near both V_{SS} pad and cko pad will find different paths to discharge. Consequently, the discharging currents running through the different paths within the chip caused internal CDM failure at ~50V stressing level. Apparently, the "from-external-to-internal" CDM zapping method over-evaluated the ESD capability (passed ~500V), while the "from-internal-to-external" FICDM zapping shows internal CDM failures at a much lower stressing level (failed ~50V). It is important to understand that, without considering the charges stored inside the IC die that can be modelled using a distributed inside-die capacitor mesh (i.e., Scenario-3), even the enhanced FICDM model is still equivalent to an "external-oriented" CDM zapping to the IC die. Further and critically, since the internal distribution of static charges inside an IC core may be random during its lifetime, the actual field CDM failure can be unpredictable regardless of the in-house test results from the existing FICDM test method. Here arises the key question: how good and useful is the FICDM ESD test method?!

D. SCENARIO-3: DISTRIBUTED REAL-WORLD CDM ESD ZAPPING

Scenario-3 is a new model proposed to, ideally, accurately describe the real-world CDM ESD phenomena, i.e., the charges accumulated inside an IC device, by whatever way during its lifetime, may be randomly distributed throughout

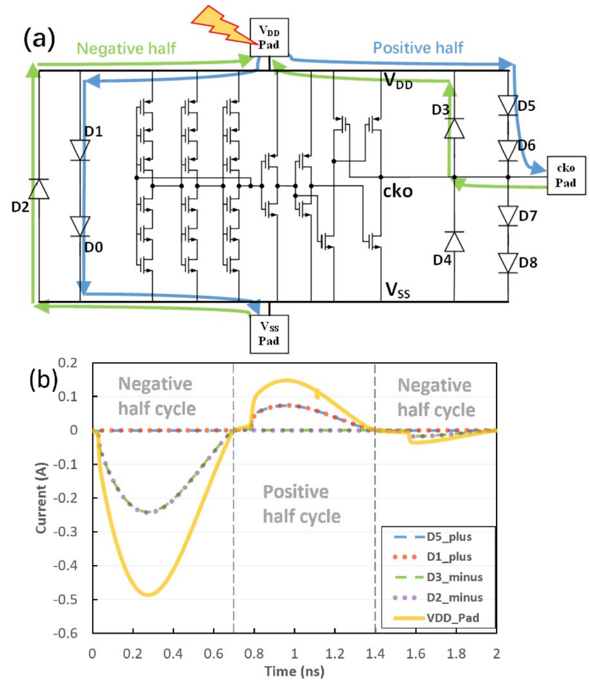


FIGURE 19. CDM ESD stressing Scenario-2 where V_{DD} pad is zapped by a CDM pulse from internal charges per FICDM model: (a) CDM discharge paths, and (b) transient CDM current waveforms.

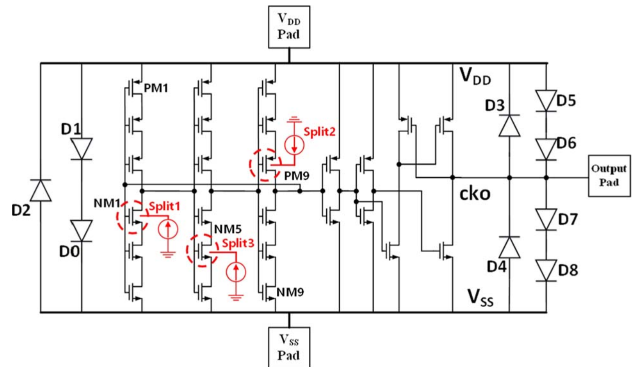


FIGURE 20. Scenario-3 internal-oriented CDM ESD stressing schematic deck where V_{DD} pad is zapped by internally generated CDM pulses from internal charges accumulated locally to NM1 (Split 1), PM9 (Split 2) and NM5 (Split 3).

the whole chip, which cannot be modelled by the over-simplified lumped FICDM model. The internally distributed charges can be modelled by a distributed capacitor mesh network within the IC die. Fig. 20 depicts the near-real-world CDM ESD discharging simulation schematic deck. Assume that the internal static charges may be distributed randomly, we designed three Splits to simulate three simple, yet representative CDM discharge cases: each assuming substantial charges are stored locally at MOSFET NM1, PM9 & NM5. We expect different internal CDM discharging routes for each Split. During the simulation, CDM current pulses (stimuli) of varying strengths are studied, reflecting varying charge distribution inside the IC chip. Fig. 21 depicts the transient voltage behaviours of exemplar MOSFETs under CDM

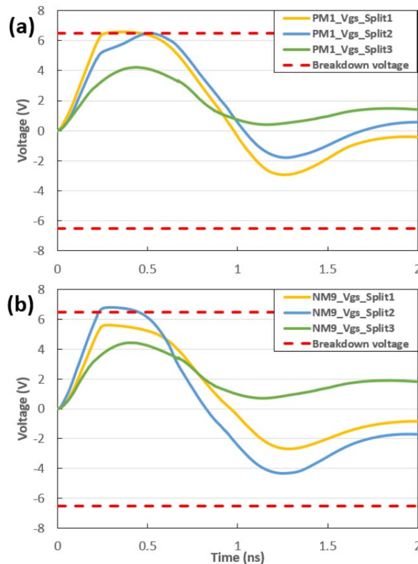


FIGURE 21. Transient ESD discharge voltage waveform analysis for the oscillator IC die in Scenario-3 under internal-distributed CDM zapping to V_{DD} pad. The local CDM zapping strength is equivalent to ∼1% of that for lumped FICDM zapping in Scenario-2; however, internal CDM failures (gate breakdown) occur at varying locations in the three internal zapping splits: (a) MOSFET PM1, and (b) MOSFET NM9.

stressing originated from different internal charge storage distribution cases when the local CDM zapping strength is equivalent roughly to 1% of that under FICDM stressing in Scenario-2. It is readily observed that CDM-induced voltage breakdown failure occurs to different MOSFETs depending on the storage locations of the internal charges, i.e., Split 1 (PM1 gate), Split 2 (PM1 gate and NM9 gate) and Split 3 (none). In addition to fully illustrating the varying CDM failures caused by random distribution of internal charges within a chip, the observed CDM failure level is much lower than that in Scenario-2, roughly ∼1% of the CDM stressing level in our examples. This study clearly shows that CDM failure is closely related to the internal distribution of the charges accumulated inside an IC die and the lumped FICDM test model is over-simplified. It shows that, for the oscillator IC die with all pads protected by ESD devices, the new internal-distributed CDM zapping model predicts internal CDM failures occurring at much lower ESD level than that predicted by using the lumped FICDM zapping model. Therefore, the classic pad-based CDM ESD protection method is fundamentally faulty. A novel CDM protection method is being explored currently. We proposed a new internally distributed CDM ESD protection method as a disruptive solution that is under development. The basic idea is that an IC die can be smartly partitioned to reflect the distributed nature of internal charge storage and ESD devices of smaller footprints will be placed at selected internal circuit nodes per the smart portioning. Therefore, as static charges are generated and accumulated internally and locally, and when reaching to a given local potential threshold, the local ESD device will be triggered to discharge the static charges locally. Therefore, the new internally distributed ESD mesh network can provide adequate whole-chip CDM ESD protection, efficiently addressing the "from-internal-to-external" CDM ESD events by a novel "internal-oriented" ESD discharge mechanism.

VI. CONCLUSION

CDM ESD protection is a challenging design problem, which has been notoriously unpredictable, unproducible and unreliable in field. Validated by analysing an oscillator IC designed in a foundry 45nm SOI CMOS, this comprehensive study found that the magic uncertainty of CDM ESD protection is closely related to the somewhat random internal distribution of the electrostatic charges accumulated inside IC chips during their life time, which cannot be accurately modelled by the over-simplified lumped FICDM CDM test method. It concludes that the classic pad-based ESD protection method, working nicely for the "external-oriented", "from-external-to-internal" HBM CDM protection, is fundamentally faulty for "internal-oriented", "from-internal-to-external" CDM ESD events. It hence calls for new revolutionary on-chip CDM ESD protection solutions and more accurate CDM test models.

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