Received 17 June 2020; revised 12 August 2020; accepted 3 September 2020. Date of publication 8 September 2020;
date of current version 4 November 2020. The review of this article was arranged by Editor J. Rajendran.

Digital Object Identifier 10.1109/JEDS.2020.3022711

Subthreshold Operation of Photodiode-Gated Transistors Enabling High-Gain Optical Sensing and Imaging Applications

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This work was supported in part by the National Key Research and Development Program of China under Grant 2016YFA0202002, and in part by the National Natural Science Foundation of China under Grant 6147403.

ABSTRACT In optical sensors and imagers, high gain that leads to high sensitivity and high signal to noise ratio (SNR) is often desirable. One popular approach is avalanche photomultiplication initiated by impact ionization in an avalanche photodiode or similar devices and the other approach is active pixel sensor (APS) with in-pixel amplifier. However, the former requires high electric field which induces high shot noise and the latter needs a multiple-transistor pixel circuit which compromises the fill factor and consequently, reduces the SNR. This work proposes and summarizes our recent efforts taken to achieve high gain optical sensors through subthreshold operation of photodiode-gated transistors.

INDEX TERMS High gain, photodiode-gated transistors, active pixel sensor, subthreshold operation.

I. INTRODUCTION

In optical sensing and imaging applications, in order to improve sensitivity and SNR, an APS including a photodetector, generally a photodiode, and several transistors forming a multi-component circuit has been designed where an in-pixel amplifier, also called a source follower, must be used. Since its birth, the APS has been evolved from three-transistor-circuit to five-transistor circuit in order to resolve issues such as blooming and reset noise. In addition to the APS, high sensitivity can be also obtained in an avalanche photodiode (APD) and its relative: silicon photomultiplier (SiPM). However, since high electric field has to be employed in order to initiate photomultiplication and impact ionization, high-field-induced shot noise is severe in these devices.

Very recently, a device concept of a subthreshold-operated photodiode (PD)-gated transistor was proposed. It achieves high gain with neither high field nor multi-transistor circuit. The gain derives from light-induced gate-modulation effect and to enable this, subthreshold operation must be conducted. It also vertically integrates a PD with a transistor in a compact one-transistor (1-T) APS format, leading to high spatial resolution. Such a device concept has been implemented in a variety of material systems, making it a viable alternative technology for high gain optical sensors.

II. VARIOUS HIGH GAIN SENSOR DESIGNS

A. PHOTODIODE-GATED AMORPHOUS SILICON THIN-FILM TRANSISTOR (TFT)

Large area optical sensors and imagers based on TFTs have been found in a wide range of applications such as flat-panel X-ray imaging, optical fingerprint scanning, and biomedical fluorescent imaging. A traditional passive pixel sensor (PPS) based on lateral integration of an amorphous silicon (a-Si:H) PIN photodiode and an a-Si:H readout/switch TFT suffers from low SNR and limited spatial resolution and is also incapable of correlated double sampling (CDS) for noise removal. To improve the SNR and enable the CDS, the APS with an in-pixel amplifier was used where a PD and multiple TFTs were packed into one pixel. However, the multi-TFT APS inevitably trades high SNR off against high spatial resolution and high fill factor due to large process critical

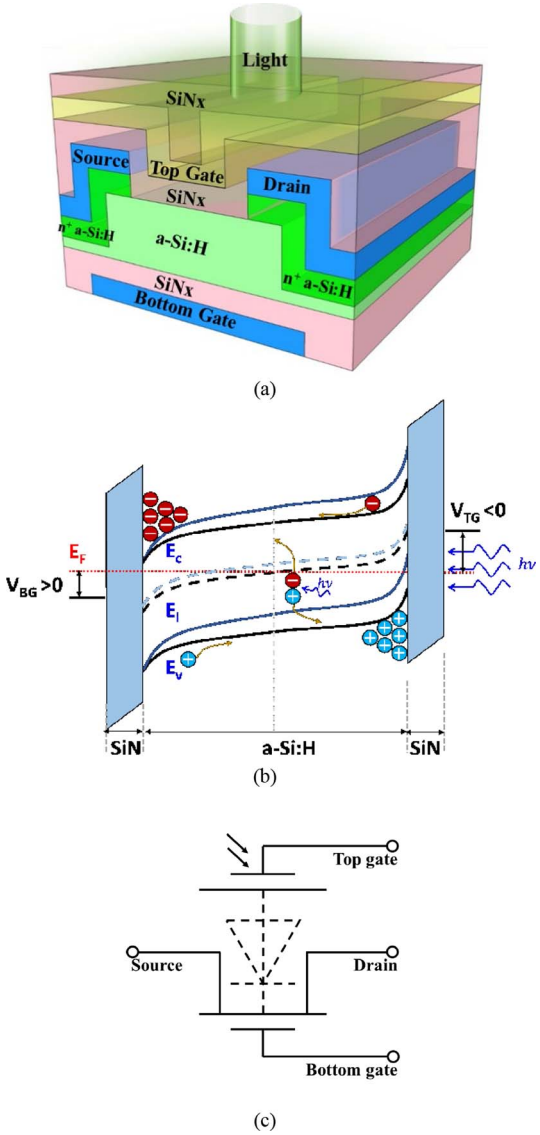

FIGURE 1. **(a) Schematic diagram of dual-gate 3-D photosensitive a-Si:H TFT [4]; (b) Energy band diagram of the dual-gate TFT where top gate (TG) and bottom gate (BG) were biased to create an embedded photodiode; (c) Equivalent circuit of 3-D dual-gate photosensitive TFT.**

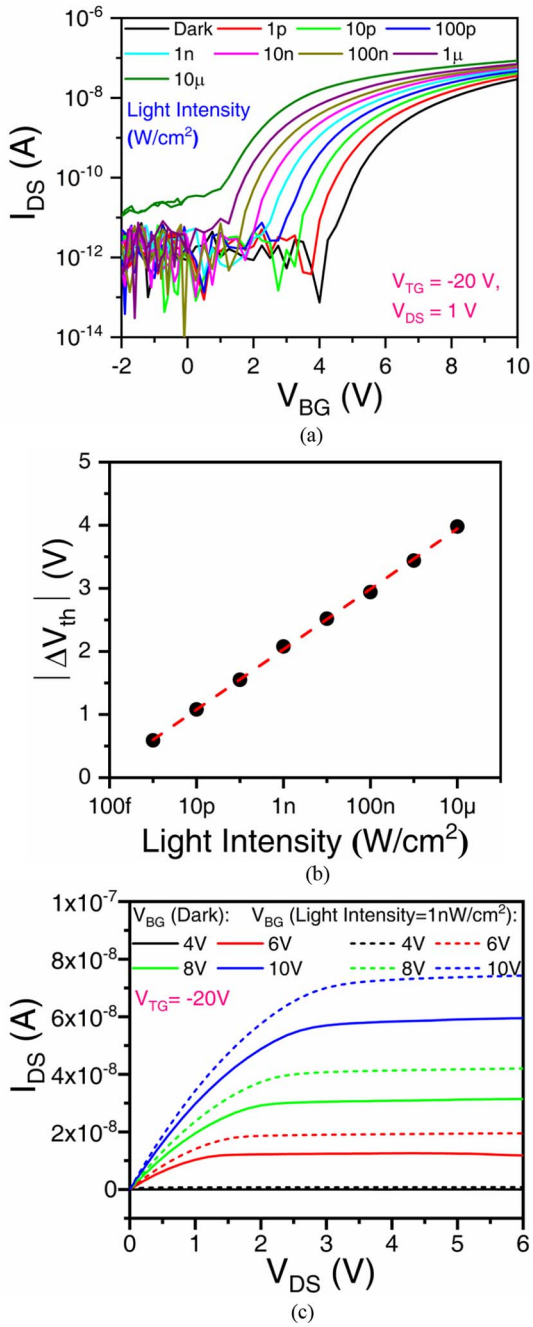

FIGURE 2. **(a) Simulated photo transfer characteristics upon light intensity from 0 to 10μW/cm² (W/L = 200μm/30μm); (b) Extracted threshold voltage change (ΔV_{th}) as a function of light intensity; (c) Output characteristics with and without light exposure.**

dimension [1]–[3]. To resolve this tradeoff, we have proposed a vertical three-dimensional (3-D) sensor architecture to form a 1-T APS that attains high SNR and spatial resolution [4]. As shown in Fig. 1, the schematic device structure of 1-T APS is formed by an a-Si:H dual-gate photosensitive TFT with a 3-D π-shape channel, the energy band diagram, and the equivalent circuit. As can be seen from the energy band diagram, an external-voltage-induced electric field is generated due to energy band bending. Under light illumination, the photogenerated electron-hole pairs are separated, then electrons and holes will be accumulated at bottom and top interfaces of the TFT, respectively. Thus, an embedded PIN-type photodiode is readily created and will bias the bottom TFT from the back gate. Therefore, upon light exposure, the threshold voltage due to gate-modulation effect will drop. Accordingly, the output photocurrent will increase exponentially in the subthreshold region. Fig. 2 presents the simulated transfer characteristics and its threshold voltage variation as a function of light intensity. As can be seen, the output photocurrent increases with decrease of the threshold voltage. The simulated output characteristics with and without light exposure is illustrated in Fig. 2 (c), where the output current elevates in response to the decrease of the light-induced threshold voltage.

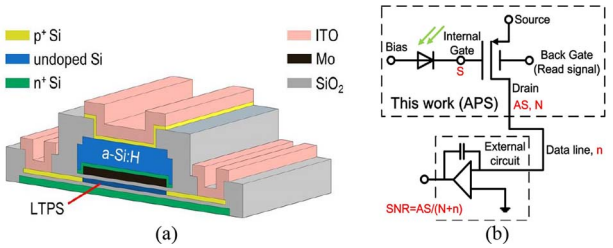

FIGURE 3. **(a) Schematic structure of a-Si:H photodiode-gated LTPS TFT [5]; (b) Equivalent circuit diagram, showing APS with high SNR [5].**

B. PHOTODIODE-GATED LOW-TEMPERATURE POLYCRYSTALLINE SILICON TFT (LTPS TFT)

Similarly, we adopted such a device concept in an a-Si:H PD-gated p-LTPS TFT and studied its optoelectronic behavior. Making a similar 3-D sensor structure is impossible due to process integration challenge, thus, a PIN-type photodiode is vertically stacked with the top gate of the p-LTPS TFT as shown in Fig. 3 (a). Such a vertical stack leads to a high fill factor and more important, the output photocurrent increases exponentially as the photo-induced threshold voltage decreases. It also acts as a 1-T APS as shown in Fig. 3 (b). The CDS can be realized through biasing the four terminals of Bias, Source, Back Gate and Drain of this integrated device. The detailed discussion of its operation and device physics can be found in [5]. Fig. 4 (a) gives the simulated photo-induced top gate voltage change (ΔV_{TG}) as a function of light intensity. Since V_{TG} is actually converted from the photogenerated charges through the top TFT capacitor, its value will be linearly proportional to the light intensity. The charge-to-voltage conversion gain is therefore governed by the top capacitance of the LTPS TFT and its dynamic range is determined by the PD. High gain and wide dynamic range can be optimized by properly co-designing the TFT and the PD. The back gate is used to tune the LTPS TFT into the subthreshold region where the high gain is achieved. The output photocurrent (I_{Photo}) will be an exponential function of light intensity. Fig. 4 (b) shows such trends at various exposure times.

C. PHOTODIODE-BODY-BIASED MOSFET

Even though, the concept of PD-gated transistors has been demonstrated in the above thin-film material systems. Optical sensors and imagers made by monocrystalline silicon with high gain, high speed and wide dynamic range are more desirable and preferable. A lot of potential applications such as photon counting, event camera, and molecular imaging can be expected where currently APDs and SiPMs are being employed. As discussed previously, the vertically-stacked 3-D dual-gate photosensitive TFTs based on non-crystalline silicon materials can obtain high gain, their photo-response speed is rather slow compared with crystalline silicon counterparts. We reported a crystalline-silicon-based optical sensor with high gain, high speed and wide dynamic range [6]. Different from the dual-gate TFTs, the realization

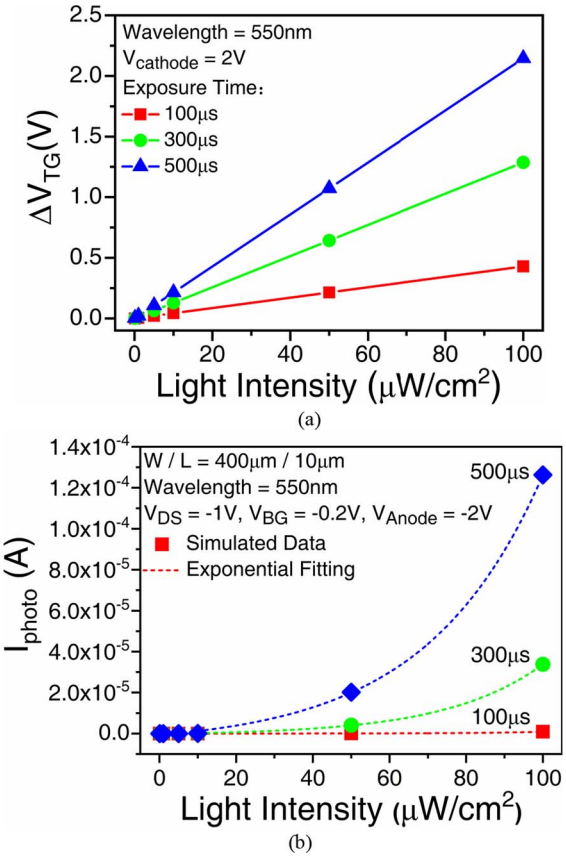

FIGURE 4. **(a) Simulated photo-induced top gate voltage change (ΔV_{TG}) with light intensity; (b) Simulated and exponential results of subthreshold output photocurrent under light exposure with different time duration.**

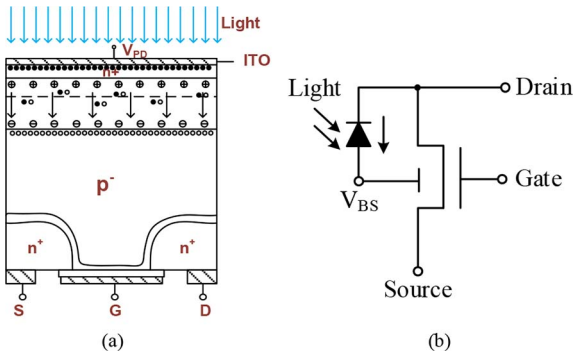

FIGURE 5. **(a) Schematic diagram of PD-body-biased MOSFET where PD is located atop a back side illuminated substrate; (b) Equivalent circuit of the PD-body-biased MOSFET with MOSFET drain connected with PD cathode, V_{PD}.**

of photodiode-gated dual-gate structure in a MOSFET is extremely difficult due to process and integration limitation. Fortunately, body bias in a MOSFET is sometimes used for modulating the threshold voltage. The threshold-modulation mechanism using a photodiode-body-biased MOSFET was then proposed instead of dual-gate configuration in the TFTs. Fig. 5 plots the schematic diagram of the photodiode-body-biased MOSFET and its equivalent circuit. Such a structure is well suited for back side illuminated CMOS image sensor

manufacture where both sides of silicon wafer are processed. The first body bias effect is to modulate the threshold voltage and the second body bias effect is to bias the parasitic drain-substrate-source ($n^+p^-n^+$ bipolar junction transistor (BJT)) in which case the device is like a PD-biased phototransistor. Thus, if the MOSFET works in the OFF-current region, the photocurrent of the PD provides the bias current to the BJT and the output photocurrent of the MOSFET (I_{DS}) is equal to the collector current and then given by:

$$I_{DS} = \beta I_{PD} = \beta I_S\left[\exp\left(\frac{qV_{BS}}{kT}\right) - 1\right], \tag{1}$$

where β is the amplification factor of the BJT, q is the electron charge, k is the Boltzmann's constant, T is absolute temperature, V_{BS} is the photo-induced body bias, I_S is the reverse-bias saturation current and I_{PD} is the photocurrent of the PD which can be written as:

$$I_{PD} = \frac{dQ_L}{dt} = q\eta A(1-R)\left(1 - e^{-\alpha d}\right) \cdot \frac{\Phi_\lambda}{h\nu}, \tag{2}$$

Q_L is the photogenerated charges, t is the time, η and A are the internal quantum efficiency and the area of the PD, respectively, R is the reflectance loss, α is the absorption coefficient of silicon, d is the depletion depth of the PD, Φ_λ is the incident light intensity, and $h\nu$ is the photon energy. The V_{BS} can be then described as follows:

$$V_{BS} = \frac{kT}{q} \cdot \mathrm{In}\left(1 + \frac{I_{PD}}{I_S}\right), \tag{3}$$

examining both (2) and (3), we can conclude that the body bias will be a quasi-logarithmic function of the light intensity.

When the V_{GS} biases the MOSFET into the subthreshold region, the first body bias effect starts to play a major role and the output current will further evaluate with the light-induced decrease of the threshold voltage. The subthreshold output photocurrent (I'_{DS}) follows [6]:

$$I'_{DS} = \mu_N C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 \exp \times \left[\left(\frac{V_{GS} - V_{T0} - \gamma\left(\sqrt{2\phi_{fp}} - \sqrt{2\phi_{fp} - V_{BS}}\right)}{nkT/q}\right)\right] \bullet\left[1 - \exp\left(\frac{-V_{DS}}{\varphi_t}\right)\right], \tag{4}$$

where μ_N is the field-effect mobility of the MOSFET, C_{ox} is the gate capacitance, W and L are the channel width and length, respectively, γ is termed as the body-effect coefficient, V_{T0} is the threshold voltage with body bias at zero volt, ϕ_{fp} is the surface potential, and the inverse slope of the sub-threshold current, n is related to the sub-threshold swing as $S = n \cdot \ln 10 \cdot (kT/q)$. Furthermore, the device simulation was implemented by Silvaco TCAD, and the corresponding parameters can be found in [6]. Fig. 6 (a) plots simulated photo transfer characteristics with light intensity various from 1n to 1W/cm^2. The light-induced positive body-bias makes the threshold voltage decrease and the output photocurrent increase. The negative shift of transfer characteristics indicates that the threshold voltage drops.

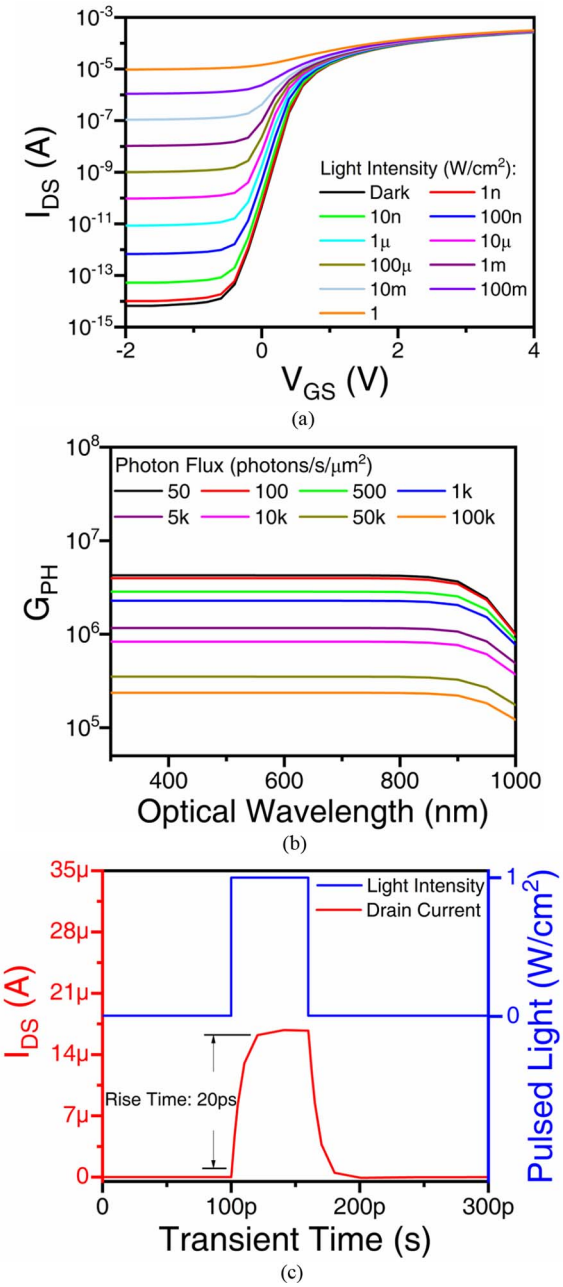

FIGURE 6. (a) Simulated photo transfer characteristics of PD-body-biased MOSFET with W/L = 5μm / 2μm; (b) Simulated G_{PH} in the subthreshold region (V_{GS} = 0.2V) at various photon fluxes; (c) Photoresponse of pulsed light with 60ps width. The rise time is about 20ps.

High photoconductive gain (G_{PH}) of $10^5 \sim 10^7$ is achieved with various photon fluxes and high gain covers the entire studied spectrum of 300 $\sim$ 1100 nm as can be seen in Fig. 6 (b). Fig. 6 (c) presents the photocurrent of the device in response of a pulsed light with a pulse width of 60ps. The rise time is about 20ps, showing a very high time resolution.

III. RESULTS AND DISCUSSION

The device concepts of PD-gated transistors in different material systems have been explored and they all have high gain when operated in the subthreshold region. The brief

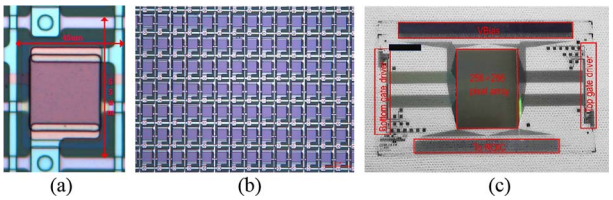

FIGURE 7. (a) Micrograph of the pixel; (b) Micrograph of the partial array; (c) Photo of the image sensor chip.

discussion on these concepts can be found in [16]. In our previous work, we experimentally proved these concepts in single-pixel optical sensors based on PD-gated a-Si:H and LTPS TFTs, respectively [4], [5]. To implement it in image sensors, we further designed and fabricated an a-Si:H TFT-based 256 × 256 image sensor array with 45μm × 55μm pixel size and 505-ppi spatial resolution. Fig. 7 displays the micrographic photos of the pixel, and the partial array, and the picture of the imager sensor array. The manufacturing of the array was conducted in an industrial-standard G2.5 TFT-LCD production line. Fig. 8 (a) illustrates the transfer characteristics of the 3-D dual-gate photosensitive TFT in the array. Upon light exposure, the transfer curves shift negatively and such a shift indicates that the threshold voltage drops with the light illumination. As a result, the output photocurrent increases. Inset of Fig. 8 (a) unveils that the threshold voltage has a quasi-logarithmic dependence on the photon flux, which is consistent with the device model and analysis discussed in the previous reports. As also mentioned previously, the studied photosensitive TFT forms 1-T APS differing from the conventional APSs in that its high SNR is achieved by operating the 3-D dual-gate photosensitive TFT in the subthreshold region where the output current is an exponential function of the threshold voltage. In another word, upon light illumination, a small threshold voltage drop causes an exponential increase in the output current. Thus, the 3-D dual-gate photosensitive TFT exhibits a high gain of $10^2 \sim 10^4$, nearly 2 ∼ 4 orders of magnitude higher than the external quantum efficiency of a typical PIN-type a-Si:H PD (Fig. 8 (b)).

In addition, such a high gain is maintained in a wide spectrum ranging from 300 nm to 1100nm. Therefore, the photosensitive TFT has a full utilization of the incoming photons in the studied wavelength range and is superior to any other approaches. Fig. 8 (c) presents the measured output characteristics of the TFT with and without light exposure. As expected, the output current elevates due to the light-induced threshold voltage.

Moreover, the 1-T APS presented in this work allows a three-phase pixel operation of reset, integration and readout and the CDS can be enabled by simply applying a reset pulse to the top gate. The sampling time of the pixel is mainly governed by the resetting operation. Comparing with the conventional multi-TFT APSs, the proposed one TFT APS removes the external reset TFT and the external PD as well, thus, a reduced pixel sampling time can be obtained.

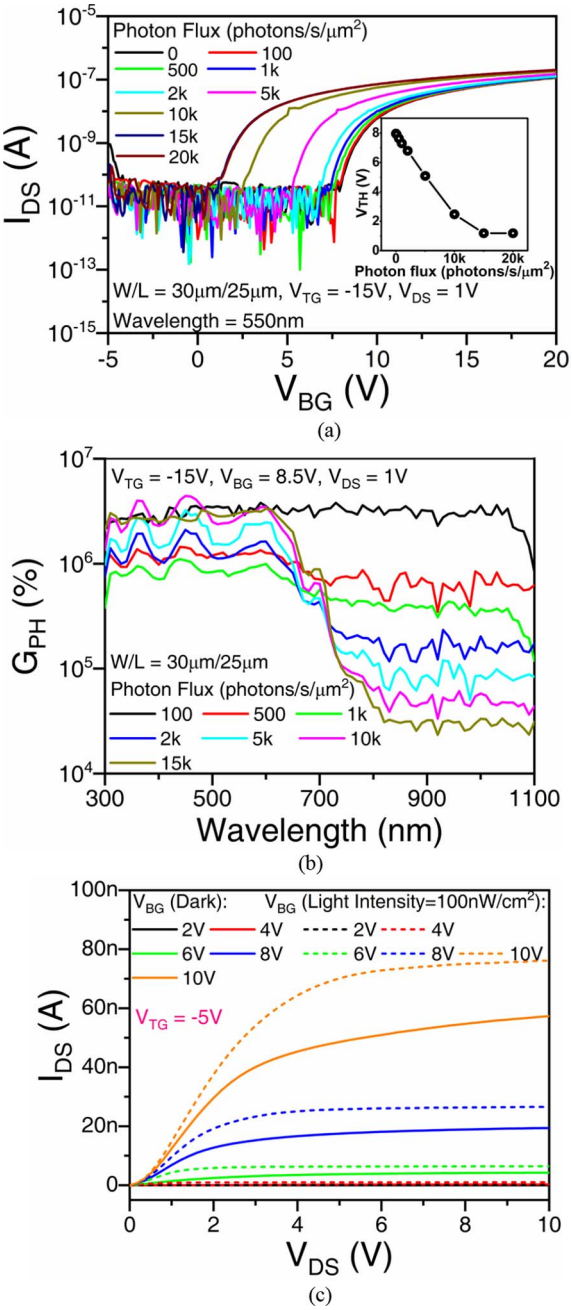

FIGURE 8. (a) Photo transfer characteristics of 3-D dual-gate photosensitive a-Si:H TFT; (b) Gain of the photosensitive TFT as a function of wavelength at various photon fluxes; (c) Output characteristics of the TFT with and without light exposure.

To capture an image using this array, an image acquisition system was developed. Fig. 9 (a) shows the photo of image acquisition system housing FPGA, gate driver ICs, and read-out IC. Fig. 9 (b) gives the original image taken by this array under weak light condition of 22nW/cm^2 (Green LED Light Source) and Fig. 9 (c) presents the processed image after removing the line defects and background noise. Such an image sensor is capable of low-light detection and imaging well-suited for low-dose indirect conversion X-ray imaging and in-display optical fingerprint scanning.

TABLE 1. Summary of this work and prior works for similar applications.

Detectors		Operation	G_{PH} or EQE (@550nm)
APS	3-D photosensitive a-Si:H TFT (this work)	Subthreshold Operation	$>10^4$
	a-Si:H PD-gated LTPS TFT (this work)		$>10^3$
	PD-body-biased MOSFET (this work)		$10^5 \sim 10^7$
	Fin-TFT [7,8,9]		$>10^4$
	p-i-n PD+ AMP TFT [10, 11]	Linear /Saturation Region	~10
	Photo-TFT [12, 13]	Off-Current Region	>100
PPS	p-i-n PD + TFT [14]	Linear /Saturation Region	<0.9
	MSM PD + TFT [15]	Linear /Saturation Region	~0.65

(a) (b) (c)

FIGURE 9. (a) Photo of image acquisition system; (b) Original image of "isense" characters taken by the array; (c) Processed image that removes the bad lines and background.

IV. CONCLUSION

Table 1 lists a couple of key parameters of several similar photodetectors for a comparison. We have demonstrated three kinds of high gain optical sensors based on an architecture of a photodiode-gated transistor. In common, the high gain and sensitivity of these sensors are obtained through operating them in the subthreshold region. The mechanism is the photo-induced threshold voltage drop leading to the exponentially-amplified photocurrent. High spatial resolution is also obtained by the vertical integration of the photodiode and the transistor. We believe this device design will be an alternative to APDs and multi-transistor APS and make a great promise for optical sensing and imaging applications especially requiring high gain and high spatial resolution.

ACKNOWLEDGMENT

The authors are grateful to Mr. Sean Su from Enli, Inc., for assistance in measuring photoresponse and photoconductive gain.

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