Received 5 August 2020; accepted 6 September 2020. Date of publication 8 September 2020; date of current version 3 November 2020.
The review of this article was arranged by Editor S. Reggiani.

Digital Object Identifier 10.1109/JEDS.2020.3022913

Simulation Study on Dynamic and Static Characteristics of Novel SiC Gate-Controlled Bipolar-Field-Effect Composite Transistor

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This work was supported in part by the Science Foundation for Distinguished Young Scholars of Shaanxi Province under Grant 2018JC-017, and in part by the 111 Project under Grant B12026.

ABSTRACT In this article, a novel bipolar-field-effect composite power transistor, called SiC GCBT (Silicon Carbide Gate-Controlled Bipolar-field-effect Composite Transistor) is presented and studied. The structure is characterized by the use of the base-gate short connection mode, instead of the conventional base-source short connection mode in SiC Vertical Double-diffusion MOSFET (VDMOS). It found that the device can obviously improve many problems of SiC Insulated Gate Bipolar transistor (IGBT) caused by the p-type substrates and eliminate the latch-up effect, having very bright prospects in high power and low frequency applications. The dynamic and static characteristics of the SiC GCBT are studied in detail and compared with SiC VDMOS, SiC IGBT and Si IGBT. Through comparative studies, the analysis results indicate that SiC GCBT has superior static characteristics, including a higher breakdown voltage, a relatively smaller threshold voltage (2.98V) and lower on-state voltage drop, and a much larger on-state current which is 28% higher than that of Si IGBT and 71% higher than that of SiC IGBT. In terms of dynamic characteristics, SiC GCBT has the shortest turn-on time, and the turn-off characteristics of the device are also improved compared with SiC and Si IGBT.

INDEX TERMS SiC power device, IGBT, VDMOS, bipolar, on-state current, breakdown voltage, latch-up effect.

I. INTRODUCTION

As one of the most promising semiconductor materials, Silicon carbide (SiC) has become especially popular in the field of high-power device research, because of its excellent properties of materials, such as wide band-gap, high critical breakdown electric field and high electron saturation speed [1]. Among the power devices in SiC, SiC Vertical Double-diffused Metal-Oxide-Semiconductor Field-Effect Transistor (SiC VDMOS) has made a lot of achievements and gradually matured [2]. However, the on-state resistance of unipolar power devices increases as the square of the breakdown voltage (BV), which limit the application of the device especially in the field of high voltage [3]. SiC Insulated Gate Bipolar Transistor (IGBT), as a bipolar device, has gradually replaced SiC MOSFET particularly in high voltage and low-frequency switching applications [4]. N-channel IGBTs performance better than p-channel IGBTs in principle [5], but p-type substrates necessary for n-channel IGBT will bring many problems, such as a high resistance ($0.8 \sim 1.0\Omega{\cdot}cm^2$) in series with the device [6]. What's more, a diode turn-on voltage (about 3.2V) exists in SiC IGBT because of the wide band-gap of SiC [7], which results in a high on-state voltage drop. Thus, SiC IGBT conduction loss even exceeds that of silicon devices [8], so the research of SiC IGBT and its universal application are very difficult.

In order to solve these difficulties, a gate-controlled bipolar-field-effect composite vertical double-diffused transistor, called SiC GCBT, is proposed [9]. This device structure is based on the original SiC VDMOS, which only changes the electrode connection mode, by replacing the original base-source short connection mode with the base-gate short connection mode. In this way, the hole carriers can be injected

into the bulk region, which makes a single carrier device become a double carrier device and greatly improves the forward on-state current. In this article, the static and dynamic characteristics of SiC GCBT are studied and discussed with SiC VDMOS, SiC IGBT and Si IGBT in detail by Technology Computer Aided Design (TCAD) simulation. It found that compared with the SiC IGBT, the structure can significantly alleviate the problems which caused by the p-type substrates and the diode turn-on voltage of 3.2V and prevent the latch-up effect. The presented SiC GCBT has a large *BV*, a relatively smaller threshold voltage (V_{th}) and a much larger on-state current, which are great advantages compared with other devices. In addition, the dynamic characteristics of SiC GCBT are also improved compared with SiC IGBT and Si IGBT. And the smaller turn-on time and lower on-state voltage drop of SiC GCBT help to reduce the conduction loss. These static and dynamic performances help to improve power-handling capability and make it possible for this device to improve energy conversion systems in terms of high power.

II. DEVICE STRUCTURE

The structures of SiC GCBT are shown in Fig. 1(a), and the difference between with SiC VDMOS is only at area A. The structures of two are basically the same and the new structure can be realized by depositing one more area of poly-silicon with other processing stepsunchanged. The biggest difference is that SiC GCBT connects the base region to the gate, which not only provides two conduction channels for the device by the parasitic bipolar transistor and the MOS structure, as shown in Fig. 1(b), but also allows a few holes to inject into the bulk region, so that the a single carrier device become a double carrier device. And Fig. 1(c) shows the conventional SiC IGBT and Si IGBT as comparison devices.

The breakdown mechanism of SiC GCBT is basically the same as that of SiC IGBT and SiC VDMOS in principle, because the gate, source and base are all short-circuited and grounded when turned off. And the high V_{th} of SiC VDMOS [10] can be effectively reduced for that when the device is turning on, the parasitic BJT turns on first, then the MOS structure turns on after the channel inversion. The voltage drop across the p-base makes the channel potential lower than the gate potential, so the channel can be inverted. Most of electrons can directly reach the source from the base region, while others can reach the source by crossing the channel under the gate. In the meanwhile, The holes injected into the drift region from the base region will participate in conduction and increase the current. Moreover, SiC GCBT does not need p-type substrate compared with IGBT, so it can also reduce resistance and improve current. The simulation results support the above analysis results well.

III. RESULTS AND DISCUSSION

In order to study the main characteristics of SiC GCBT, two-dimensional numerical simulation was performed by ISE TCAD [11]. The static and dynamic characteristics are simulated and discussed. Several traditional devices

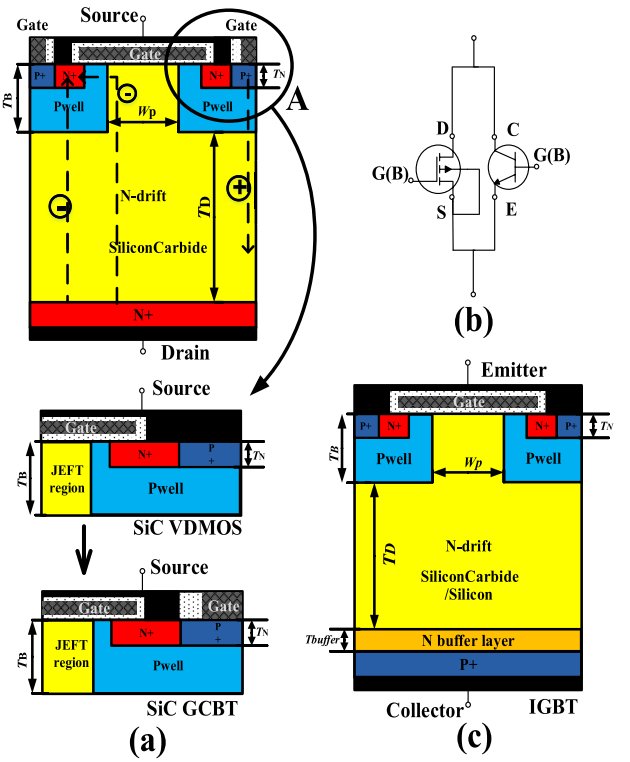


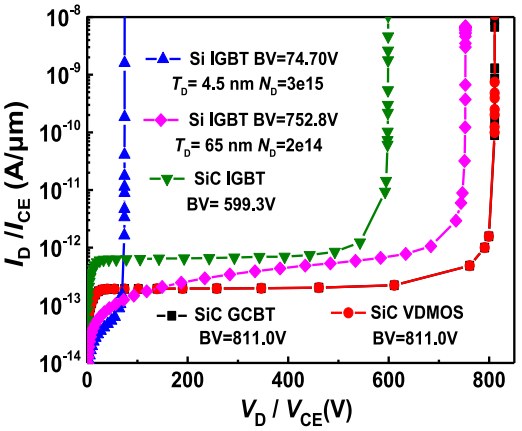
FIGURE 1. (a) Schematic cross-section of the conventional SiC VDMOS and the novel SiC GCBT. (b) The equivalent circuit diagram of the novel SiC GCBT. (c) Schematic cross-section of the traditional IGBT. ($T_D = 4.5\mu m$, $T_B = 1\mu m$, $T_S = 0.3\mu m$, $W_P = 5\mu m$ and $W_B = 4\mu m$ are used in the structures for simulation.)

as comparison, including SiC VDMOS, SiC IGBT and Si IGBT, are simulated under the same conditions for showing the performance advantages and disadvantages of SiC GCBT. The main physics models are applied, including Effective Instrinsic Density, Old Slotboom, mobility (Doping Dep High Fieldsat), Shockley-Read-Hall, Auger Avalanche (Eparal) model for recombination, et. The criterion of breakdown is BreakCriteria {Current (Contact = "drain" Absval = 1e-7)}. In order to verify the correctness of the model, the above models are used to simulate the structure in [12]–[13], and the simulation results agree with the experiments well. Therefore, the model can be used to simulate the proposed structure to obtain reliable results.

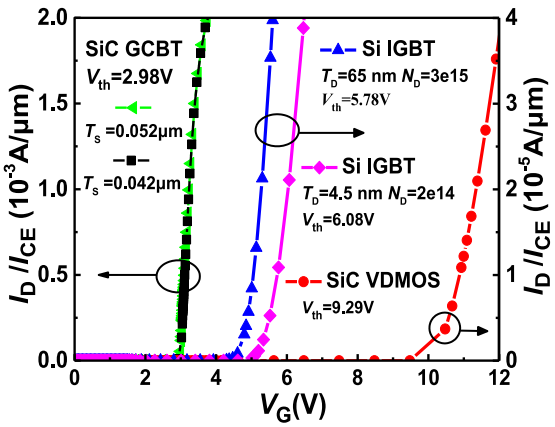
The key parameters in the two-dimensional numerical simulations are listed in Table 1. We choose to use the universal and typical dimensional and physical parameters of the conventional SiC VDMOS [14]. In order to facilitate the simulation, the thinner T_D was selected, which does not affect the performance comparison of the devices in principle. And all the simulation parameters of SiC GCBT used for comparison are exactly the same. As for IGBTs, the only change is to substitute the n-type drain for p-type collector with the same doping concentration, and add the n-type buffer layer. The parameter settings are shown in Table 1, and the N_D will be adjusted appropriately with different devices to obtain accurate breakdown voltage.

TABLE 1. Key parameters used in device simulations.

Symbol	Definition	Values
N_D , cm^{-3}	concentration of N-drift	1×10^{15}
N_P , cm^{-3}	concentration of P-well	4×10^{17}
N_{buffer} , cm^{-3}	concentration of N-buffer	1×10^{18}
T_S , μm	thickness of SiO_2 layer	0.052
T_D , μm	thickness of N-drift layer	4.5
T_B , μm	thickness of P-well	1
T_N , μm	thickness of source layer	0.3
T_{buffer} , μm	thickness of N-buffer	0.5
W_p , μm	width of JFET region	5
Lc , μm	length of channel	1



(a)



(b)

FIGURE 2. (a) Simulated breakdown voltage comparison curves for SiC GCBT and other devices. (b) Simulated threshold voltage characteristics comparison curves of the devices. (V_D = 10V).

A. STATIC CHARACTERISTICS

The comparison curves of breakdown voltage are shown in Fig. 2(a). The results show that the *BV* of SiC GCBT is identical with that of SiC VDMOS, because the breakdown mechanism of the two devices is totally the same in the off state when the gate, base and source are grounded. In addition, the *BV* of SiC IGBT is lower than that of SiC GCBT with the same T_D, which is due to the existence of an n-type buffer layer with a slightly higher concentration than N_D. Besides, thanks to the wide band gap of SiC materials, the *BV* of SiC GCBT is 10 times higher than that of Si IGBT with the same T_D, while if the *BV* of Si IGBT wants to reach the same level (about 800V), the T_D is required to reach over 65nm, which will greatly reduce the other performances of the device.

The threshold voltage comparison curves of the devices are drawn in Fig. 2(b). Illustrated by graphs, the V_{th} of SiC GCBT is almost unchanged with the increase of T_S, hence, it can be inferred that the V_{th} is the on-voltage of parasitic bipolar transistor (about 3V) while the V_{th} of SiC VDMOS and SiC IGBT are both the on-voltage of MOS structure (about 9V). When the T_S is 0.052μm, the V_{th} of SiC VDMOS is 9.29V, and that of Si IGBT with the same T_D and with the same *BV* is 5.78V and 6.08V respectively, while the V_{th} of SiC GCBT is 2.98V, which is one third of that of SiC VDMOS, and about one-half of that of Si IGBTs.

The forward current–voltage ($I-V$) characteristics when gate voltage (V_G) is 10V are shown in Fig. 3(a). When V_D is 20V and W_P is 5μm, the I_D of SiC GCBT is 1.66×10^{-3}A/μm, that is 16.7 times larger than that of traditional SiC VDMOS which is only 1.052×10^{-4} A/μm. And a section of current (V_D = 6V to 18V) in stable state is selected to calculate the open state resistance (R_{on}), the results show that the R_{on} of SiC GCBT (4.017Ω·cm^2) is about 1/7 of that of SiC VDMOS (29.032Ω·cm^2). This is a very attractive advantage that conducive to high power applications.

But there is a negative current at the beginning, which is a potential disadvantage of SiC GCBT. It can been seen from Fig. 3(a) that the maximum negative current is quite large, which can be −0.0654A/μm and the current goes up to positive when V_D rises to 1.9V. Because that the PN junction between source and base will open first under the large V_G while the V_D is small, at this time, the electron current from the source to the base will show a negative flow. Then, with the increase of V_D, parasitic BJT will be turned on, and the positive current generated will cancel out the negative current, making the overall current turn to positive. How to avoid and reduce this negative current is a difficult problem worthy of consideration and in-depth study.

During the research, it found that with the change of the width of JFET region (W_P), the current of SiC IGBT changes a little under the same conditions, which is also a valuable advantage. Fig. 3(b) draws the $I-V$ characteristics varying with W_P, which has an influence that cannot be ignored on SiC VDMOS [15]. According to Fig. 3(b), when V_D = 20V and W_P decreases from 5μm to 3μm, the I_D of SiC GCBT decreases by 0.09×10^{-3}A/μm, accounting for 5.42%, while I_D of SiC VDMOS decreases by 0.572×10^{-3}A/μm, accounting for 54.45%. The comparison of the decline rate reflects that W_P has less effect on SiC GCBT. To explain this phenomenon, the current distribution on cross section are show in Fig. 4, from which it can been seen that the current

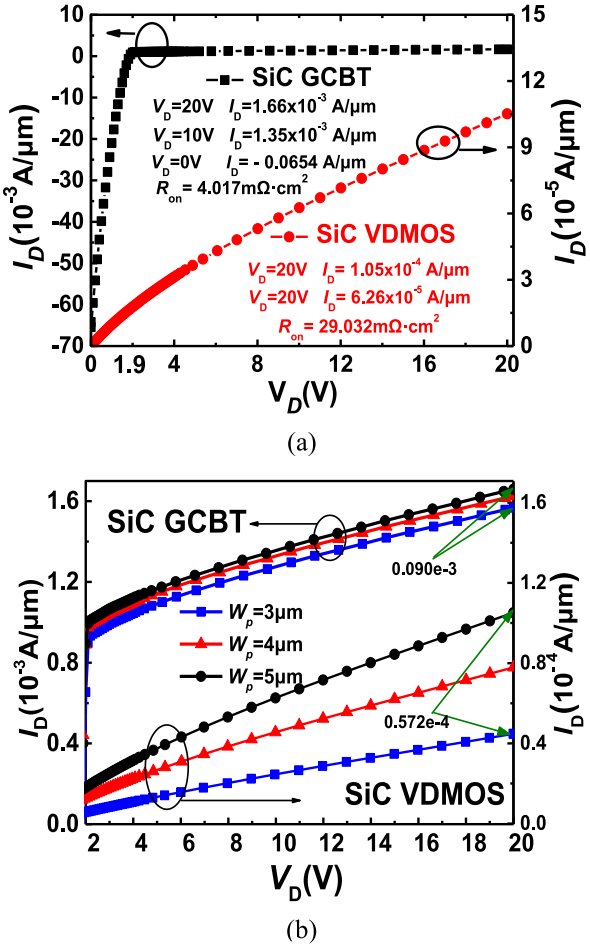


FIGURE 3. (a) Simulated forward $I-V$ characteristic for SiC GCBT and SiC VDMOS. (V_G = 10V) (b) The forward $I-V$ characteristics of SiC GCBT and SiC VDMOS changing with W_P.

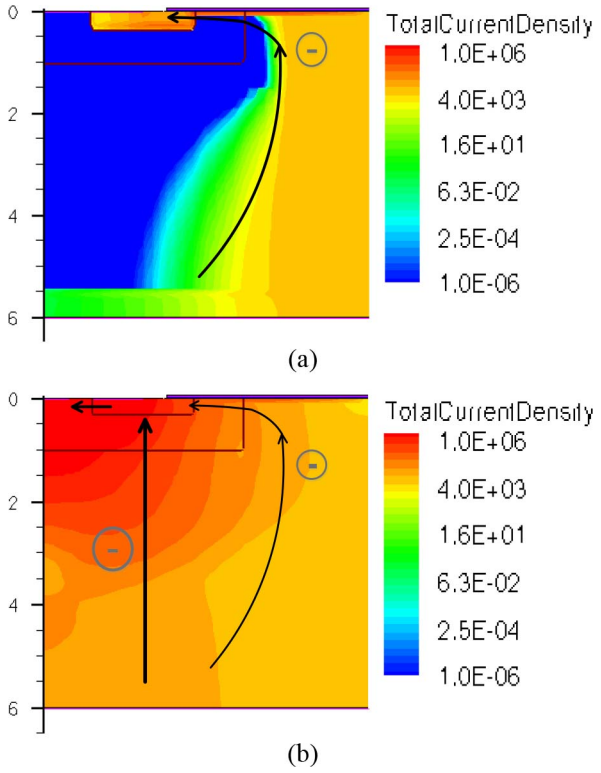


FIGURE 4. The distribution of current density of (a) the conventional SiC VDMOS and (b) the proposed SiC GCBT. (V_D = 20V, V_G = 20V and V_S = 0V).

density is more crowding in JFET region of SiC VDMOS, while most of electrons of SiC GCBT is flow through the edge of devices indicated n Fig. 4(b). Therefore, the current of SiC GCBT is less affected by W_P, which means the device is less influenced by JEFT resistance and more conducive to the improvement of integration.

In addition to compared with that of SiC VDMOS, the $I-V$ characteristics of SiC GCBT are also compared with that of Si and SiC IGBT. The Si IGBT and SiC IGBT with the same T_D are chosen for simulation, while the IGBT with the same BV it is not selected because the T_D is too thick and the performance is too poor. The results are shown in Fig. 5(a). When V_{CE} is 10V, it is noticed that SiC GCBT obtains a maximum on-state current (I_{CE}) of 1.36×10^{-3}A/μm. Under the same conditions, this current value is 28% higher than that of 1.06×10^{-3}A/μm for Si IGBT and 71% higher than that of 7.96×10^{-4}A/μm for SiC IGBT. The reason is that the p-type substrates which cause high series resistance of SiC IGBT are not present in SiC GCBT, and the P-type base region is used to inject holes instead of the p-substrate. At the forward current density (I_{CEsat}) of 2×10^{-4} A/μm, the diode turn-on voltage (V_{on}) of SiC IGBT is 3.26 V, while the V_{on} of SiC GCBT is 1.88V, a decrease of 42%, which means that the problem of high diode turn-on voltage caused by wide band-gap in SiC IGBT has been improved obviously.

What's more, the proposed SiC GCBT has no latch-up effect, which is an important problem to limit the high voltage application of IGBTs [16]. The IGBT inherently has a parasitic thyristor structure, and when a current arises in this thyristor it means the latch-up of the IGBT [17]. But in SiC GCBT, the equivalent circuit becomes a triode instead of a thyristor, so the latch-up effect won't happen. This can be illustrated in Fig. 5(b). It can be seen that both Si IGBT and SiC IGBT have very obvious phenomenon of sharp increase of current with decrease of voltage, what we called latch-up effect. But for SiC GCBT, there is no such phenomenon, and as the voltage increases to 180V, the current increases almost stably, which makes it possible for the device to work at a higher voltage.

B. DYNAMIC CHARACTERISTICS

The circuit with a resistive load, shown in Fig. 6(a), is used to simulate the devices under the input signal of the gate shown in Fig. 6(b). As mentioned above, SiC VDMOS structure, SiC IGBT structure and Si IGBT structure with the same T_D are all selected to make a simulation comparison with the proposed SiC GCBT structure. In order to ensure that all simulation objects can work normally, we choose to set

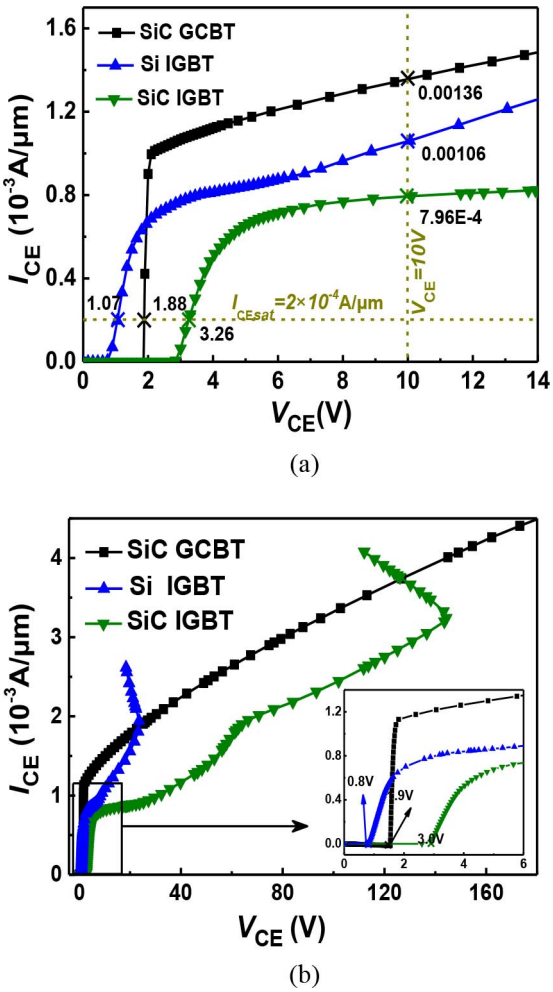


FIGURE 5. (a) Simulated forward $I - V$ characteristic for the proposed SiC GCBT and the traditional SiC IGBT and Si IGBT with the same T_D. (b) Latch up effect of the above three devices. (V_G = 10V).

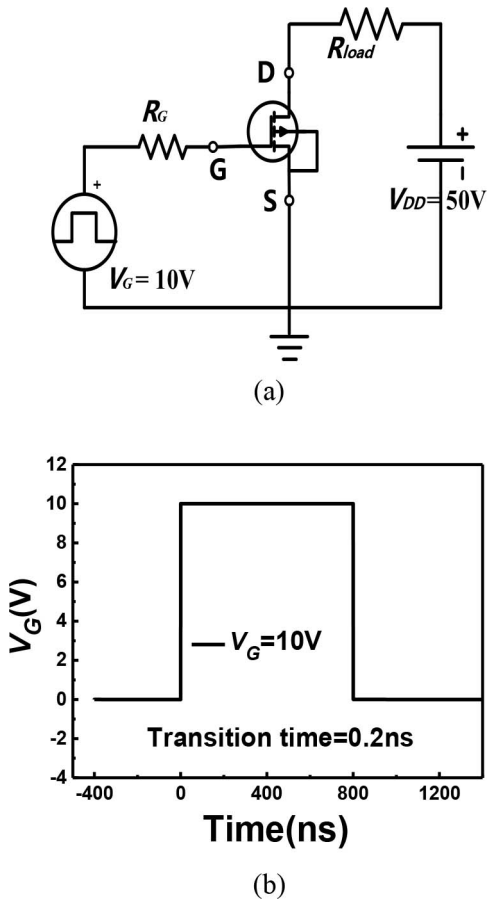


FIGURE 6. (a) The switching circuit with a resistive load for the devices. (b) The input signal curve of the gate. (V_G = 10V, Transition time = 0.2ns).

V_{DD} as 50V, V_G as 10V, and load resistance (R_{load}) value as $1 \times 10^7\Omega$ and resistance of gate (R_G) as 5Ω.

The voltage and current curves at opening are shown in Fig. 7(a). When the voltage drops to 10% of the highest voltage, and the current rises to 90% of the highest current in the working state, the device is considered to be turned on. The time difference between this time and the rise time of gate voltage is defined as the turn-on time (t_{on}) of the device. As can be seen from the Fig. 7(a), SiC GCBT has the shortest t_{on} of 0.148ns, while the t_{on} of SiC VDMOS, SiC IGBT and Si IGBT are 0.496ns, 0.408ns and 0.504ns, respectively. The t_{on} of SiC GCBT is 0.348ns shorter than that of SiC VDMOS because double carriers are involved to participate in the electric conduction and a few other factors are caused by lower V_{th}, and 0.356ns shorter than that of Si IGBT because of the advantages of SiC materials.

The turn-off waveforms of the devices are shown in Fig. 7(b), and the devices are considered to be turned off when the current drops to one tenth of the highest current in the working state. The time difference between this time and the time when the V_G starts to drop is defined as the turn-off time (t_{off}) of the device. As a unipolar power device, SiC VDMOS has excellent turn off characteristics with the shortest t_{off} of 21ns. But it should be noticed that the turn-off waveform of the proposed device has a reaction time for 99.1ns before the current starts to drop, this small reverse current perhaps will bring some difficulties to the application of SiC GCBT in high frequency circuits. Neglecting this reaction time, the t_{off} of SiC GCBT is 40.1ns, twice of the switch speed of SiC VDMOS. It is gratifying to have such a fast speed for a bipolar device, which may be due to the comparable switching speed of SiC BJT compared with SiC MOSFET [18]–[19]. The total turn-off time of SiC GCBT is 139.2ns, which is 7.0ns lower than that of SiC IGBT (146.2ns), and 15.2ns lower than that of Si IGBT (154.4ns), which is due to the low minority carrier lifetime of SiC materials and the long tailing current of IGBTs.

After years of development, MOSFET structure has been very mature and versatile, so any structural change may reduce its applicability in some aspect. Therefore, there are some concerns about SiC GCBT after changing the original short connection mode of the base region. The first concern is that the absence of voltage drop between source and

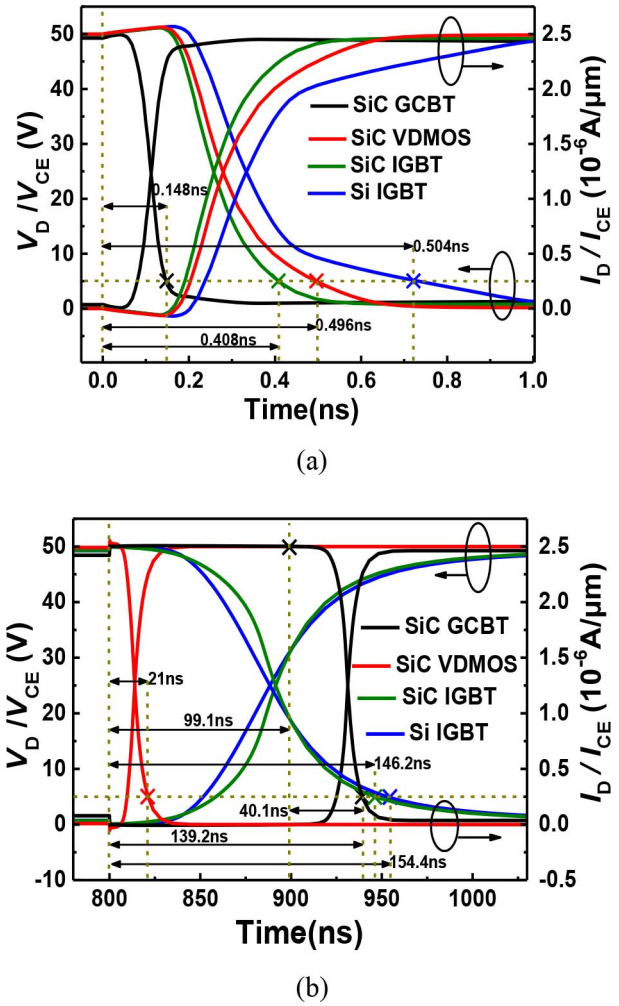


FIGURE 7. **(a) Simulated resistive turn-on characteristics for SiC GCBT and other devices. (b) Simulated resistive turn-off characteristics for SiC GCBT and other devices.**

p-base cannot be guarantee in the actual application, which means the drain will not be able to withstand the same high breakdown voltage as SiC VDMOS. Another thing to worry about is that the body diode formed in the body (base)-drain p-n junction of a power MOSFET may not be as convenient as the one in MOSFETs. So this device may not be suitable for half-bridge converter circuits and full-bridge converter circuits in motor control applications. Besides, the negative current appeared at source may limit the high-frequency application. However, SiC GCBT solves many existing difficulties of SiC IGBT, so it can be a potential substitute in other applications. Of course, we are also committed to finding better solutions in the follow-up research.

IV. CONCLUSION

A novel bipolar carrier device (SiC GCBT) is proposed to solve the existing problems of SiC IGBT in this article. Its static and dynamic characteristics compared with other traditional devices are simulated and discussed, including SiC VDMOS, SiC IGBT and Si IGBT with the same T_D and with the same BV. The mainly comparison results have been listed in Table 2.

TABLE 2. **Key comparison results of the devices.**

Symbol	Description	SiC GCBT	SiC VDMOS	SiC IGBT	Si IGBT
BV	Breakdown voltage (V)	811.0	811.0	599.3	74.7
V_{th}	Threshold voltage (V)	2.98	9.29	9.29	6.08
$I_{on\text{-}state}$	The current (A/μm) when V_D=V_G=10V	1.36 ×10^{-3}	6.26 ×10^{-5}	7.96 ×10^{-4}	1.06 ×10^{-3}
V_{on}	the turn-on voltage (V)	1.88	/	3.26	0.8
Latchup	Is there a latch up effect	no	no	yes	yes
t_{on}	The turn-on time(ns)	0.148	0.496	0.408	0.504
t_{off}	The turn-off time(ns)	139.2	21	146.2	154.4

In terms of static characteristics, the results show that with the same structural parameters, the BV of SiC GCBT is equal to that of SiC VDMOS, about 26% higher than that of SiC IGBT and 10 times higher than that of Si IGBT. The V_{th} of SiC GCBT is one third of SiC VDMOS and about one-half of that of Si IGBT. And SiC GCBT has a large on-state current, which is 16.7 times of that of SiC VDMOS and almost unaffected by JEFT resistance. Furthermore, this large current value is 71% higher than that of 7.96×10^{-4}A/μm for SiC IGBT and 28% higher than that of 1.06×10^{-3}A/μm for Si IGBT. The V_{on} of SiC IGBT is 3.26V, while the V_{on} of SiC GCBT is 1.88V, a decrease of 42%. And SiC GCBT also has no latch up effect, which means that the problems of SiC IGBT, like high resistance introduced by p-type substrate, high diode turn-on voltage caused by wide band-gap and latch up effect, have been improved obviously.

As for dynamic characteristics, SiC GCBT can be turned on and off normally, and has the shortest t_{on} of 0.148ns, which is 0.348ns shorter than that of SiC VDMOS and 0.356ns shorter than that of Si IGBT, which can help to reduce the conduction loss. The total turn-off time of SiC GCBT is 139.2ns, which is 7.0ns lower than that of SiC IGBT, and 15.2ns lower than that of Si IGBT. However, the negative current appeared at source causing a small but long reverse current when turn off, which does harm to the t_{off} and may limit the high-frequency application of the device, although it does better than SiC IGBT. This problem and other potential limitations will be the important issues for us to do further research.

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